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THE DESIGN OF A SEMI-CUSTOM INTEGRATED CIRCUIT FOR THE SLAC SLC TIMING CONTROL SYSTEM *

ERIC LINSTADT
Stanford Linear Accelerator Center, Stanford, California, 94305

Abstract

A semi-custom (gate array) integrated circuit has been designed for use in the SLAC Linear Collider timing and control system. The design process and SLAC's experiences during the phases of the design cycle are described. Issues concerning the partitioning of the design into semi-custom and standard components are discussed. Functional descriptions of the semi-custom integrated circuit and the timing module in which it is used are given.

1. Introduction

The timing and synchronization requirements of the SLC control system architecture[1] are met by a CAMAC module which distributes 16 independent channels of timing information to other modules within a CAMAC crate. Each timing signal is a pulse delayed relative to a fiducial, or beam time pretrigger, by an amount of time programmable in 8.4 nsec increments, over the entire 2.78 msec (360 Hz) interpulse period. A 119 MHz square wave with a missing pulse denoting the fiducial time is made available to the module, and a semi-custom integrated circuit, whose design is detailed in the following sections, uses this square wave as a clock to generate the required delayed output pulses. These output pulses, 67.2 nsec (8 clock periods) long, are distributed to the rest of the CAMAC crate as differential ECL signals by means of an auxiliary upper backplane.

2. Semi-Custom Design

A design that is realised solely with standard integrated circuits may be inappropriate for an application due to cost, size, power consumption, complexity, maintainability, or speed. A growing industry now offers the service of customising only the final interconnection of preprocessed circuit elements on mass produced wafers. An example is the gate array, a chip which contains several identical cells of uncommitted transistors and resistors. These may be connected in different ways to perform assorted logical functions. This provides the benefits of integrating entire printed circuit board assemblies onto a single chip, while sharing the time and costs of mask and wafer development and circuit characterization among several small to moderate volume users.

Several factors influence the selection of a particular device. The system speed requirement determines the appropriate device technology. The density of the device, the number of available signal I/O's and their levels (TTL, ECL, or both) determine the amount of system integration which is possible, and influence the ultimate system cost. Device packaging and thermal management must also be considered. Vendors are selected by the CAD facilities and services they offer, device availability, the time required for the delivery of prototype and production quantity parts, and the existence of alternate source agreements.

The device we selected was the Fairchild[2] FGE 2000 ECL gate array whose relevant features are listed in Table 1.

Table 1. FGE 2000 Features

- ECL Gate Array
- 224 Internal Logic Cells
- 26 Transistors and 16 Resistors Per Cell
- 2000 Gate or 224 D Flip–Flop Equivalent Logic Density
- 120 Signal I/O's
- 25 Ω Output Drive Capability
- Programmable Speed, Power and Output Drive Options
- Fully Integrated CAD System
- MSI Cell Library
- 132 Pin Ceramic Pin–Grid Array Package
- 7° C/W Junction to Ambient Thermal Resistance θ_{ja}

The design process is outlined in Fig. 1. A schematic capture program is used as a means of entering the netlist, the description of the desired logical components (intra-cell connections) and their interconnections. The schematic is composed of elements contained in the cell library. The cell library contains descriptions of the logical functions which correspond to previously defined connections between the uncommitted resistors and transistors fabricated on the wafers. This allows the design to be described at a level of complexity corresponding to that of standard SSI and MSI components. A logic simulator is then used to verify the functionality of the network, by observing the outputs and states of internal nodes in response to sequences of input vectors. Only preliminary timing estimates may be made at this point, as the loading due to interconnection lengths are unknown. When the results of the logic simulation are satisfactory, placement and routing programs are used to assign device inputs and outputs to physical package pins, place logical cells within the array, and route the interconnections. This may be done either manually or automatically. Manual placement and routing allows the optimization of time

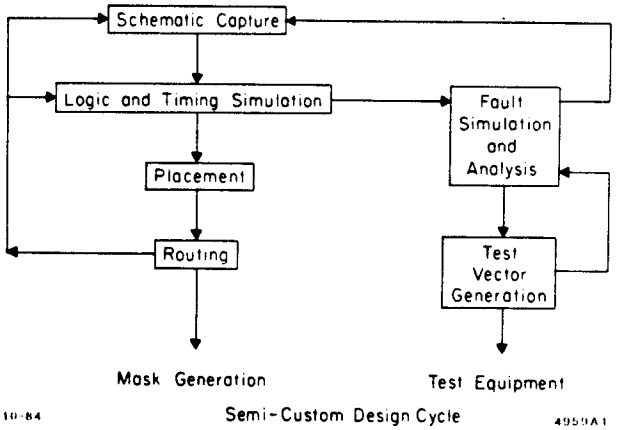

Figure 1

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critical paths, and is often is necessary to finish connecting nets that an auto-routing program could not complete. Auto-placement programs generally have routines to allow the optimization of global geometric features such as total interconnection length or routing congestion. Once placement and routing are completed, a timing simulation may be performed using the actual netlengths. Upon approval of these results, the fabrication of prototype chips may be started. After acceptance testing of the prototypes, a separate production agreement may be negotiated.

The manufacturer must be provided with information to test the finished device. In bipolar devices, faults are successfully modeled at the gate level by assuming that circuit nodes become stuck at either logical high or low levels. A fault is observable if, in response to a sequence of inputs, its presence is manifested at the output of the device as a difference between actual and expected values. A necessary condition for the observability of a fault is that the fault state be controllable. That is, you must be able to generate the effect of the fault at its source. For example, a stuck-at-low fault of the output of an AND gate is controllable if the set of test vectors manipulate the surrounding network so that all of the inputs to the AND gate are in the 'high' state at the same time. This fault would be observable if its effect were propagated to the output of the device. The controllability analysis of a set of test vectors, the percentage of faults potentially detectable, is relatively straightforward to perform, while the observability analysis is computationally a much more complex problem, and frequently is run on larger computers or with special hardware. It is reasonable for a manufacturer to refuse to build a chip whose controllability or observability is so low as to be essentially untestable. In general, the vectors used in the logical functional simulation are inadequate for device testing, and additional test vectors must be written. Quite often, particularly for designs involving substantial amounts of sequential logic (i.e., counters), additional circuitry must be added to allow the testing of the device in an acceptable amount of time.

3. The Eight Channel Alarm Clock

The SLC timing system design criteria could be met by building a presettable counter for each channel, using the terminal count to generate the required output pulse. However, a counter uses substantial amounts of combinatorial logic around the flip-flops of each bit. A significant reduction in the total amount of logic required is obtained in our design by sharing the logic costs associated with a counter among eight channels. The form of the design resembles that of a content addressable memory. As well as being able to write to and read from addressed locations, a content addressable memory has a match output associated with each word in memory. This output is asserted whenever a data word presented to the array is identical to the data stored in that memory location. This is accomplished in parallel for each word in memory by having the output of each latch feed an exclusive-or gate, which performs the comparison with the appropriate data bit. The outputs of all of the exclusive-or gates in a word are summed together to generate the match output, as shown in Fig. 2.

The completed chip is constructed as follows. There are eight 20-bit words of memory, composed of transparent latches. The outputs of a 20-bit, pseudo-synchronous, resettable up counter, indicating the time elapsed since the last fiducial,

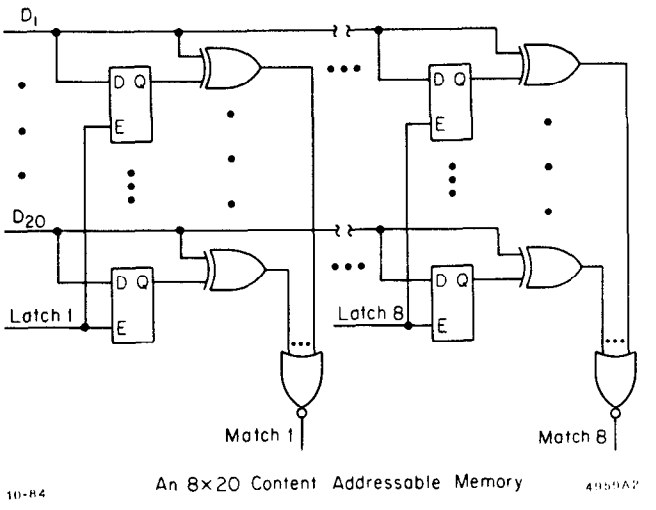

Fig. 2. In our design, after the desired times of output pulse generation have been latched in the 8 words of memory, the counter places the time elapsed since the last fiducial onto the 20 data lines.

are compared with the data stored in memory. Match outputs are generated internally for both the 3 least significant and the 17 most significant bits of each word. The match output of the 3 LSB's is used to gate the match output of the 17 MSB's, and thereby produces an eight clock cycle wide output pulse. The match outputs, as well as a buffered version of the input clock, are able to directly drive the auxiliary upper backplane, and are enabled by a separate input control line. Another differential output pair is the logical AND of the second and third most significant bits of the counter, being asserted at the 3/8 and 7/8 points in the counters range, and de-asserted at the 0 and 1/2 points, and is intended to be used to indicate counter overflow.

Additional chip inputs were necessary for the testing of the counter and the memory array, and could be used in other applications to either preload the counter or to gate the input clock. Results from the fault simulator indicate that the test vectors will detect nearly 99% of the possible faults. More than 95% of the internal logic cells in the array were utilized, and the worst case power consumption is estimated to be 7 Watts. Timing simulator results indicate worst case operation to above 140 MHz with a 50% duty cycle clock. The design was completed in approximately 5 weeks.

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References

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2. Fairchild Camera and Instrument Corp., Gate Array Division, 1801 McCarthy Blvd., Milpitas, CA 95035