

DESIGN AND PERFORMANCE OF THE STANFORD LINEAR COLLIDER CONTROL SYSTEM*

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Abstract

The success of the Stanford Linear Collider (SLC) will be dependent upon the implementation of a very large advanced computer-based instrumentation and control system. This paper describes the architectural design of this system as well as a critique of its performance. This critique is based on experience obtained from its use in the control and monitoring of 1/3 of the SLAC linac and in support of an extensive experimental machine physics experimental program.

1. Introduction

The SLAC Linear Collider¹ (SLC) project will provide electron-positron colliding beams at a center-of-mass energy of 100 GeV with a luminosity in excess of $10^{30} \text{ cm}^{-2} \text{ sec}^{-1}$. The SLC general layout in Fig. 1 shows how the existing SLAC 2 mile linac will be combined with several additional accelerator components to produce colliding beams.

An accelerator cycle will begin with the assumption that the electron and positron damping rings each contain two equally spaced high-intensity low-energy bunches. One of the positron bunches will be extracted from the damping ring, passed through a bunch-length compressor, and injected into the linac. Then both electron bunches will be extracted from the electron damping ring, passed through a bunch-length compressor, and injected into the linac. The typical spacing of the three bunches in the linac will be about 15 meters.

The three bunches will be accelerated along the linac. The third bunch, an electron bunch, will be extracted from the linac at the two-thirds point and directed at a positron production target. The first two bunches, a positron bunch followed by an electron bunch, will continue to the end of the 2 mile linac where they will have attained an energy as high as 50 GeV. At the end of the linac, the two bunches will be separated by a DC magnet and each will then pass through approximately 4000 feet of matching transport, collider arc, and a final focusing section, before colliding at the interaction point.

In the mean-time, the positrons produced by the third "scavenger" electron pulse will be focused and accelerated and then brought back to the beginning of the linac. These positrons will then be accelerated through the first linac sector and injected into the positron damping ring to replace the positron bunch that was previously ejected. Then two bunches of electrons, created by the electron gun and electron booster, will be accelerated through the first linac sector and injected into the electron damping ring to replace the two electron bunches previously ejected. The following cycles will continue in the same manner with the positron bunch, that is extracted then replaced, alternating between the two positron damping ring bunches.

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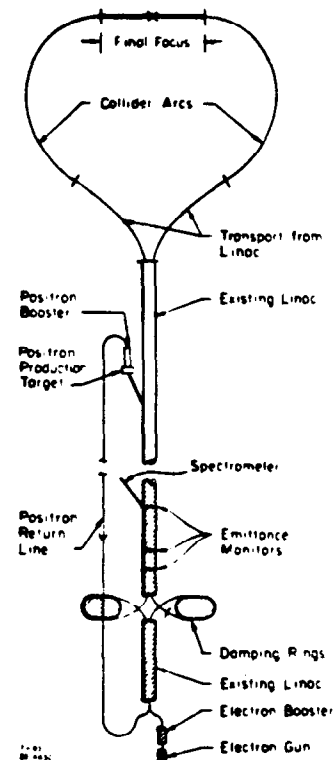


Fig. 1. Layout of the SLAC Linear Collider.

The purpose of the SLC Instrumentation and Control (I&C) system is to produce the appropriate monitoring and control functions to successfully direct the complex SLC operation described above in order to deliver two reliable low-emittance beams to the collision point. The system must also provide a quick and efficient means of switching between SLC operation and other linac operations, such as delivery of beams to the experimental yard and the filling of the SPEAR and PEP storage rings.

The first chore for the control system is to provide an efficient and flexible means for setting up the thousands of devices which affect the beam parameters. Then the system must monitor the beam parameters and make appropriate corrections to the initial settings. Finally, the system must monitor the health of all components and automatically correct for inoperative devices, if possible, or at least notify the machine operators of a failure.

The SLC I&C task is especially demanding because of the tight beam-tolerance requirements and the very large number of unique devices that affect the beam. Further, the control system must not only work flawlessly, but it must simultaneously allow for the rapid development and testing of new or upgraded

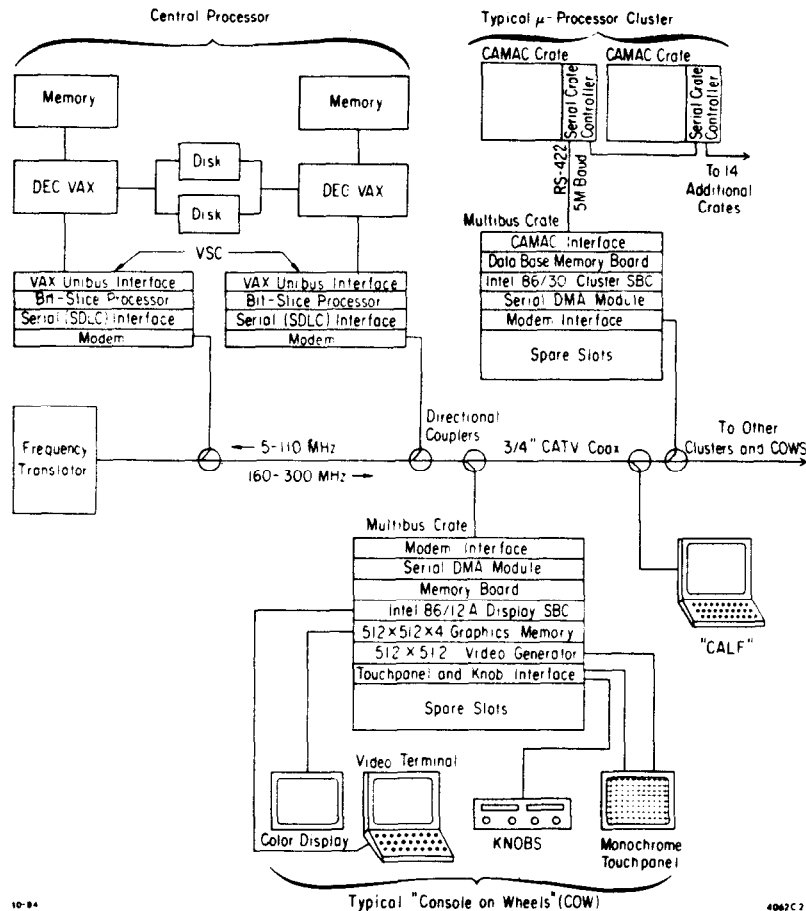


Fig. 2. The SLC computer control system.

algorithms in order to maximize the SLC performance.

The "old" linac computer control system² is based primarily on a "look-and-adjust" manual control system. The SLC requirements preclude this type of control philosophy. Rather, a control philosophy based on machine modeling such as successfully employed in the SPEAR³ and PEP⁴ storage rings is required. Further, the old system has its roots based on technology that is nearly twenty years old. Therefore, the linac I&C is being replaced by a new system that will assume the functions of the present system plus provide a greatly enhanced capability for the precision control and monitoring of devices as well as the implementation of a model driven control system.

The complexity of the SLC project has dictated the "new" control system be implemented in several phases such that it can be installed and made operational without disturbing the continuing operation of accelerator components and so that it can be used to support the development efforts of accelerator physicists who are testing and studying the various accelerator systems as they become available for SLC use. To this end, the first phase of the control system became operational in 1981 to support the testing of the injector and the first linac sector. This system was based on the use of a mixture of SLC prototype hardware and older hardware designs from the PEP storage ring control system.⁵ In the fall of 1983, the second phase of the system became operational using production quality hardware and software to control most of the equipment in the first third of the linac, the injector, and one damping ring and compressor. This system, which contains nearly all of the control system

Fig. 2. The SLC computer control system.

components that will be required for the full implementation of the overall control system, has been operational for about a year now. It has been extensively used and a great deal of experience has been obtained with respect to its operation and performance.

Further control system efforts will center on the improvement and refinement of the system hardware and software as well as extending the system to serve all SLC accelerator components. In addition, a tremendous amount of applications oriented software must be developed to provide efficient SLC operation. The whole system must be operational for support of the formal SLC start-up activity scheduled to begin in October, 1986.

2. The Computer System

In its final state, the SLC computer control system will be an order of magnitude larger and more complex than any of SLAC's other accelerator control systems. The final system provides a combination of two large central processors networked to 70-100 μ -processor clusters, as shown in the block diagram in Fig. 2. Each of these clusters has the capability of supporting an arbitrary number of 16-bit single-board computers operating in parallel. It is estimated that the initial total processing power placed into operation for the new linac control system alone will be 15-25 times greater than the processing power in the existing system. Further, the system can be easily expanded to include much more processing power in the future.

The μ -processor clusters interface directly to the equipment

to be monitored and controlled and are distributed near their related accelerator components. Clusters are located in each of the 30 linac sectors and near the damping rings, electron gun, positron source, etc.

Operator control and monitoring of the system is performed through the use of "Console-On-Wheels" (COW's). Further, access to the system by technical support personnel is provided by the use of portable terminal based "CALF's" which can be easily moved to any geographical location.

The current operational system contains 2 Digital Equipment Corp. (DEC) VAX 11/780's, approximately 50 μ -processor clusters, 7 COW's, and approximately 40 terminals which can be used as CALF's.

2.1 HARDWARE ARCHITECTURE

2.1.1 Central Computers: The heart of the SLC computer system is based on two DEC VAX systems each with twin disks. These computers provide on-line execution of large modeling programs and serve to interface with the machine operators in order to direct the overall efforts of the control system. These computers also serve as a base for both the VAX and μ -processor software development efforts.

The system is currently operated with one VAX serving as the "on-line" processor while the second one serves to support the development effort. In the event of a hardware failure, the roles of the computers can be interchanged with relatively simple hardware switching operations.

The VAX's have been chosen for use as central computers because their virtual-memory operating system can simultaneously support many physically large, CPU-bound operating programs and on-line users, as well as provide an environment for fast, efficient program development and maintenance. There are other processors which can also provide these features, but the VAX was chosen because of extensive hardware and software support already existing at SLAC.

2.1.2 Micro-Processor Clusters: The distributed μ -processor clusters are based on the Intel Multibus architecture. This architecture provides support for the arbitrary number of single-board computers (SBC) which communicate with each other through the use of shared memory and interrupts. Currently, the μ -processor clusters contain an Intel 86/30 SBC, 768 kilobytes of RAM and 8 kilobytes of EPROM. Various benchmark tests have shown that each μ -processor cluster has somewhere between 1/10 and 1/7 the processing power of the VAX 11/780.

The actual interfaces to the SLC technical components will be made through the use of CAMAC. The CAMAC crates are located very near to their related equipment. It is anticipated that the entire SLC system will eventually contain ~250 crates. The crates are interfaced to their respective Multibus crates through high-speed (10 μ sec/cycle) low-cost serial crate controllers that were developed at SLAC. The Multibus/CAMAC interface is a high-speed Direct Memory Address (DMA) device that directly executes lists of CAMAC commands from the Multibus address space.

The choice of specific equipment for the μ -processor cluster was carefully examined with respect to the FASTBUS architecture. The powerful and flexible FASTBUS architecture easily meets all of the cluster requirements and could potentially be used to replace both the Multibus and CAMAC crates. However, the overall SLC schedule did not allow adequate time

to develop and support a FASTBUS implementation of the μ -processor clusters. In contrast, both Multibus and CAMAC are mature systems that are well supported by industry and within SLAC.

2.1.3 Communications Network: Almost all SLC communications are based on the use of a broadband (5-300 MHz) Cable Television (CATV) system⁶ that has the capability to support several hundred frequency-divided communications channels on a single 3/4 inch coaxial cable. This cable is installed in all equipment areas, control rooms, and laboratory development areas. Approximately 5 miles of cable has been installed to date and it is anticipated that the system will eventually extend over 7 miles.

A high-speed one Megabaud polled network⁷ has been developed at SLAC to interconnect the μ -processor clusters with the VAX's. This network is based on an SDLC⁸ protocol and uses a bit-sliced μ -processor to direct the sequential polling operation and to serve as a high-speed DMA channel into the VAX. The μ -processor clusters communicate with the network by using commercially available SDLC communications modules and modems. The use of a bit-sliced μ -processor as the network controller allows the system to poll at a rate in excess of 1200 polls/second.

Terminal to VAX communications are supported with commercially available equipment using protocols similar to Ethernet. Several hundred terminals are supported on one 125 kHz cable channel.

The cable also provides several television, voice and point-to-point data channels.

2.1.4 Operator Consoles: The system contains two types of operator consoles. A more elaborate type has been given the name of Console-On-Wheels (COW) because it is a fully portable unit which may be connected to any of the CATV communications system ports. It contains a 4 color, 512 element x 512 line graphics display; a 8x8 button touch panel; 8 general purpose slew knobs; and an Ann Arbor Ambassador VDT. The COW is based on the Multibus architecture and contains a SBC to provide local intelligence.

The second type of console is called a CALF because it is a smaller (more portable) and less expensive version of the COW. It consists of an Ann Arbor Ambassador terminal and modem which allows it to be attached to the CATV system. The CALF can emulate a subset of the COW functions and nearly any operation that can be performed using a COW can also be performed using the CALF without the development of special software.

Although the CALF was developed to be primarily used by technical support personnel for maintenance and development activities, it has found wide use for direct control of the accelerator in applications where the high cost of the COW cannot be justified.

2.2 COMPUTER SYSTEM SOFTWARE ARCHITECTURE

Essentially all of the SLC software development is performed through the use of the VAX. Wherever possible, FORTRAN 77 is used for applications programming in both the VAX and the μ -processor clusters. FORTRAN 77 was chosen as the standard language because of its extensive support in the VAX, and because it is the most universally understood language. Although alternative languages could be used for the μ -processors, the consistency provided by standardizing on FORTRAN 77 has

Module Name (acronym)	Source	Approximate No. of modules to be used in the system	Description	Use
Serial Crate Controller (SCC)	SLAC	250	Serves as a CAMAC Crate Controller. Interfaces to a host computer via 2 RS-422 level signals on a twisted pair cable. An entire cycle, consisting of receiving a command, executing the CAMAC cycle, and responding, is performed in ~ 10 μ seconds. The bit data rate is 5 MHz. 16 controllers may be run from a single daisy-chained cable at distances in excess of 2000 feet with repeaters. (double-width).	Used as the Standard SLC Crate Controller.
Crate Verifier	SLAC	250	Contains command line spy register, independent function read and write register, LAM testing registers, and supply voltage and local temperature measurement capability. (single-width).	Used to verify proper crate and crate controller operation and aid in problem diagnosis.
Smart Analog Monitor (SAM)	Transiac Corp. or Standard Engineering Inc.	325	Provides 32 differential channels of μ -processor controlled digitization. Ranging, polarity selection, and self calibration are fully automatic. The module may be operated in the "slow" mode where each channel is integrated for one 60 Hz period (16.67 ms) or in a fast mode where each channel is digitized in 2 milliseconds. AC voltage is also read for each channel. All data is stored in a local memory and can be read asynchronously with the digitizing process. Accommodates full-scale inputs from 10 mV to 10.24 V and digitizes the signal with a resolution of 14 bits. The digitized value is presented in either VAX or IEEE floating print formats. The module may be interfaced to thermocouples by dedicating one of its input channels to a reference temperature thermister. In this mode the module can be programmed to provide the thermocouple junction temperature directly. (single-width).	Temperature monitoring of Linac waveguide. Monitoring of multi-channel "small" analog power supplies. Monitoring of miscellaneous analog reference signals.
Transiac DAC (DAC)	Transiac Corp.	275	Provide 16 channels of analog output with a full scale range of ± 10 V, a resolution of 16 bits, and a basic accuracy of .01%. (single-width).	Used to control multi-channel "small" power supplies and miscellaneous devices such as illumination for beam profile monitors.
Isolated Digital Input Module (IDIM)	SLAC	200	Contains 32 optically isolated non-latching digital input channels. (single-width).	Used for reading miscellaneous digital status information.
Isolated Digital Output Module (IDOM)	SLAC	100	Contains 32 channels of open-collector optically isolated digital output. Each channel may be programmed to latch its output data or to pulse high or low for a prescribed time period. (single-width).	Used for controlling digital devices such as beam screens, power supply on/off controls, etc.

Pulsed Power Output Module (PPOM)	SLAC	75	Provides a minus 24 volt output pulse with a nominal duration of 1/4 second to any one of 32 channels. (single-width).	Primarily used to replace the "Remote Control System" in the Linac.
Power Supply Controller (PSC)	SLAC	175	Provides a 14 bit analog output channel, a 14 bit analog input channel, digital input status bits, and 2 pulsed and 4 latched digital output bits. (single-width)	Primarily used to control and monitor "large" power supplies.
Programmable Delay Unit (PDU)	SLAC	175	Contains 16 channels of programmable pulse delay. Delay resolution is 8.4 ns and the delay is adjustable to 2.7 ms. The module is driven at its front panel by 476 MHz square wave with a missing pulse serving as the "start delay" fiducial. All outputs are provided to the CAMAC auxiliary backplane. (double-width).	Used to time modules and devices such as BPMs, PAUs, PIOPs, etc., which must be synchronised to the beam (see Ref. 9).
Single Timing Buffer (STB)	SLAC	175	Contains buffers to supply the 16 PDU channels to external destinations. Also contains a high-speed timer to measure delay of any channel for diagnostic purposes (single-width).	Used in conjunction with a PDU to verify its correct operation and to buffer its pulses.
Programmable Synchronization Unit (PSU)	SLAC	5	Provides a chain of "N" NIM level pulses of width W at pulse period of P after a delay D, where N, W, P and D are programmable in the module. The module is driven at its front panel by a 476 MHz square wave with a missing pulse serving as the "start delay" fiducial. (double-width).	Used to synchronize devices to the damping ring beam.
Programmable Width Unit (PWU)	SLAC	10	Receives 8 delayed triggers from the CAMAC upper backplane and provides output pulses with a programmed duration. (double-width).	Used in applications where programmed duration synchronization or gated pulses are required, such as gun triggers, etc.
Vernier Delay Unit (VDU)	SLAC	5	Provides 2 channels of Vernier delay for timing signals selected from the auxiliary backplane or from front panel connectors. The delay resolution is 1 nanosecond and the range is 10.5 nanoseconds (single-width).	Used in applications when the 8.2 nanosecond resolution to the PDU is not sufficient
Cable Access Transmitter (CAT)	SLAC	5	Transmits a 2 Megabaud SDLC bit stream on the CATV cable. 16 bit parallel data may be supplied from the CAMAC backplane or from a front panel connector. Used in conjunction with one or more Cable Access Receivers (CARs). Can be set to transmit on any of 5 CATV channels (triple-width).	See CAR usage below.

Cable Access Receiver (CAR)	SLAC	100	Demodulates a 2 Megabaud SDLC serial bit stream from the CATV cable and converts it to 16 bit parallel data words. These pass through a FIFO buffer and can be read from the CAMAC backplane or from a front panel connector. Used in conjunction with a Cable Access Transmitter (CAT). Can be set to receive on any one of 5 CATV channels. (triple-width).	Used in specialized point-to-point digital communications applications. One main use is in the Beam Pattern System where one CAT, driven by a μ -processor transmits beam related information at the accelerator cycle rate (360 Hz) to approximately 100 CARs which receive the information simultaneously and forward it to their related μ -processors. Also used in digital beam feedback loops.
Video Cable Access Module (VCAM)	Coherent Systems Inc.	25	Can be programmed to accept one of eight video (TV camera) inputs and place it on one of five possible CATV channels. The images may then be observed anywhere in the system using standard television receivers. (double-width).	Used to multiplex TV camera signals to operator control stations.
Parallel I/O Processor (PIOP)	SLAC	250	Contains an Intel 8088 processor which supports both RAM and EPROM memory. Has a general purpose interface to the CAMAC backplane and contains a front panel I/O port that supports a differential driver/receiver version of the 8088 I/O bus. It is designed to be used with special purpose "heads" which provide an interface to a device. Its program may reside in EPROM or may be downloaded from a VAX. Cross-compilers and network supported software exist to aid in the development process. (single-width).	Primary use to date has centered on the klystron control for the Linac. ¹⁰ Phase & Amplitude Detector (PAD) ¹¹ and Modulator Klystrons Control (MKII) heads have been developed to allow PIOP to monitor and control a klystron, its modulator and to measure its output phase and amplitude with respect to a stable reference. See Figure 3.
Beam Position Monitor (BPM)	SLAC	325	Provides 12 bits of resolution and 8 bits of attenuation control as well as a self-calibration mode to digitize fast (1 ns) bipolar pulses. (double-width).	Digitizes signals derived from beam position monitor striplines.
Beam Position Multiplexer (SP10T)	SLAC	325	Provides a single pole 10 throw (SP10T) switch for fast (1 ns) bipolar signals. (single-width).	Used to multiplex beam position monitor signals into the BPM modules in some applications.
Pulsed Amplitude Unit (PAU)	SLAC	25	Provides 32 "time-multiplexed" channels of pre-programmed analog amplitude. Receives timing information from CAMAC auxiliary backplanes and pattern information from the CAMAC backplane. (single-width).	Used for the control of devices such as pulsed magnets and phase shifters which must change state at the accelerator pulse rate (360 MHz).
Toroid Charge Monitor (TCM)	SLAC	15	Digitizes a signal generated by charge passing through a toroid with a nominal 1% accuracy.	Used to digitize beam current intensities.

been a great advantage for both the development and support of applications programs.

A significant effort has been expended by SLAC to create an efficient and user-friendly environment for the development of μ -processor software. In collaboration with the Intel Corp., FORTRAN 77 and PLM 86 cross-compilers, a cross-assembler, and a cross-linker have been developed to support the 8086/8088 series of μ -processors. Further, a symbolic debugger has been developed to allow the remote debugging of μ -processor based programs.

Applications tasks executed in the VAX are written as structured subroutines which are attached to a VAX process that provides interface routines to the operator console, and to a structured database. This process also provides a scheduling service for the subroutines.

The μ -processor clusters provide local control algorithms for the operation of the technical equipment. In general, the μ -processors receive an operational configuration in engineering units for their equipment from the VAX. They then ensure that the equipment is set to that configuration and only report back to the VAX when they are unable to achieve or maintain the desired configuration. The μ -processor clusters also provide monitoring information in engineering units to the VAX upon request and support a "pass-thru" mode for I/O commands from the VAX. The I/O commands may originate from a VAX applications process or from a system user via individual or a file of interpretive commands. The μ -processor systems will be used in the future to implement time-sensitive digital control loops.

3. Equipment Interfaces

In its completed state, the SLC control system will contain more than 250 CAMAC crates housing over 3200 CAMAC modules that provide I/O capability for nearly 50,000 signal points. Because of the size of these requirements, a significant development effort has been made to develop a comprehensive and flexible complement of CAMAC modules that serve to interface the SLC technical equipment to the computer system. Table 1 provides a listing and description of the interface modules used in the SLC system as well as typical applications.

4. Operational Experience

Although a portion of the control system has now been fully operational for a year, the project is still in its infancy and, as anyone who has been involved with a large system at this point in its evolution can appreciate, most of our current thoughts regarding the performance of the system relate to those items that must be improved. We are committed to the defining and implementing of improvement programs and have simply overlooked or forgotten to identify the many real successes of the system. With this thought in mind, we present the following list of observations regarding the performance of the system to date and generalize the successes of the system by stating that over the past year it has successfully supported the needs of accelerator physicists and machine operators in a series of very important and demanding operating experiments that have proven the viability of the SLC project.

- It is extremely important to be able to trace problems efficiently in the system's operating environment. Although an extensive effort has been applied to providing remote debugging tools and comprehensive diagnostics, significant

resources will continue to be directed to support these efforts.

- The number of simultaneous users of the system has been overwhelming at times. It is not unusual to have 5 COW's, 5-7 CALFS, and 2-3 program development terminals simultaneously active on a single VAX. Though current response-times for the system may be tolerable even under heavily loaded conditions with our current configuration, it is evident that we will have to do battle with a response-time problem as the system expands to its fully-implemented state.
- It is evident that the "information bandwidth" to the operator provided by a single COW as currently configured is not sufficient for efficient performance. This problem will probably have to be attacked by providing more devices (touchpanels, CRT's etc.) as well as increasing the performance of those devices.
- The system has been designed to support a diversity of operating and support personnel and it has been very successful in that regard. However, this success has developed into a tremendous need for user oriented software such that our relatively small software staff is greatly overloaded. In addition to continuing on a best efforts basis to provide this software, it is clear that more features and support are required to allow "casual" users programming access to the system so that they can write their own dedicated applications programs and have them supported in an integrated fashion.

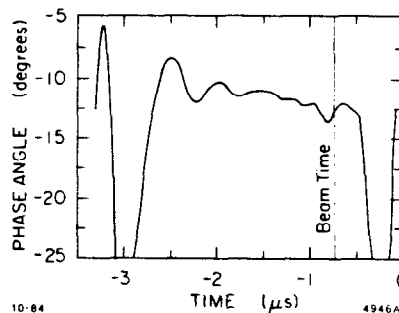


Fig. 3. A fast-time plot of the RF phase of a linac klystron pulse relative to a reference line and with respect to time. This plot was made using data supplied by a PIOP module (See Table 1) that collected the 64 data points on consecutive klystron pulses by adjusting a timing trigger delay to the phase detection digitizer on a pulse-to-pulse basis.

Acknowledgments

Over 100 people at SLAC have been involved with development and implementation of the SLC control system hardware and software, so individual acknowledgments are impossible. But I would like to take this opportunity to collectively thank all the people involved for their dedicated efforts in bringing the system to its current state and wish them the best of luck in their efforts to expand and improve it.

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