

THE VERNIER DELAY UNIT*

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Abstract

This module will accept differential ECL pulses from the auxiliary rear panel or NIM level pulses from the front panel. The pulses are produced at the output with a fixed delay that is software programmable in steps of 0.1 ns over the range of 0.1 to 10.5 ns. Multiple outputs are available at the front panel. Minimum delay through the module is 9 ns.

Introduction

One of the most critical timing specifications for the SLC machine occurs at the injector and ejector magnets for the Damping Ring. It has been determined that the trigger pulses to the magnets must be controlled to 0.1 ns. The primary source for all trigger pulses for the SLC machine is the Programmable Delay Unit (PDU). The PDU generates a 67.2 ns wide pulse with delay increments of 8.7 ns. The gap between the required accuracy and that available from the PDU requires the design of a new module that is called the Vernier Delay Unit (VDU). This module accepts the 67.2 ns pulse from the PDU and is capable of increasing the delay in steps of 0.1 ns from 0 to 10.7 ns plus the minimum 9 ns delay.

The module has two totally independent channels. The pulse input to the module is software selectable from either the auxiliary backplane or a front panel Lemo connector. The auxiliary backplane pulses are to be the 67 ns differential ECL pulses from the PDU. The front panel input is to be a NIM level (-0.7 V 50 Ω termination).

With the exception of the Pos 5 V signal, all output pulse widths will track the input pulse widths. The following outputs are available on the front panel:

1. Differential ECL
2. NIM level
3. Pos 5 V, 500 ns wide pulse

The delays for the two channels are independently software programmable over the range of 0 to 10.7 ns. The delay is achieved by utilizing the PECLDL Programmable Delay Lines that are available from Engineered Components Company of San Luis Obispo, California. Two units were used per channel: the PECLDL 2.8-0.1 and the PECLDL 2.8-0.6.

These delay lines are connected in series, and both are 4 bit programmable. The 2.8-0.6 model produces stepped delays in increments of 0.6 ns from 0 to 9.0 ns. The model 2.8-0.1 has increments of 0.1 ns and is programmable from 0 to 1.5 ns. Each unit presents a minimum of 2.8 ns delay. Added to this 5.6 ns delay is the VDU internal delay of approximately 3 ns, giving a minimum delay of approximately 9 ns. For all of the testing and calibration, this fixed delay is measured by programming 0 delay to the module and measuring the delay between input and output pulse. All subsequent delay measurements made during calibration and testing were corrected to present incremental delays that do not include this fixed value.

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The two programmable delays in series [0.6 ns and 0.1 ns] will have the condition that some delays which are to be requested could be requested by several different programs. For example: If we wish to request a delay of 1.5 ns, there are three possible choices:

0.6 Program		0.1 Program		Total Delay
1.	2 = 1.2	3 = 0.3	=	1.5 ns
2.	1 = 0.6	9 = 0.9	=	1.5 ns
3.	0 = 0	15 = 1.5	=	1.5 ns

```

Output 16 From CHANNEL 0
0 0000 0.000 0.110 0.000 0.295 0.377 0.476 0.078 0.663
0 0000 0.121 0.816 0.903 1.008 1.073 1.177 1.256 1.336
16 0010 0.121 0.816 0.718 0.821 0.919 1.026 1.127 1.221
16 0010 1.258 1.142 1.222 1.221 1.221 1.221 1.221 1.221
32 0020 1.067 1.180 1.174 1.262 1.433 1.559 1.670 1.775
40 0020 1.816 1.902 1.986 2.093 2.163 2.240 2.321 2.406
48 0030 1.639 1.774 1.868 1.967 2.067 2.167 2.262 2.363
64 0040 2.376 2.472 2.506 2.664 2.734 2.838 2.923 3.006
64 0040 2.577 2.670 2.560 2.679 2.791 2.891 2.974 3.063
72 0040 3.106 3.217 3.311 3.392 3.425 3.503 3.587 3.670
80 0050 2.965 3.062 3.160 3.277 3.367 3.450 3.518 3.592
96 0060 4.442 3.759 3.861 3.969 4.003 4.074 4.201 4.313
96 0060 4.584 3.692 3.807 3.919 4.017 4.110 4.202 4.309
104 0060 4.353 4.444 4.515 4.595 4.652 4.739 4.871 4.964
112 000 0 4.404 4.495 4.577 4.673 4.784 4.899 4.994 5.074
120 0070 5.106 5.205 5.301 5.398 5.448 5.531 5.607 5.699
128 0080 5.071 5.164 5.259 5.374 5.468 5.541 5.607 5.687
136 0090 5.745 5.866 5.978 6.075 6.125 6.226 6.330 6.444
144 0090 5.685 5.802 5.929 6.033 6.147 6.230 6.322 6.438
152 0090 6.483 6.577 6.651 6.735 6.799 6.914 7.026 7.122
160 00A0 6.327 6.460 6.504 6.639 6.713 6.805 6.902 7.017
168 00A0 7.082 7.177 7.264 7.366 7.442 7.536 7.634 7.710
176 00B0 6.877 7.010 7.121 7.224 7.314 7.420 7.516 7.611
184 00C0 7.459 7.741 7.821 7.929 8.011 8.124 8.209 8.293
192 00C0 7.436 7.552 7.643 7.730 7.818 7.922 8.033 8.144
200 00C0 8.197 8.291 8.381 8.490 8.545 8.653 8.731 8.805
208 00D0 8.069 8.128 8.224 8.312 8.405 8.508 8.607 8.686
216 00D0 8.737 8.824 8.916 9.016 9.117 9.226 9.312 9.401
224 00E0 8.627 8.714 8.789 8.867 8.999 9.128 9.227 9.312
232 00E0 9.373 9.470 9.569 9.669 9.725 9.805 9.892 9.973
240 00F0 9.170 9.275 9.364 9.467 9.568 9.665 9.743 9.816
248 00F0 9.877 9.977 10.070 10.209 10.277 10.369 10.444 10.522
                                FIXED DELAY (MIN/MAX) =
                                28.816
    
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Output 16 From CHANNEL 0
MOR PKDR MOR PKDR MOR PKDR MOR PKDR MOR PKDR
DLY ADDX DATA VAN DLY DLY CAN DATA
0 001F 00000 0.004 0.004 0.004 -0.001 000F 33 001C 0007A 0.001 5.301 5.280 0005
1 001E 00001 0.020 0.120 0.112 000E 34 001F 0007B 0.002 5.398 5.380 000A
2 001D 00002 0.004 0.204 0.197 000D 35 001C 0007C 0.031 5.531 5.525 000E
3 001C 00003 0.005 0.295 0.289 000C 36 001C 0007D 0.006 5.604 5.603 000E
4 001B 00004 0.023 0.377 0.370 000B 37 001C 0007E 0.001 5.699 5.699 000B
5 001A 00005 0.024 0.476 0.467 000A 38 001C 00091 0.005 5.805 5.781 000A
6 001F 00011 0.016 0.616 0.608 000E 39 001C 00092 0.029 5.929 5.909 000A
7 001B 00007 0.017 0.683 0.675 000B 40 001C 00084 0.022 5.978 5.972 000E
8 001F 00009 0.016 0.816 0.801 000F 41 001C 00085 0.025 6.075 6.066 000E
9 001F 0000A 0.063 0.903 0.898 000F 42 001C 00086 0.024 6.224 6.222 000E
10 001E 00005 0.008 1.008 1.004 000E 43 001C 00094 0.022 6.422 6.403 000A
11 001A 0000C 0.027 1.073 1.064 000F 44 001F 0007F 0.036 6.436 6.413 000B
12 001E 00021 0.020 1.180 1.173 000E 45 001B 00098 0.017 6.493 6.473 000F
13 001A 00022 0.026 1.274 1.264 000D 46 001B 00099 0.023 6.577 6.572 000A
14 001A 00014 0.022 1.422 1.409 000E 47 001C 00044 0.013 6.713 6.705 000E
15 001F 00019 0.021 1.521 1.514 000E 48 001B 0009C 0.001 6.799 6.804 000E
16 001F 0001C 0.008 1.592 1.585 000E 49 001B 00046 0.005 6.905 6.895 000A
17 001C 00010 0.007 1.707 1.705 000E 50 001B 00081 0.010 7.010 7.008 000E
18 001C 00011 0.004 1.804 1.795 000E 51 001B 00048 0.018 7.082 7.080 000E
19 001C 00029 0.002 1.902 1.890 000A 52 001F 0004F 0.023 7.177 7.173 000A
20 001A 0002A 0.014 1.984 1.973 000D 53 001B 00044 0.014 7.314 7.301 000A
21 001A 0002B 0.007 2.093 2.084 000A 54 001C 0005C 0.020 7.420 7.412 000A
22 001F 00035 0.013 2.187 2.174 000A 55 001B 00054 0.016 7.516 7.507 000A
23 001B 00036 0.018 2.282 2.267 000F 56 001B 0005F 0.011 7.611 7.602 000A
24 001F 00038 0.005 2.398 2.378 000F 57 001B 0004E 0.010 7.710 7.715 000E
25 001B 00039 0.028 2.472 2.459 000A 58 001B 0005C 0.018 7.819 7.815 000E
26 001B 0004C 0.040 2.540 2.533 000D 59 001B 0005E 0.022 7.922 7.924 000A
27 001A 0004J 0.021 2.679 2.672 000C 60 001A 0000E 0.329 8.000 8.000 000E
28 001C 00044 0.009 2.791 2.787 000B 61 001A 0008U 0.024 8.124 8.126 000E
29 001C 00045 0.009 2.891 2.889 000A 62 001C 0002C 0.003 8.197 8.213 000E
30 001C 00034 0.006 3.006 3.004 000C 63 001A 0000F 0.007 8.293 8.294 000A
31 001C 00048 0.004 3.106 3.086 000F 64 001B 00054 0.005 8.405 8.403 000A
32 001B 00049 0.017 3.217 3.197 000A 65 001A 0000G 0.008 8.506 8.511 000A
33 001B 00050 0.004 3.311 3.291 000A 66 001F 00056 0.005 8.607 8.602 000A
34 001B 00048 0.008 3.392 3.371 000A 67 001B 0001E 0.014 8.696 8.689 000E
35 001C 00040 0.003 3.503 3.493 000E 68 001A 0000C 0.005 8.805 8.803 000E
36 001B 00057 0.008 3.592 3.579 000A 69 001A 00043 0.015 8.857 8.867 000E
37 001A 00061 0.008 3.692 3.675 000E 70 001A 00054 0.004 8.999 9.004 000E
38 001B 00062 0.007 3.807 3.794 000E 91 001A 0005F 0.017 9.117 9.119 000E
39 001B 00063 0.019 3.919 3.908 000E 92 001A 0001E 0.026 9.226 9.225 000E
40 001F 0005C 4.441 4.400 4.391 000A 93 001A 0000E 0.012 9.312 9.314 000E
41 001C 00055 0.004 4.094 4.092 000E 94 001A 0000F 0.005 9.403 9.409 000E
42 001C 00054 0.001 4.201 4.197 000A 95 001A 00059 0.030 9.470 9.466 000E
43 001A 0005P 0.003 4.303 4.304 000A 96 001F 0001E 0.031 9.569 9.567 000E
44 001B 00070 0.004 4.404 4.392 000E 97 001A 0000C 0.025 9.725 9.733 000E
45 001C 00071 0.005 4.495 4.487 000E 98 001B 0000E 0.002 9.805 9.813 000E
46 001A 00069 0.005 4.595 4.587 000A 99 001C 0000E 0.008 9.892 9.881 000E
47 001B 00073 0.007 4.673 4.650 000C 100 001B 0000E 0.013 9.977 9.985 000E
48 001C 00074 0.016 4.784 4.783 000F 101 001A 0000E 0.010 10.000 10.000 000E
49 001C 00075 0.001 4.899 4.884 000A 102 001A 0000F 0.005 10.209 10.211 000A
50 001C 00076 0.004 4.994 4.974 000E 103 001E 0000E 0.023 10.277 10.273 000E
51 001C 00078 0.006 5.106 5.091 000E 104 001F 0001E 0.031 10.369 10.374 000E
52 001C 00079 0.005 5.205 5.189 000A 105 001E 0000E 0.006 10.444 10.444 000E
    
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Fig. 1. FROM Programming

In theory any of these programs should produce the requested delay. In practice we are looking for the best fit to the ideal requested value. In the example, that value would be 1.500 ns. Another requirement is that the value of the incremental delay increase monotonically as the requested delay is increased. To obtain the addresses for a best fit, a computer program was written that cycles through all possible delay address combinations, measures and records the delay, and address, and stores these values in RAM. The computer then looks for the best fit to the ideal curve. When it finds this best fit, it prints out the ideal value, address of the closest available delay, and does a second measurement of the delay and prints this value.

At the completion of this program, the printout will contain the delay addresses that will produce the most linear monotonically increasing delay. These delay addresses are stored in a PROM that is addressed by the software requested delay. The PROM is acting as a program director, insuring best fit of the requested delay.

The computer printout is shown in Fig. 1 for the programming of a specific PROM. Each of the units will have a unique PROM program. The upper portion of the printout lists the delay at each address. The lower portion shows how to program the PROM to get the best fit available.

The result of a final test of the module is shown in Fig. 2. The PROM has been programmed and the module is functional and ready for delivery. Fig. 3 is a system diagram, Fig. 4 is a VDU-1 channel block diagram and Fig. 5 is a schematic of the module.

OUTPUT IS FROM CHANNEL 0	DELTA-ERR	TOTAL-ERR	FIXED-DELAY (ns)
0 0.000 0.000 -0.160 0.000	33 3.300 5.342 -1.756e-6 0.042		
1 0.100 0.108 0.008 0.006	34 4.400 5.444 0.002 0.044		
2 0.200 0.210 0.002 0.010	35 5.500 5.585 0.041 0.085		
3 0.300 0.330 0.020 0.030	36 6.600 5.675 -0.010 0.075		
4 0.400 0.421 -0.009 0.021	37 5.700 5.752 -0.020 0.055		
5 0.500 0.507 -0.014 0.007	38 5.800 5.822 -0.030 0.022		
6 0.600 0.633 -0.004 0.003	39 5.900 5.922 -0.003 0.022		
7 0.700 0.680 -0.026 -0.035	40 6.000 5.975 -0.043 -0.021		
8 0.800 0.832 0.067 0.032	41 6.100 6.070 -0.009 -0.030		
9 0.900 0.936 -0.002 0.030	42 6.200 6.232 0.065 0.035		
10 1.000 1.040 0.040 0.040	43 6.300 6.342 0.007 0.042		
11 1.100 1.111 -0.029 0.011	44 6.400 6.421 0.009 0.051		
12 1.200 1.172 -0.039 -0.028	45 6.500 6.501 -0.050 0.001		
13 1.300 1.284 0.010 -0.018	46 6.600 6.608 0.007 0.008		
14 1.400 1.438 0.102 0.084	47 6.700 6.792 0.082 0.090		
15 1.500 1.582 -0.002 0.082	48 6.800 6.822 -0.038 0.052		
16 1.600 1.645 -0.047 0.045	49 6.900 6.941 0.009 0.061		
17 1.700 1.737 -0.008 0.037	50 7.000 7.023 -0.038 0.023		
18 1.800 1.822 -0.015 0.022	51 7.100 7.060 -0.063 -0.040		
19 1.900 1.936 0.014 0.036	52 7.200 7.132 -0.005 -0.045		
20 2.000 2.030 -0.006 0.030	53 7.300 7.329 0.074 0.029		
21 2.100 2.132 0.005 0.035	54 7.400 7.444 0.015 0.044		
22 2.200 2.171 -0.064 -0.029	55 7.500 7.543 0.001 0.045		
23 2.300 2.273 0.002 -0.027	56 7.600 7.631 -0.014 0.031		
24 2.400 2.448 0.075 0.048	57 7.700 7.728 -0.063 0.028		
25 2.500 2.547 -0.001 0.047	58 7.800 7.883 0.025 0.083		
26 2.600 2.586 -0.061 -0.014	59 7.900 7.971 -0.012 0.071		
27 2.700 2.680 -0.006 -0.020	60 8.000 8.026 -0.045 0.026		
28 2.800 2.768 -0.012 -0.032	61 8.100 8.081 -0.045 -0.019		
29 2.900 2.874 0.006 -0.026	62 8.200 8.163 -0.018 -0.037		
30 3.000 3.041 0.067 0.041	63 8.300 8.284 0.001 -0.036		
31 3.100 3.114 -0.007 0.034	64 8.400 8.417 0.025 0.017		
32 3.200 3.237 0.063 0.037	65 8.500 8.518 0.001 0.016		
33 3.300 3.336 -0.001 0.036	66 8.600 8.606 -0.012 0.004		
34 3.400 3.437 0.001 0.037	67 8.700 8.702 -0.004 0.002		
35 3.500 3.529 0.002 0.039	68 8.800 8.835 0.033 0.035		
36 3.600 3.623 -0.036 0.023	69 8.900 8.941 0.006 0.041		
37 3.700 3.704 -0.049 0.004	70 9.000 9.024 -0.017 0.024		
38 3.800 3.796 -0.008 -0.004	71 9.100 9.080 -0.044 -0.020		
39 3.900 3.912 0.016 0.012	72 9.200 9.174 -0.006 -0.026		
40 4.000 4.021 0.009 0.021	73 9.300 9.262 -0.009 -0.035		
41 4.100 4.124 0.003 0.024	74 9.400 9.362 -0.003 -0.038		
42 4.200 4.225 0.001 0.025	75 9.500 9.452 -0.010 -0.046		
43 4.300 4.312 -0.010 0.012	76 9.600 9.548 -0.004 -0.052		
44 4.400 4.380 -0.035 -0.020	77 9.700 9.727 0.079 0.027		
45 4.500 4.507 0.027 0.007	78 9.800 9.832 0.008 0.032		
46 4.600 4.680 0.073 0.080	79 9.900 9.922 -0.013 0.022		
47 4.700 4.769 -0.071 0.009	80 10.000 10.004 -0.015 0.004		
48 4.800 4.796 -0.013 -0.004	81 10.100 10.077 -0.027 -0.023		
49 4.900 4.896 -1.756e-6 -0.004	82 10.200 10.165 -0.012 -0.035		
50 5.000 4.983 -0.013 -0.017	83 10.300 10.227 -0.038 -0.073		
51 5.100 5.135 0.052 0.035	84 10.400 10.324 -0.003 -0.076		
52 5.200 5.242 0.007 0.042	85 10.500 10.416 -0.008 -0.084		

Fig. 2. Final Test Printout

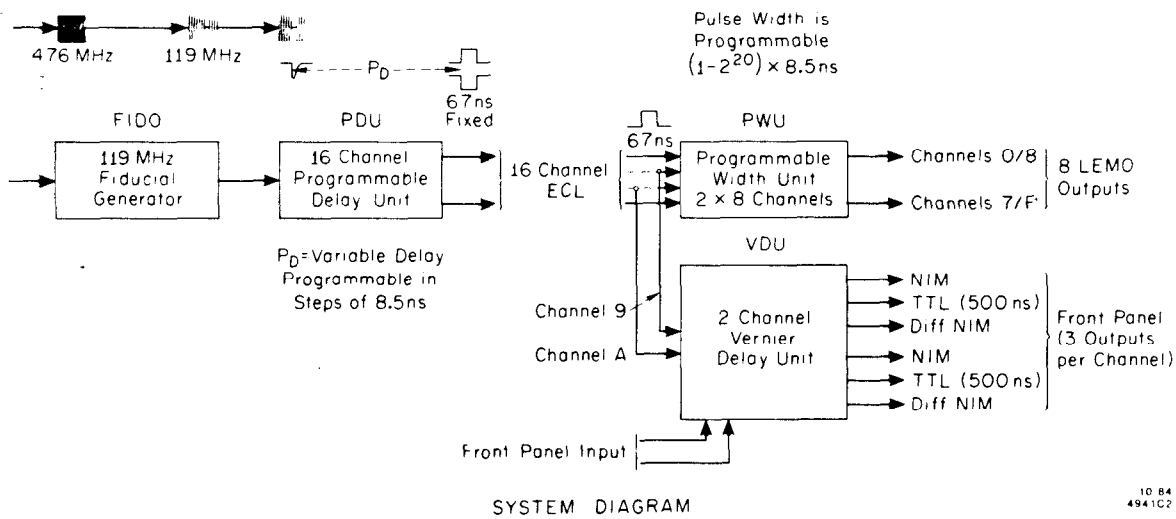
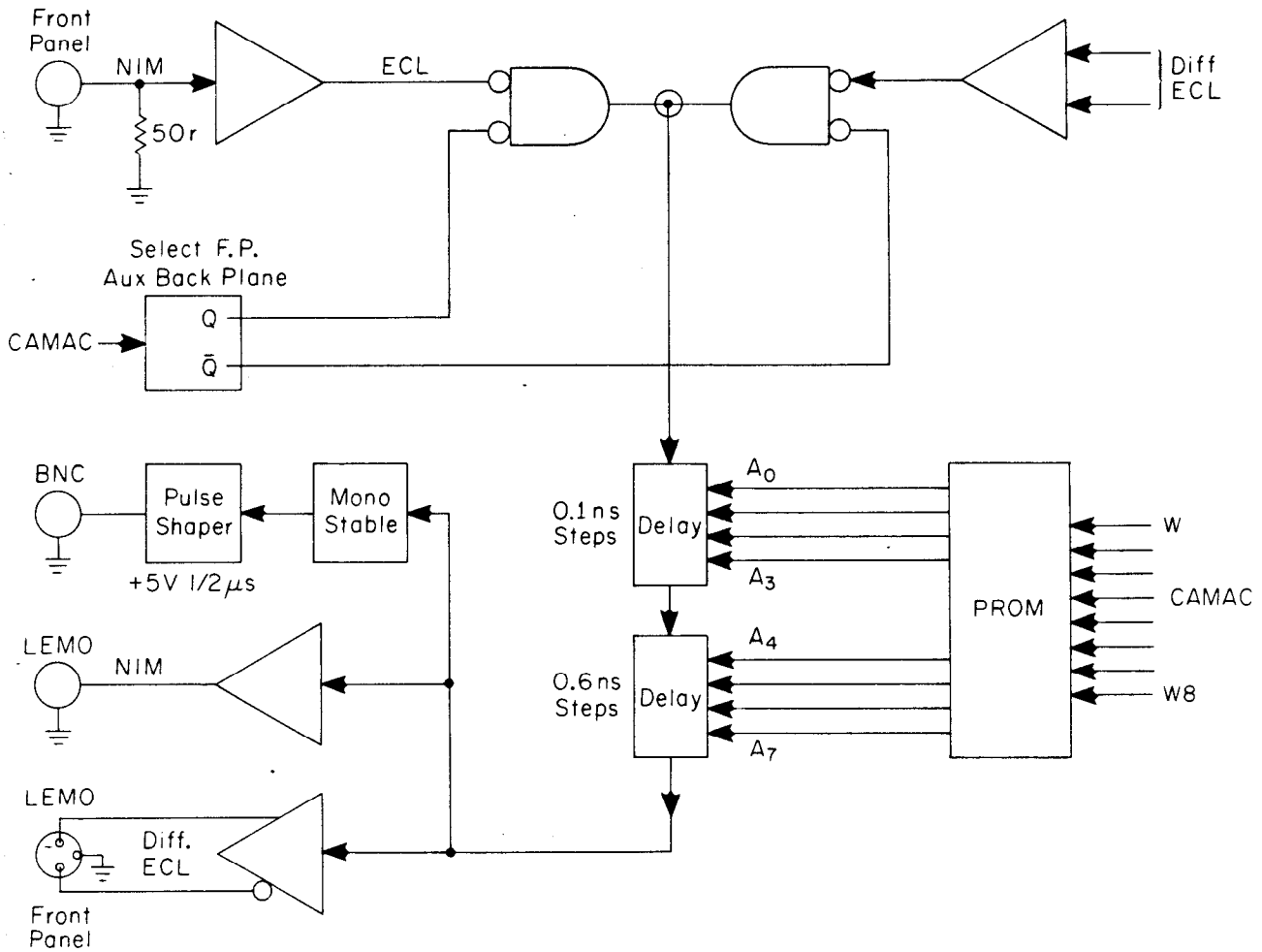


Fig. 3. System Diagram



10 84

VDU-1 CHANNEL BLOCK DIAGRAM

4941B1

Fig. 4. VDU-1 Channel Block Diagram

The following discussion refers to Fig. 5 [Schematic Drawing DS-135-756-01-R2], and is an effort to describe the circuit function of the chips utilized. U14, U17 are ECL line receivers that present proper terminations to the driving circuits. U16 and U15 are ECL gates that ultimately determine which condition is selected, i.e., rear panel, front panel or channel disabled. U11 and U12 are the programmable TTL registers that dictate which condition the gates will be in. (Again: front/rear panel select or disable) U18, 19, 20, 21 are the ECL programmable delays. U19, 21 are programmable delays of 15 steps of 0.1 ns per step. U18, 20 are programmable in 15 steps of 0.6 ns per step.)

U22, 24 are ECL line drivers that condition the output signal to the desired levels. U23 and U25 are ECL monostables that generate the fixed 500 ns output pulse width and Q4, Q5 and Q6, Q7 are discrete transistors that generate the +5 V amplitude of this 500 ns pulse. U1, U2 are latches that hold the requested delay that is on the CAMAC write lines. U7, U8 are PROMs that are programmed to get the optimum incremental delay response. U3, U4, U5 are TTL circuits used to read back the information as to what delay has been programmed into the circuit. U3 and U4 act as a multiplexer selecting between Ch1 and 0. U5 is the CAMAC READ line driver. U13 is the "n" light driver.

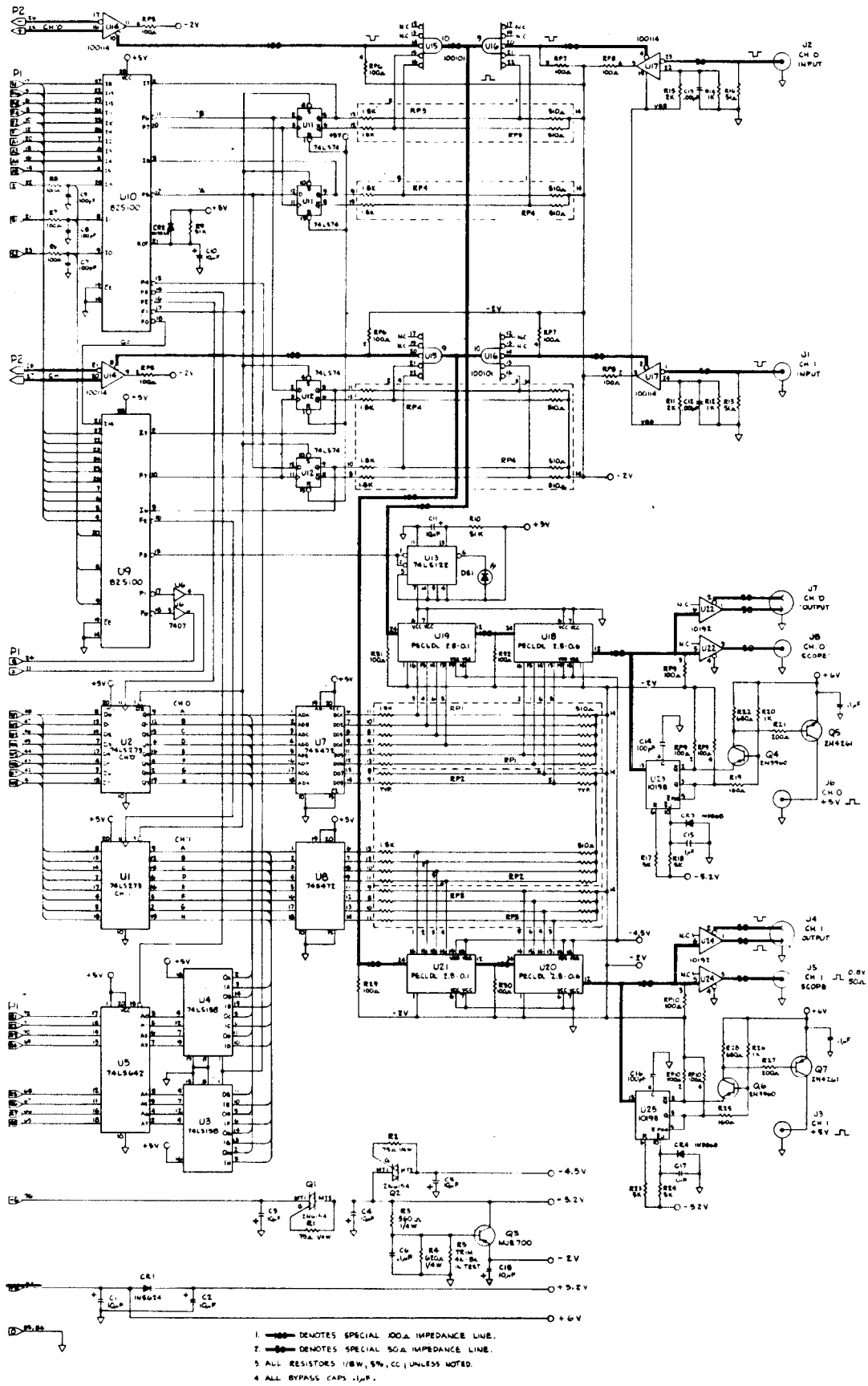


Fig. 5. Module Schematic

The VDU module is a single width CAMAC module. Figure 6 is a photo of the module.

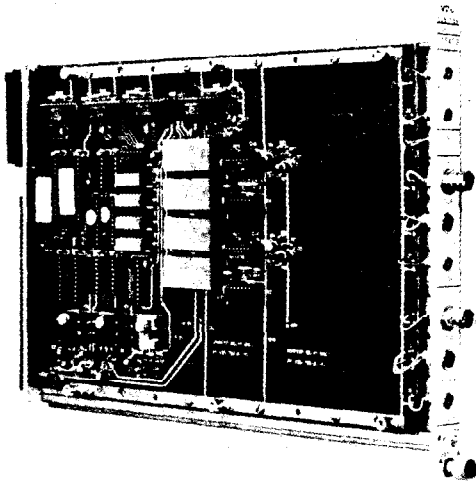


Fig. 6. VDU Module

The CAMAC commands utilized for this module are as follows:

CAMAC CODES

- Power On, $F9 \cdot AX \cdot S2$, $Z \cdot S2$ will disable all outputs and clear all channels.
- $F0 A0/A1$: Read the contents of the delay register. $Q=1$ implies that the auxiliary backplane is selected AND channel (0/1) is enabled.
- $F1 A0/A1$: Read the contents of the delay register. $Q=1$ implies that the front panel is selected AND channel (0-1) is enabled.
- $F10 A0/A1$: Disable channel (0/1).
- $F16 A0/A1$: WRITE $W1-W7$ into channel 0 or 1, in straight binary. This command also selects the auxiliary backplane, and enables the output.
- $F17 A0/A1$: Same as $F16 A(0/1)$ except that the inputs are selected from the front panel.
- $F25 A0/A1$: Enable channel (0/1). Enable rear panel input.
- $F26 A0/A1$: Enable channel (0/1). Enable front panel input.
- $F27 A0/A1$: $Q=1$ implies that channel (0/1) is enabled.