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PROGRAMMABLE SYNCHRONIZATION UNIT*

H. Kang
Stanford Linear Accelerator Center
Stanford University
Stanford, California 94305

Abstract

A Programmable Synchronization Unit (PSU, 135–726) has been designed as an element of the new timing system for the Stanford Linear Collider (SLC) project to provide synchronization signals needed for various apparatus in the SLC Damping Ring, or anywhere it is necessary to monitor longer than the fiducial period ($\simeq 2.8\ \mu s$). A 119 MHz pulse train derived from the 476 MHz main drive line and superimposed with 360 Hz fiducial signal is the frequency source. Following a programmable delay D of up to 4.4 μs, the PSU can deliver N pulses of width W (in increments of 8.4 ns) with a pulse period of P (in increments of 58.8 ns, the damping ring half period). The device may be programmed at any time during the interfiducial period.

Introduction

In the SLAC Linear Collider operation, electron and positron beams which have been produced in the linac are stored for a time ($5 \rightarrow 10\ \mu s$) in two circular damping rings until the beams have been reduced in size. The Programmable Synchronization Unit (PSU) has been primarily designed for various synchronization functions at the damping ring, such as to be able to follow a beam bunch or to sample it at any time. Up to now, it has been in use to trigger the beam position monitors positioned along the damping ring by a single output pulse and the fast CCD cameras by a successive output bunch. (See Fig. 1, PSU Application Diagram) The module is a double width CAMAC module with a four-layer PC board. (See Fig. 2, PSU Photograph.)

Functional Description

The input to the PSU is a train of pulses at 119 MHz with a 360 Hz fiducial signal indicated by a missing pulse derived from the fiducial detector (SLAC 135–724). The fiducial is detected by means of a retriggerable one-shot, which generates a single pulse ($\simeq$ 8.4 ns width) at the fiducial time. (See Fig. 3, PSU Block diagram.)

The data on the number of output pulses (N), interpulse period (P), output pulse width (W) and the output delay (D) from the fiducial can be loaded into transfer registers at any time during the interfiducial period. These operations also set an internal programmed flag.

Upon receipt of the next fiducial, a series of operations is initiated: The D output-control is enabled and the contents of the D program registers are loaded into the D counter. The BUSY output which is a fiducial inhibit is set. (See Fig. 4, PSU Timing Diagram.) The clock pulse path to the counters is enabled. The delay counting is initiated. At the end of the D counting, a look-ahead circuit associated with the D (P) counter generates a pulse (4.2 ns width) which simultaneously loads both the period (P) data into the P counter and width (W) data into the W counter. Now, both P and W counters start counting.

The half period of the damping ring (Tdr) is 58.8 ns. Therefore, a separate divide-by-seven counter associated with P counting is required so that the P counting advances in increments of seven clock pulses (58.8 ns). If $N > 1$, a pulse is generated at the end of the P counting through the same look-ahead logic, parallel loading again both P and W counters.

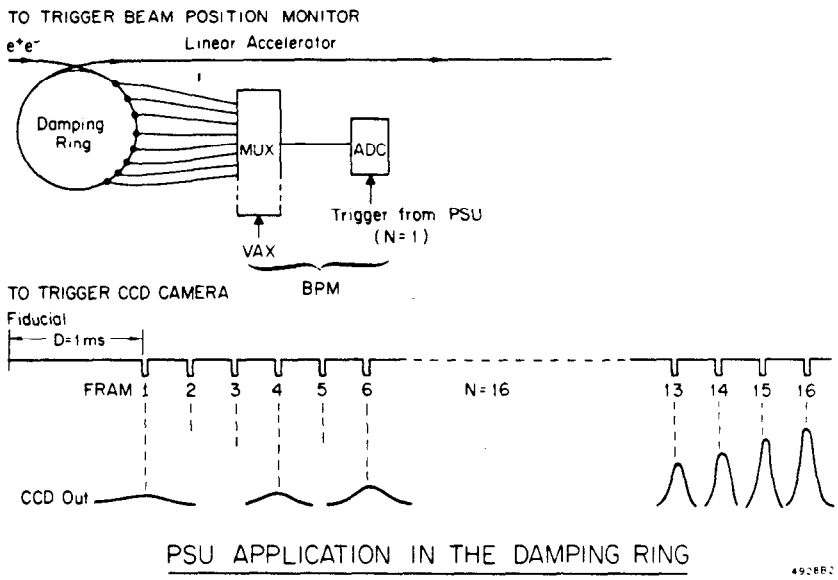

Fig. 1. PSU Application Diagram

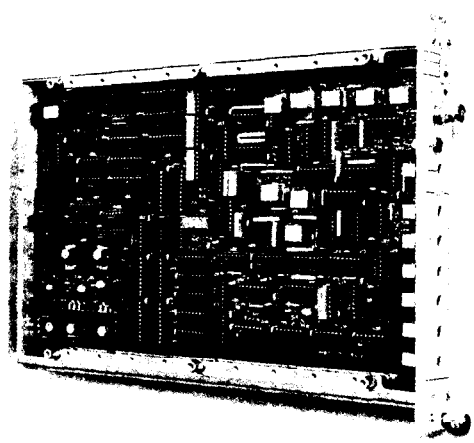

Fig. 2. PSU Photograph

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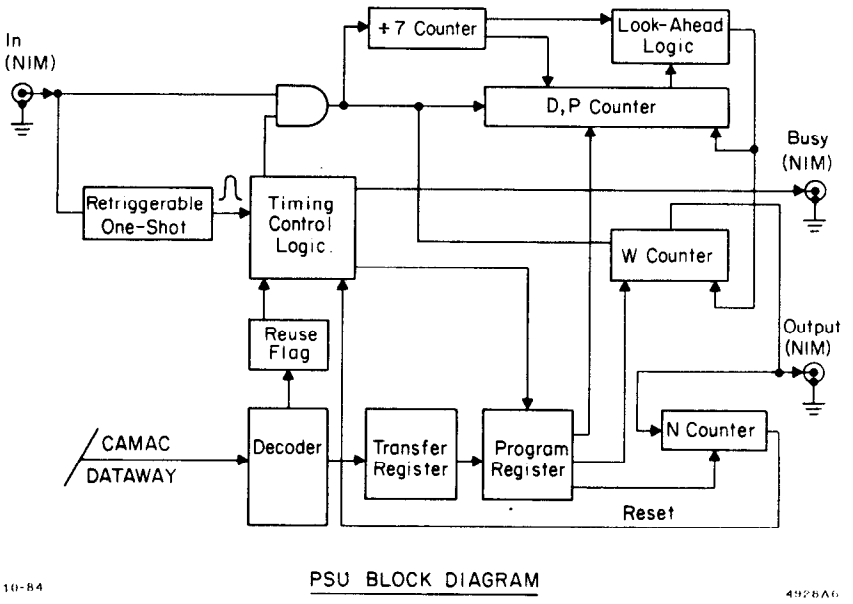

Fig. 3. PSU Block Diagram

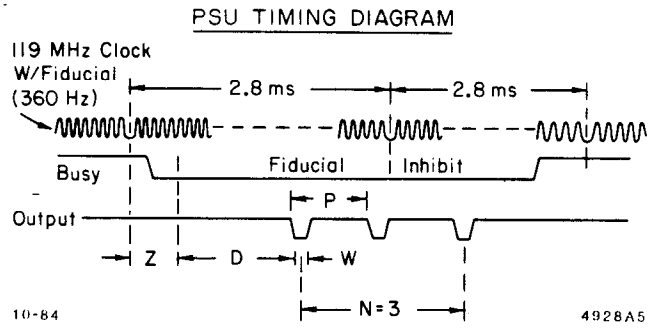

Fig. 4. PSU Timing Diagram

The output of the module is extracted from the W counter and is level translated into NIM. The output from the W counter also serves as the clock to the N counter. At the end of the N counting, a RESET pulse is generated, which resets all the counters and registers including the BUSY flag. The total operation time span from the fiducial reference to the BUSY flag reset is given by

$$[\, Z + D \cdot \Delta + (N-1) \cdot P \cdot Tdr + W \cdot \Delta \,] \text{ (ns)}$$

where

Z = initial delay time (constant)

Δ = 8.4 ns (119 MHz)

Tdr = 5.8.8 ns (half period of the damping ring)

The next fiducial repeats another operation cycle if the REUSE flag is set. There is a special case where the current operation continues indefinitely if the infinity bit is set (W_{21} = "1"). In this case, the operation can only be terminated by either resetting W_{21} or by a CLEAR command.

To save the power consumption of the module, TTL (LS) logic is implemented wherever the speed is less critical. All the TTL to ECL level translation was implemented by the resistor divider networks.

Specifications

Number of Channels	1
Input Clock (from FIDO)	NIM level at 119 MHz
Input (Fiducial)	Missing pulse of 119 MHz Clock at 360 Hz
Delay Range (Fiducial to output)	8.4 ns to 4.4 ms
Output Signals (6)	NIM pulse train, $4V_0$, $2V_0$ D = pulse delay P = pulse spacing at 58.8 ns increments N = Number of pulses W = Width of pulses in 8.4 ns increments
Range of D	$1 \le D < 2^{19}$ Δ = 8.4 ns step
Range of P	$1 \le P < 2^{12}$ T_{dr} = 58.8 ns
Range of N	$1 \le N \le 10^6$ or special case $N = \infty$
Range of W	$1 \le W \le 2^8$
CAMAC Codes	
Write N	F(16)A(2)S1 (W1 thru W21)
Write P	F(16)A(1)S1 (W1 thru W12)
Write D	F(16)A(0)S1 (W1 thru W19)
Write W	F(16)A(3)S1 (W1 thru W8)
SET REUSE	F(16)A(4) W1S1
CLEAR REUSE	F(16)A(4) $\overline{\text{W1S1}}$
RESET	F(9)A(0)S2 or PW/ON
$Q = X = 1$	VALID COMMAND
Busy Output (to FIDO)	NIM, differential signal
Busy Output (for test)	NIM
Jitter	±250 ps max
Delay Resolution	8.4 ns

Pulse-to-Pulse Resolution	
within *N*	±250 ps max
Front Panel Indications	
X	LED
REUSE	LED
Power Supply Requirements	
+6V at 1A	CAMAC Power Supply (P1-84)
−6V at 2.9A	CAMAC Power Supply (P1-76) and CAMAC Power Supply (P1-79)
Module	CAMAC Double Width
Temperature	0 to 60 °C operating with/≥ 500 fpm airflow
Delay drift	< 0.5 ns at 0 – 60 °C

Conclusion

The design and implementation of the PSU has met or exceeded the specifications required. In particular, jitter in over 60 °F environment was found to be less than 250 ps. The PSU has been in use for about twelve months in the damping ring. Recently, the maximum period of 2^{12} (0.24 μs) has been extended to 2^{16} (3.85 μs) to meet an extended functional feature in the damping ring.