SLAC-PUB-3450
September, 1984
(I)

AUDIOFREQUENCY MEASUREMENT OF JFET NOISE VS. TEMPERATURE IN A HIGH IMPEDANCE PREAMPLIFIER*

SPENCER KLEIN, WALTER INNES, JOHN C. PRICE

Stanford Linear Accelerator Center
Stanford University, Stanford, CA, 94305

Abstract

We describe a high impedance audiofrequency preamplifier and present audiofrequency noise spectra for 2N4416 and U311 JFET's, in a temperature range from room temperature to 80^0K. It is found that optimum noise performance is obtained at -140^oK. We present an analysis of some of the sources of noise. Amplifier input capacitance is also measured and discussed.

Submitted to Review of Scientific Instruments

---

* Work supported by the Department of Energy, contract DE-AC03-76SF00515

1. Introduction

To search for fractional charges by direct charge measurement using Gauss' law requires a low noise, high impedance preamplifier.[1-2] Such an apparatus produces a voltage $V = Q/C_{tot}$, where C_{tot} is the apparatus plus amplifier capacitance. For our apparatus, the signal frequency is 8 KHz and C_{app}, the apparatus capacitance is 20 pF. The signal to noise ratio is $S/N \propto 1/C_{tot}N_{tot}$, where N_{tot} is the amplifier plus apparatus noise expressed as a voltage referred to the input.

For this type of application, a silicon JFET is the best choise for the input stage. Bipolar transistors have too low an input impedance, and too high a current noise. MOSFET's and GaAs JFET's have too high a voltage noise.

2. JFET Noise Sources

A JFET has several noise mechanisms. They include thermal noise from the channel resistance, shot noise from gate leakage current, generation-recombination noise from electron-hole pair creation and annihilation, dielectric loss noise from the FET header, and others. These noise sources may be conveniently divided into voltage noises and current noises. Figure 1 gives a circuit model for the following discussion.

The thermal current fluctuations in the channel may be represented by a voltage source at the input, given by:

$$e_n = \sqrt{4kT\alpha/g_{fs}} \tag{1}$$

where α is a constant, about 0.7, and g_{fs} is the forward transconductance.[3] It has been reported that below room temperature α rises due to increasing carrier mobility.[4] The channel noise spectrum is flat at audiofrequencies.

These channel current fluctuations also capacitively couple to the gate, producing a current noise which is partly correlated with e_n. Since the effect is fairly small, and the correlation is small (40%), the correlation can be neglected. It is

given by:[5]

$$i_{ccr} = \frac{3}{8} e_n \omega C_{gs} \tag{2}$$

Total generation-recombination (g-r) noise, e_{gr} is a sum of noise from different trapping impurities. These trap noises sum to give a roughly $1/f^a$ voltage noise spectra, where $a \approx 1 - 2$.[6] It has been reported that as FET's are cooled, the total g-r noise remains the same, but its spectrum shifts to lower frequencies.[7] Since g-r noise is impurity dependent, it varies greatly from device to device.

The leakage current shot noise is given by:

$$i_s = \sqrt{2qI_l} \tag{3}$$

where I_l is the gate leakage current, and q is the electron charge.[8] It is easy to eliminate this by cooling the FET, since leakage current decreases exponentially with temperature, roughly halving for a $10^0 C$ temperature drop.[7]

Another source of current noise is the dielectric on which the FET chip is mounted. This dielectric produces a current noise equivalent to a resistor with resistance equal to the real part of its impedance, i.e.

$$i_{die} = \sqrt{4kT\omega C_{die} \tan\delta}\,. \tag{4}$$

where $\tan\delta$ is the loss factor of the capacitor and C_{die} is the header capacitance, typically .3 pF. For borosilicate glass, the usual FET header material, $\tan\delta \approx$ .003.

Since they are uncorrelated, these noise sources add in quadrature to give the total noise:

$$e_{tot} = \sqrt{e_n^2 + e_{gr}^2 + (i_{ccr}/\omega C_{tot})^2 + (i_s/\omega C_{tot})^2 + (i_{die}/\omega C_{tot})^2} \tag{5}$$

It is possible to measure the voltage noises directly by measuring the noise with the gate grounded, setting C equal to infinity. The current noise must be measured indirectly, by measuring the total noise with a small, low noise, capacitor

connected to the gate, and quadrature subtracting the voltage noise. This procedure introduces large errors if the current noise is small. Since the frequency independent shot noise is divided by ωC_{tot}, it appears as a 1/f contribution to the total noise, in contrast to the channel noise which is generally flat.

Since our amplifier (described in Section 3) has ample feedback, the source voltage follows the gate voltage closely. So, essentially all of e_n is fed back and appears at the source. This extra e_n is divided by the voltage divider C_{gs} and C_{app} paralleled with C_{gd} (since the drain is a virtual ground) and appears between the gate and the source. This effectively increases e_n by:

$$e_{eff} = e_n(1 + \frac{C_{gs}}{C_{app} + C_{gd}}) \tag{6}$$

where e_{eff} is the voltage noise contribution to total noise. e_{gr}, also a voltage noise, increases by the same factor. For a 2N4416, C_{gs} is 3.2 pF, so e_n will increase by 20% for $C_{app} = 20pF$. This noise increase matches the decreased input capacitance, leaving the signal to noise ratio unchanged. When feedback is used, e_{eff} directly replaces e_n in equation 5.

Several different FET's were tried in the amplifier. They were the 2N4117A, 2N4220A, 2N4416, U310, U311, and J203. For 20 pF input capacitance, we found that a 2N4416 was the best choice. For a larger apparatus, a U311 might be better. Table I gives a summary of expected noise factors for these FET's.

3. The Circuit

The circuit is shown in Figure 2. It is a FET input cascode with a few unusual features. The closed loop gain is 1000, between -3dB points of 10 Hz and 170 Khz. To ensure that noise from the second stage is negligible, a low noise op amp (NE5534) and a low noise polystyrene coupling capacitor were used. A 23 - 47 volt low noise drain voltage power supply allows different FET's to be accomodated, as well as allowing compensation for the change in I_d as the FET's are cooled. The high voltage allows R_d to be chosen large enough so that the first stage gain $(A = g_{fs}/(1/R_d + 1/r_{ds}))$ is high enough so that noise from suceeding stages is

negligible. The FET output conductance, $1/r_{ds}$, sets an upper limit on the first stage gain. At the low drain voltage used ($V_d = 4V$), the output impedance r_{ds} is $2 - 6K\Omega$, depending on the particular FET. A high current, low voltage noise FET (2N6550) regulator keeps the power supply noise low ($< 5nV/\sqrt{Hz}$). The audio frequency noise of the second stage op amp is specified at $< 4nV/\sqrt{Hz}$. If the first stage gain is at least 10, the noise contributions from all sources other than the first stage are measured to be $< .8nV/\sqrt{Hz}$ referred to the input at 8 Khz.

The FET was installed in a vacuum box, mounted on its cooler. A Joule-Thompson micro-miniature refrigerator[9] provided the cooling. At 5μ vacuum, it could maintain any temperature between 78^0K and room temperature for a FET dissipation up to 100 mW.

4. Operating Parameters

The main adjustable parameter was V_d. Of course, varying V_d also changed I_d, with $\Delta I_d = \Delta V_d/r_{ds}$. $V_d = 4V$ was chosen as a standard operating point. At lower V_d's, r_{ds} was too small, and the FET was still in the ohmic region. At higher V_d's, the current noise increased significantly. $V_d = 4V$ gave 2N4416 I_d's of 6-11 ma, and U311 I_d's of 35-55 ma.

As expected, I_d increased as the FET cooled. It rose by about 50% as it was cooled to the optimum temperature, then decreased slightly. The decrease with further cooling can be explained by carrier freezout. Figure 3 shows the changes for a typical 2N4416. g_{fs} also increased with temperature, closely following I_d. As Figure 4 shows, it increased with temperature until about -140^oK, then began to drop.

The 2N4416 input capacitance was also measured, both with the feedback connected and disconneced. It was measured by applying a signal to the input through a known capacitor and measuring the attentuation. Depending on the particular 2N4416, it varied between 4.0 and 5.0 pf with no feedback, and 2.0-2.9 pf with feedback. The capacitance with feedback was significantly higher than

was expected, since the 2N4416 C_{gd} is specified as 0.8 pf,. while C_{gs} is specified as 3.2 pF.[10] With a small audio signal input, the AC voltage at the source was 95% of the gate voltage, and the AC drain voltage was about 5% of the gate voltage, with a negligible phase shift. This is as expected, since the drain is a virtual ground, and the source is heavily fed back. Therefore the input capacitance should be $1.05C_{gd} + .05C_{gs}$, or about 1 pf. Part of the discrepancy is because the specified figure is at $V_{ds} = 15V$, but at $V_{ds} = 4V$, C_{gd} should only rise to 1.2 pf.[11] The rest of the difference is at present not understood. The measured capacitance was independent of frequency below the op amp cutoff frequencies. The noise measurements discussed in Section 6 show that our noise data fits the model described in section 2 when the Siliconix capacitance figures are used, but not when our capacitances are used. This discrepancy is apparently a failure of the lumped element circuit model, possibly due the the effect of distributed capacitance along the channel.

The gate leakage current was measured also. The gate was grounded, and the drain current measured. Then the gate was connected to a voltage through a $10^{12}\Omega$ resistor. Then the voltage was varied until the FET returned to it's $V_g = 0$ drain current. The gate leakage current was found from Ohm's law. The 2N4416 leakage current ranged from 0.5-1.5 pA at $V_d = 4V$, and was roughly exponential in V_d, increasing roughly 50% per volt of V_d. Gate leakage current found at $V_g = 0$ gives a rough estimate of the leakage under actual operating conditions. The FET parameters are summarized in Table III.

5. Biasing

In charge sensitive JFET preamplifiers, several methods are used to bias the gate. They include large resistors,[12] optical feedback methods based on the photoelectric effect,[13] and transistorized switches.[14] However, all of them add either noise, capacitance, or dead time. In many cases, these schemes are necessitated by a D.C. current from the source. If there is no net D.C. current, it is simplest to let the gate float. While this does not eliminate the leakage current, since current can leak from the drain to the gate, then flow out the

source, it does simplify the circuit. At room temperature this worked extremely well; stray resistances were small enough to keep the gate biased firmly in one place. Measuring the change in drain current when the gate is grounded gives the gate voltage:

$$V_g = \Delta V_g = \frac{\Delta I_d}{g_{fs}} \approx +.2V \tag{7}$$

With higher current FET's, this method required that a close watch be kept on temperature, because it produced very large drain currents. Without adequate cooling, the larger FET's (U311's) would burn themselves out quickly.

When cold, except for 2N4416's made by Intersil, all the FET's biased themselves as at room temperature, although they sometimes took a few minutes to equilibrate if a charge was applied to the gate. Intersil 2N4416's were different. They could be set to a specified V_g by applying a voltage to the gate, and they would not drift from that point. Their internal resistance was high enough that the drift rate was negligible, less than $\Delta V_g/\Delta t < .01V/sec$. This locking to a specific point began at about 5^0C. However, no signiticant change in noise was observed when V_g was made slightly ($< .5$V) positive or negative.

6. Noise Measurements

Noise measurements were made on 16 2N4416 and 5 U311's. The more promising half of these devices were also measured cold. The following data is for 2N4416's unless otherwise specified, although the U311 data is qualitatively very similar.

Aside from a few notably bad devices, noise levels were quite similar from device to device. No star performers were found. About 3/4 of the devices examined had voltage noise levels within $\pm 25\%$ of each other. Current noise varied somewhat more, probably because leakage current varied by a factor of 3 from device to device.

A Wavetek 5820A spectrum analyzer was used to measure the noise in the 0-10 Khz range. All noise data was taken with the amplifier feedback connected

to maintain a constant gain, compensating for changes in g_{fs} with temperature.

Table II presents a summary of noise data. T_{opt}, the optimum low noise temperature, varied from device to device, but was in the -140^oC to -150^oC range. The total noise levels are somewhat higher than the theoretical predictions in Table I. For the voltage noise, the difference is probably due to the increase in α with cooling. The large variation in voltage noise levels is largely due to a few obviously poor devices. Neglecting them brings the average down significantly.

Representative spectra are presented in Figures 5-8. Figure 5 shows voltage noise and 20 pF total noise spectra at room temperature. Above 3 Khz the voltage noise spectrum is quite flat, indicating that g-r noise is negligible. The 20 pf spectrum is composed of roughly equal voltage noise and current noise contributions. Figure 6 shows the noise with the gate open.

Figure 7 shows the voltage noise at $T = -100^oC$. The spectrum is roughly 1/f, and is probably due to g-r noise. As most of the FET's were cooled, the voltage noise spectrum went from roughly flat, as in Figure 5, to 1/f as in Figure 7, then flattenned out with further cooling.The 1/f spectrum was visible from roughly -30^oC to -120^oC in most devices.

Figure 8 shows the typical voltage and 20 pf total noise from a 2N4416 at it's optimum temperature. The voltage noise spectra still shows a slight frequency dependence. At lower temperatures, this disappeared, but the flat spectrum voltage noise rose. Due to this tradeoff, T_{opt} is a function of frequency. The total noise spectrum is also quite flat, evidence that the leakage current noise has disappeared. However, the 20 pF noise is substantially higher than the gate grounded noise. A large part of this is due to the feedback arrangement.

To measure high frequency noise, 0-50 Khz spectra were also taken. Figure 9 shows one with 20 pF input capacitance. It levels out above 25 Khz at $2.6nV/\sqrt{Hz}$. This is higher than the $2.2nV/\sqrt{Hz}$ expected if our input capacitance measurements are used to calculate C_{gs} and C_{gd}; however it is consistent with noise expectations from feedback and correlated current noise if the Silconix C_{gs} and C_{gd} are used.

Several spectra were taken with small (2-5 pF) capacitors attached to the gate. At 40 Khz, the spectrum was relatively flat in all cases. The 40 Khz noise as a function of capacitance is shown in Figure 10. The curves are compatible with expectations from voltage noise (with the feedback effect discussed earlier) plus the current noises if the Silconix capacitance figures are used, but not with our capacitance measurements.

Finally, the 40 Khz gate open noise was measured as a function of temperature. It tracked the gate grounded voltage noise closely, showing a slight hump at -50^0C, decreasing to 80% of it's room temperature value near T_{opt}, and then rising sharply with further cooling. This indicates strongly that its root cause is is voltage noise, and not some sort of leakage or dielectric effect.

Figures 11 and 12 show the voltage noise and 20 pF noise as a function of temperature. As mentioned earlier, the hump in the -30^oC to -120^oC range has a 1/f spectrum and is probably g-r noise. It is also evident that the 4 Khz T_{opt} is slightly lower than the 8Khz T_{opt}, because of this slight frequency dependence.

By quadrature subtracting the voltage noise (corrected for input capacitance) from the total noise with a given input capacitance it is possible to calculate the current noise. Questions about the FET capacitances makes this dubious, but the following calculations use the Siliconix numbers. At room temperature, the current noise contribution is $1.5nV/\sqrt{Hz}$ at 8 Khz and $2.5nV/\sqrt{Hz}$ at 4Khz. The current noise drops very quickly with temperature, and at T_{opt} it is minimal, implying that the dielectric contribution is small. If it is all comes from shot noise, the room temperature current noise is $1 - 1.5fA/\sqrt{Hz}$, in agreement with the measured leakage current.

7. Conclusions

By cooling JFET's it is possible to reduce their noise significantly. Although the reduction in voltage noise is negligible, the total noise may be reduced by about 25% at 8 Khz for 20 pF input capacitance.

By examining noise spectra, it is possible to compare contributions to total

noise from different noise sources. It is seen that, for room temperature 2N4416's at audio frequencies, the dominant noise sources are channel noise and leakage current noise. When cold, the dominant noise source is channel noise. In both cases, the channel noise can be multiplied by feedback effects.

In a cascode circuit with gate floating and feedback to the source, the effective input capacitance was observed to be significantly larger than C_{gd}, an apparent failure of the lumped circuit element model. The reason for this is not understood, but it may be due to distributed capaitance along the channel.

8. Acknowledgements

The authors wish to thank Paul Griffon for help with experimental measurements. We also thank Martin Perl and the SLAC directorate for their support.

REFERENCES

1. Walter Innes, Spencer Klein, Martin Perl and John C. Price, SLAC Pub 2938, June 1983
2. E.R. Williams and G.T. Gillies, Lett. Nuevo Cimento,**37**,520(1983)
3. A. Van der Ziel, Proc IEEE **50**,1808(1962)
4. F.M. Klaasen and J.R. Robinson, IEEE Trans. Electron Dev.,**17**, 852 (1970)
5. A. Van der Ziel, Proc IEEE **51**,461(1963)
6. C. T. Sah, Proc. IEEE,**52**, 795 (1964) and references therein.
7. F. Bordoni, G. Maggi, A. Ottaviano and G.V. Pallottino, Rev. Sci. Instrum. **52**,1079 (1981)
8. A. Ambrozy, Electronic Noise,, 1982 Mc Graw-Hill International Book Company, Chapter 3-4.
9. Model K770OT, from MMR Technologies, 1400 Stierlin Road, Suite A5, Mountain View, CA, 94043
10. Silconix Inc. FET Design Catalog, July, 1983
11. Gary Matthai, Silconix Corp., private communication. This is also what would be expected using the standard p-n junction model.
12. see, for example, P.W. Nicholson, Nuclear Electronics, 1974, John Wiley and Sons., Chapter 5
13. D.A. Landis, N. W. Madden, and F. S. Goulding, IEEE Trans Nuc. Sci., **26**,428(1979)
14. D.A. Landis, C. P. Cork, N. W. Madden, and F. S. Goulding, IEEE Trans. Nuc. Sci., **29**,619, (1982)

Table I

Predicted Noise Levels at 8 Khz with 20 pF on gate (in units of $nV/\sqrt{Hz}$).

	2N4416		U311	
Source	300 K	140 K	300 K	140 K
Channel Noise ($\alpha = 0.7$)[a]	1.9	1.35	.85	.60
G-r Noise[b]	?	?	?	?
Correlated Current Noise	.11	.08	.08	.05
Shot noise (I_l = 1.5 pA)	1.4	0	1.4	0
Dielectric Noise(C_d=.3 pF)[c]	.74	.53	.74	.53
Total	2.5	1.5	1.8	.80

[a] α is assumed independent of temperature. [b] G-r noise is not calculatable.
[c] $\tan\delta = .003$.

Table II

FET Noise Measurements (in units of $nV/\sqrt{Hz}$.) The best device in one category was not always the best in others. Total noise measurements were made on 15 2N4416s and 5 U311s at room temperature and 7 2N4416s and 2 U311s at -140^oK. Voltage noise measurements were made on 15 2N4416s and 5 U311s at room temperature and 2 2N4416s cooled. The listed uncertainties are the widths of the distributions. Where no uncertainty is shown, the width was comparable to the experimental error ($.1nV/\sqrt{Hz}$).

Frequency		4 kHz		8 kHz	
		300 K	140 K	300 K	140 K
2N4416 gate grounded	best	2.1	2.0	1.8	1.7
	avg.	2.1	2.0	2.1 ±.3	1.9 ±.6
2N4416 20 pF on gate	best	3.6	2.6	3.0	2.4
	avg.	3.9 ± .4	2.9 ± .3	3.4 ± .5	2.5 ±.1
U311 gate grounded	best	1.5	-	1.5	-
	avg.	2.4 ± 1.5	-	1.9 ± .6	-
U311 20 pF on gate	best	5.4	3.0	5.4	3.0
	avg.	10.1 ±3.0	3.3 ± .3	6.8 ± 1.4	3.1 ± .1

Table III

Measured FET Parameters (2N4416). The leakage current I_g is expected to be 0 at 140^0K. There is no reason to expect the capacitances to change significantly during cooling.

Parameter	Measurement		
	300 K	140 K	$R(140K/300K)$
I_d	6-11 mA	12-17 mA	1.5
g_{fs}	5-6 mhos	8-9 mhos	1.6
I_g	.5-1.5 pA	-	-
C_{gs}	2.5 pF	-	-
C_{gd}	2.5 pF	-	-
V_g (gate floating)	.2V	variable	

FIGURE CAPTIONS

Figure 1. The FET model used in the noise and capacitance calculations. e_N and i_N are the total voltage and current noises, respectively.

Figure 2. Schematic diagram of the amplifier. All resistors are metal film.

Figure 3. I_d as a function of temperature for a typical 2N4416.

Figure 4. g_{fs} as a function of temperature for a typical 2N4416.

Figure 5. Voltage noise and 20pF total noise spectra at room temperature. The 20 pF simulates our apparatus.

Figure 6. Room temperature noise with the gate open. The current noise is dominant.

Figure 7. Voltage noise at $T = -93^oC$, showing g-r noise.

Figure 8. Voltage noise and 20pF total noise spectra at T_{opt}. The 20 pF simulates our apparatus.

Figure 9. 0-50 Khz spectrum with 20 pF on gate at room temperature.

Figure 10. Room temperature noise vs. capacitance on gate.

Figure 11. Voltage noise vs. temperature.

Figure 12. 20 pF noise vs. temperature.

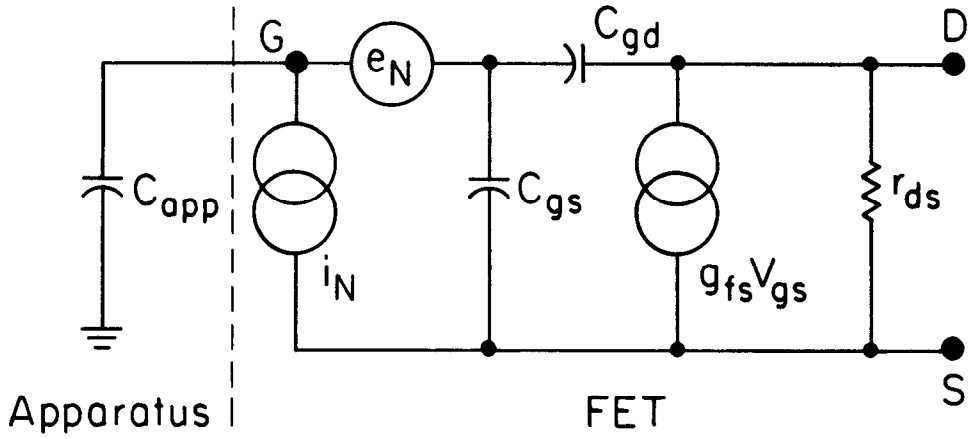

Fig. 1

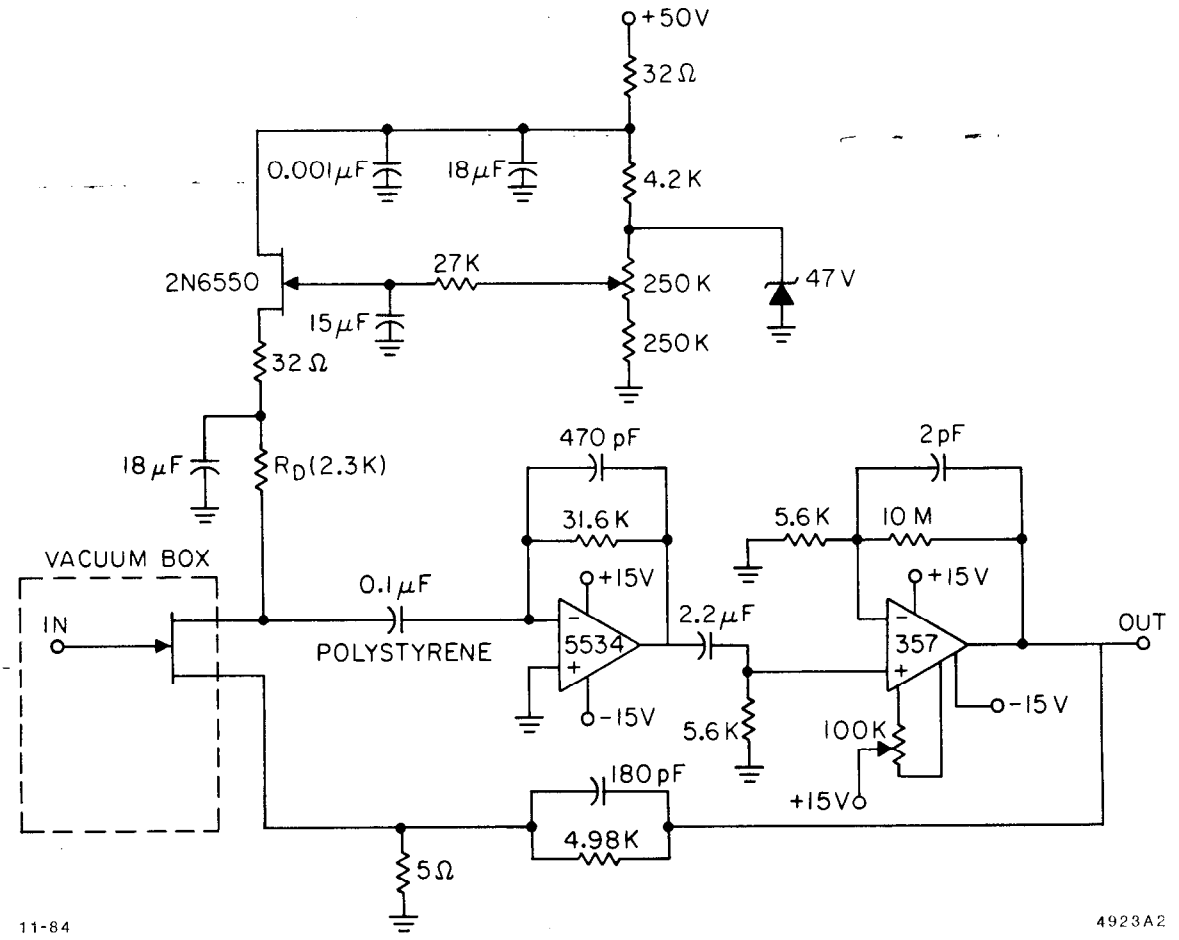
+50V
32 Ω
0.001μF
18μF
4.2 K
2N6550
27K
250 K
47 V
15μF
250K
32 Ω
18μF
RD(2.3K)
470 pF
2pF
31.6 K
5.6 K
10 M
VACUUM BOX
0.1μF
+15V
+15V
IN
POLYSTYRENE
5534
2.2μF
357
OUT
-15V
-15 V
5.6K
100K
180pF
+15V
4.98K
5Ω
11-84
4923A2

Fig. 2

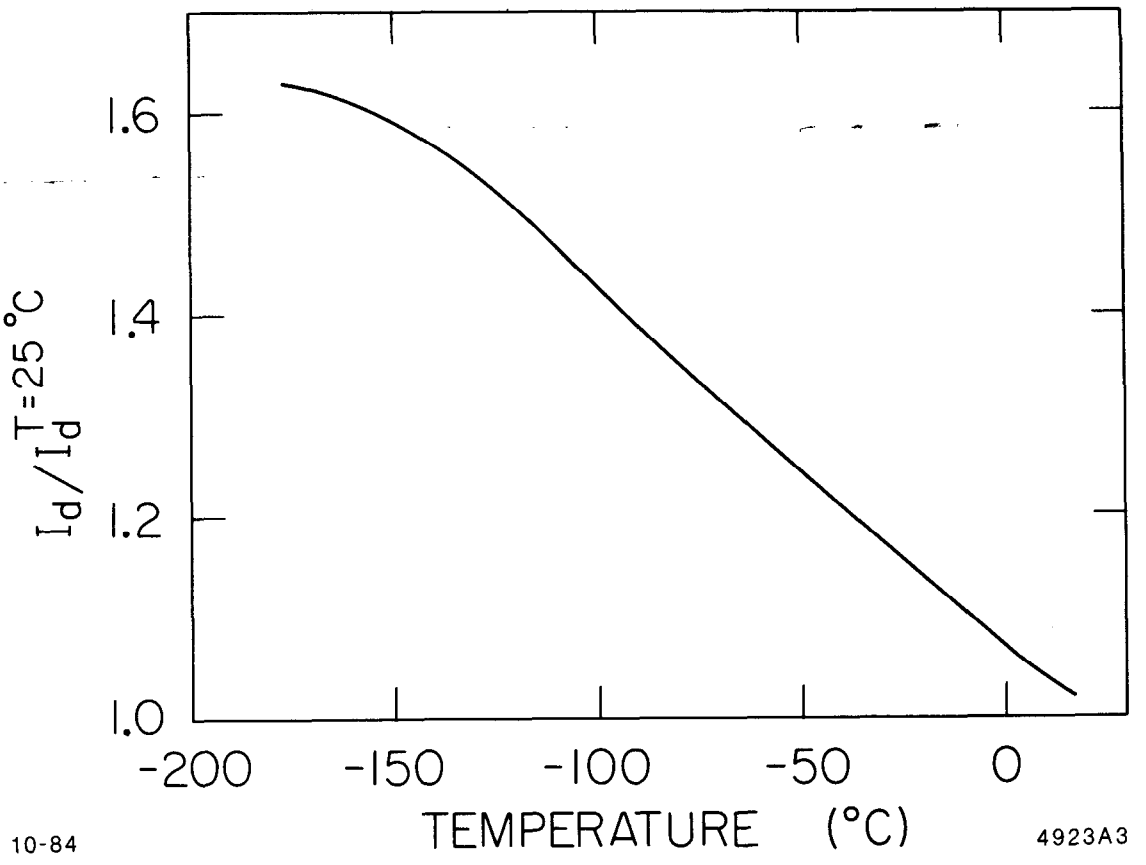
1.6
1.4
1.2
1.0
$I_d/I_d^{T=25\,°C}$
-200
-150
-100
-50
0
TEMPERATURE (°C)
10-84
4923A3

Fig. 3

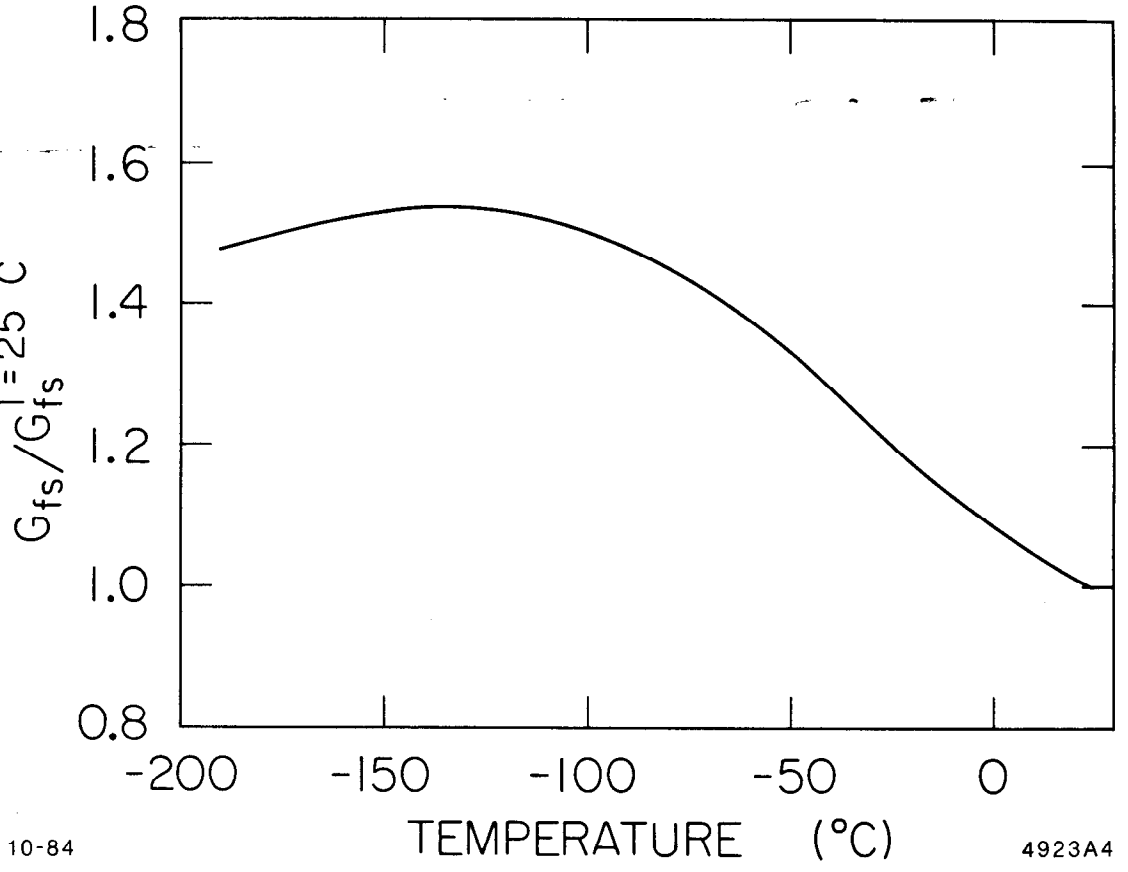
1.8
1.6
1.4
1.2
1.0
0.8
$G_{fs}/G_{fs}^{T=25\,°C}$
-200
-150
-100
-50
0
TEMPERATURE (°C)
10-84
4923A4

Fig. 4

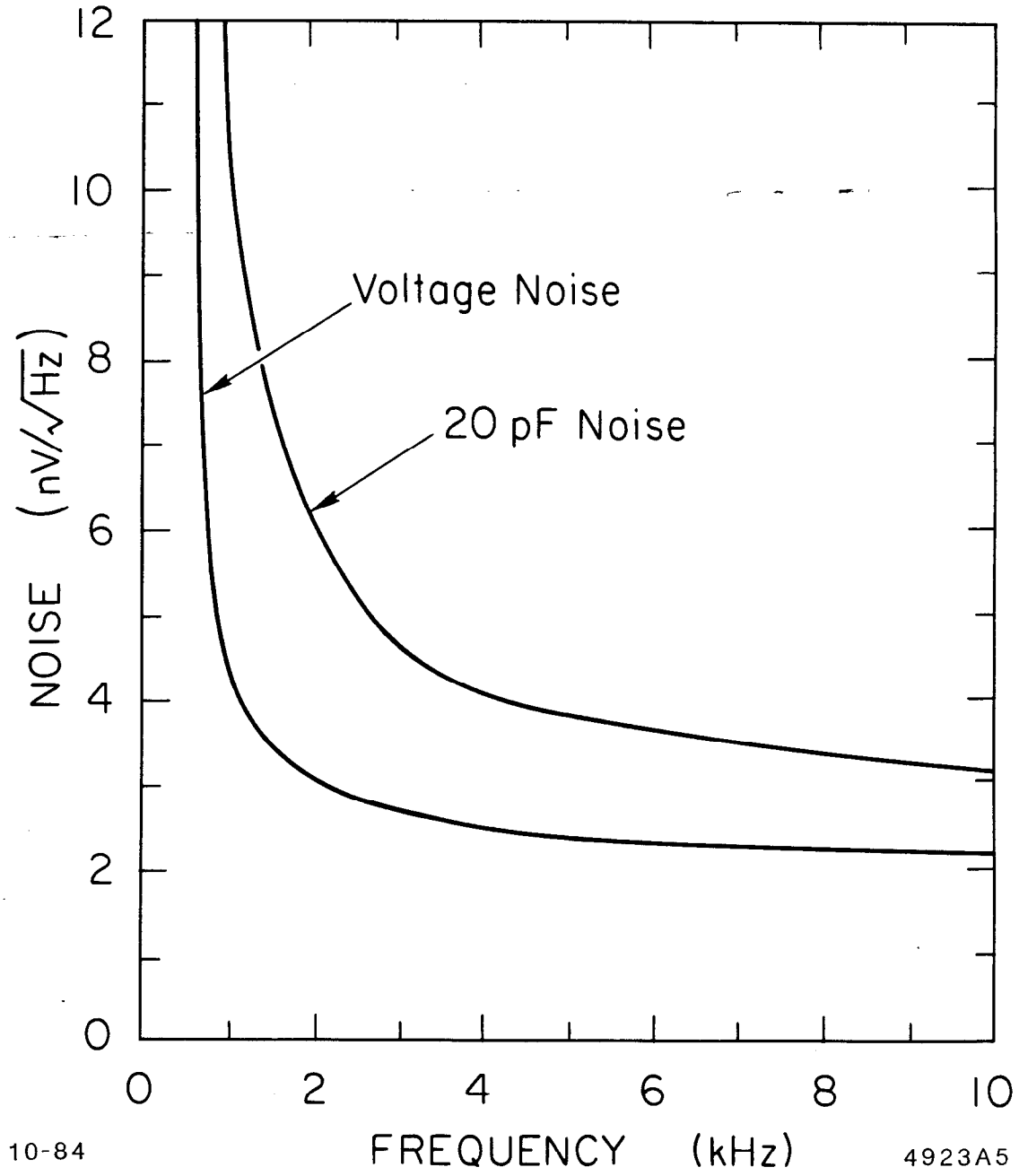
12
10
8
6
4
2
0
NOISE (nV/√Hz)
Voltage Noise
20 pF Noise
0
2
4
6
8
10
FREQUENCY (kHz)
10-84
4923A5

Fig. 5

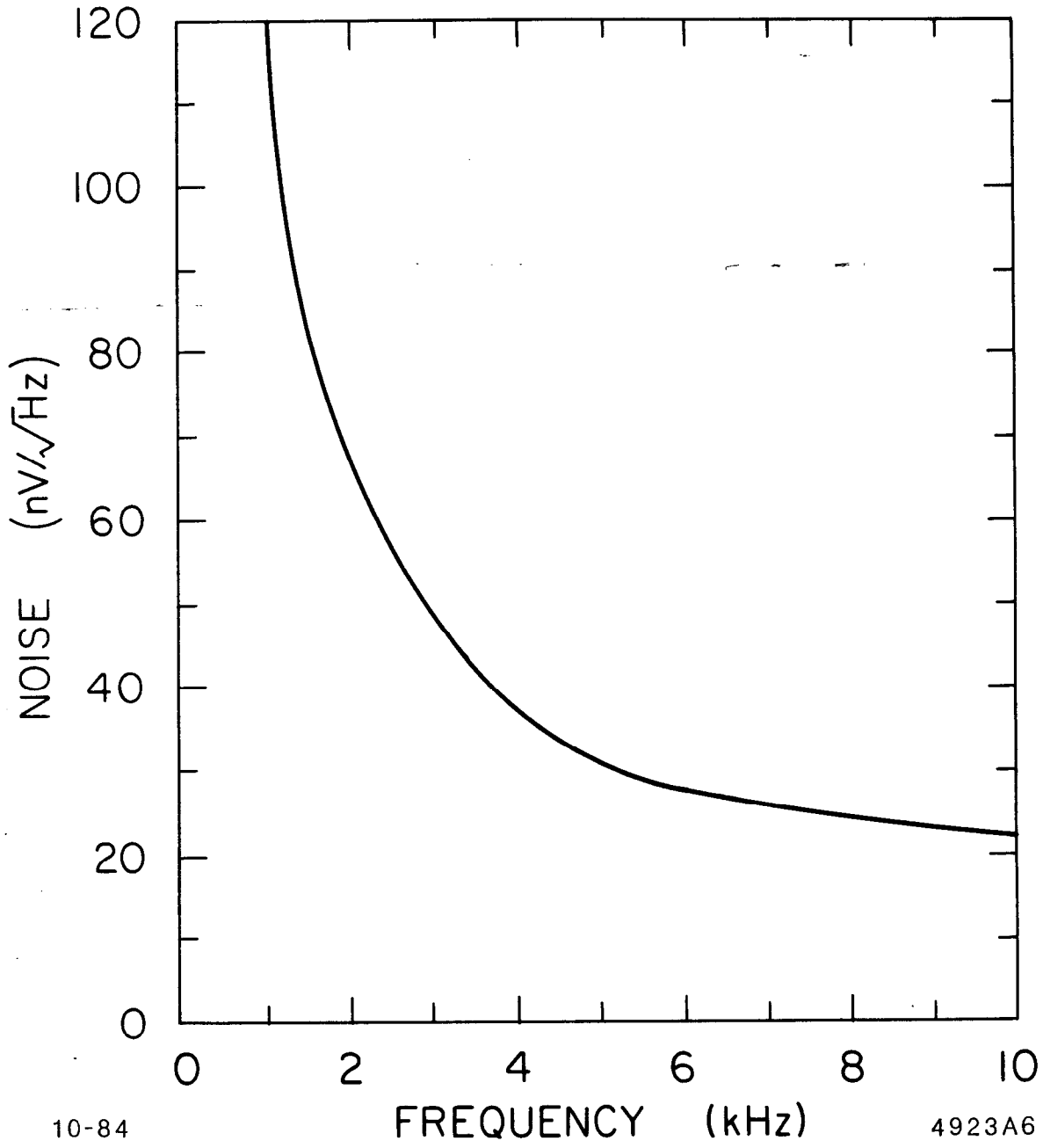
120
100
80
60
40
20
0
NOISE (nV/√Hz)
0
2
4
6
8
10
FREQUENCY (kHz)
10-84
4923A6

Fig. 6

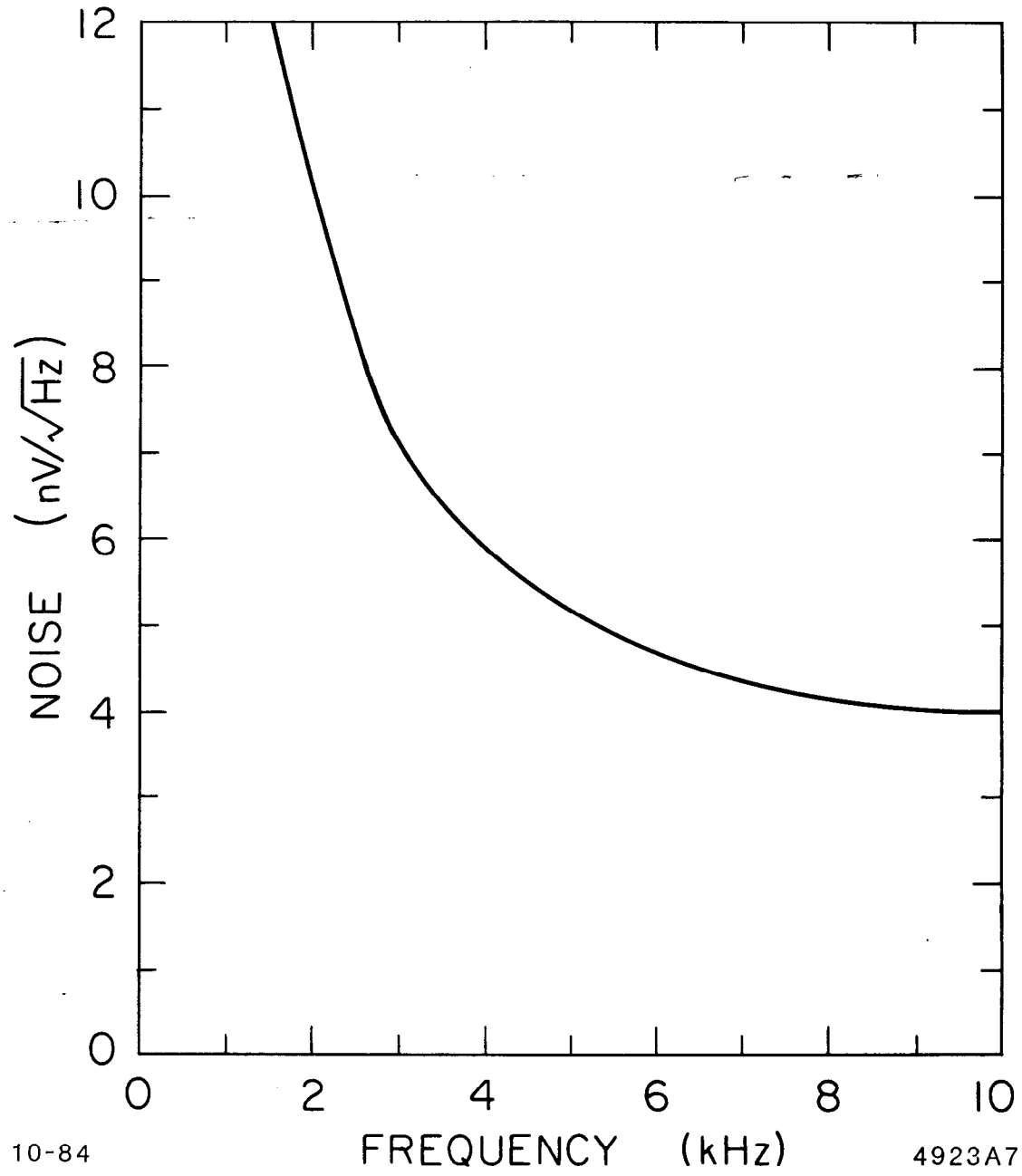

Fig. 7

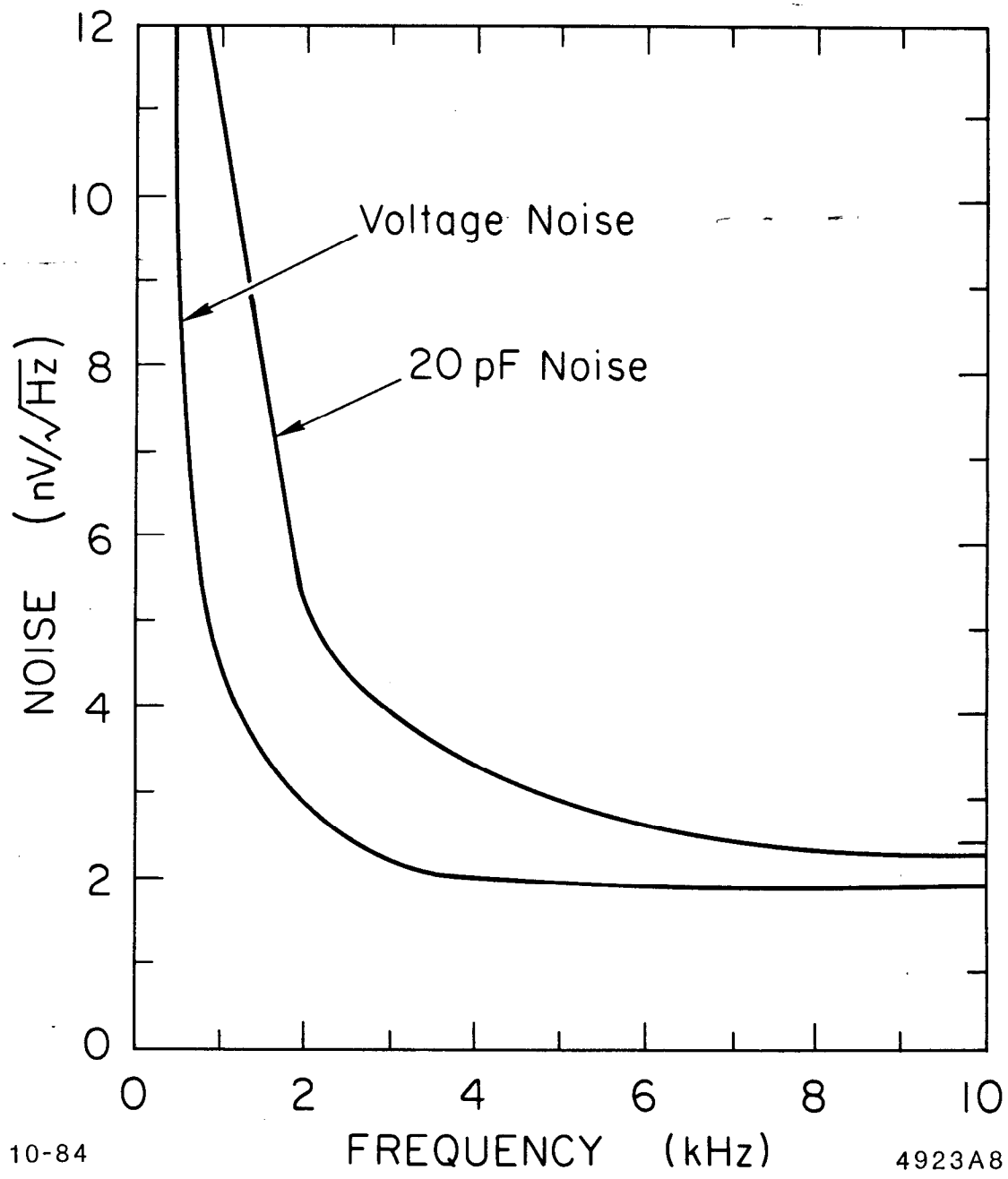
12
10
8
6
4
2
0
NOISE (nV/√Hz)
Voltage Noise
20 pF Noise
0
2
4
6
8
10
FREQUENCY (kHz)
10-84
4923A8

Fig. 8

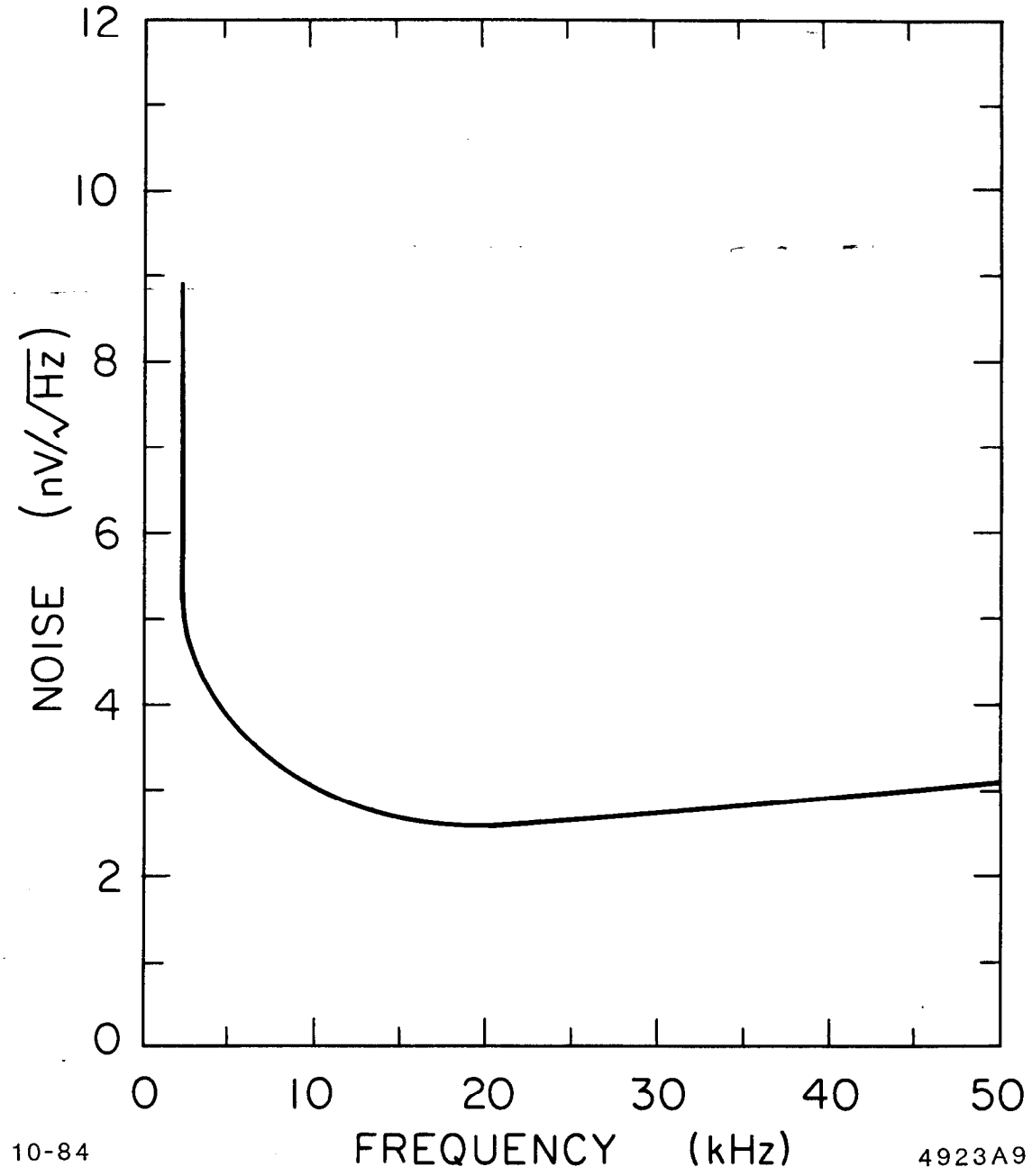
12
10
8
6
4
2
0
NOISE (nV/√Hz)
0
10
20
30
40
50
FREQUENCY (kHz)
10-84
4923A9

Fig. 9

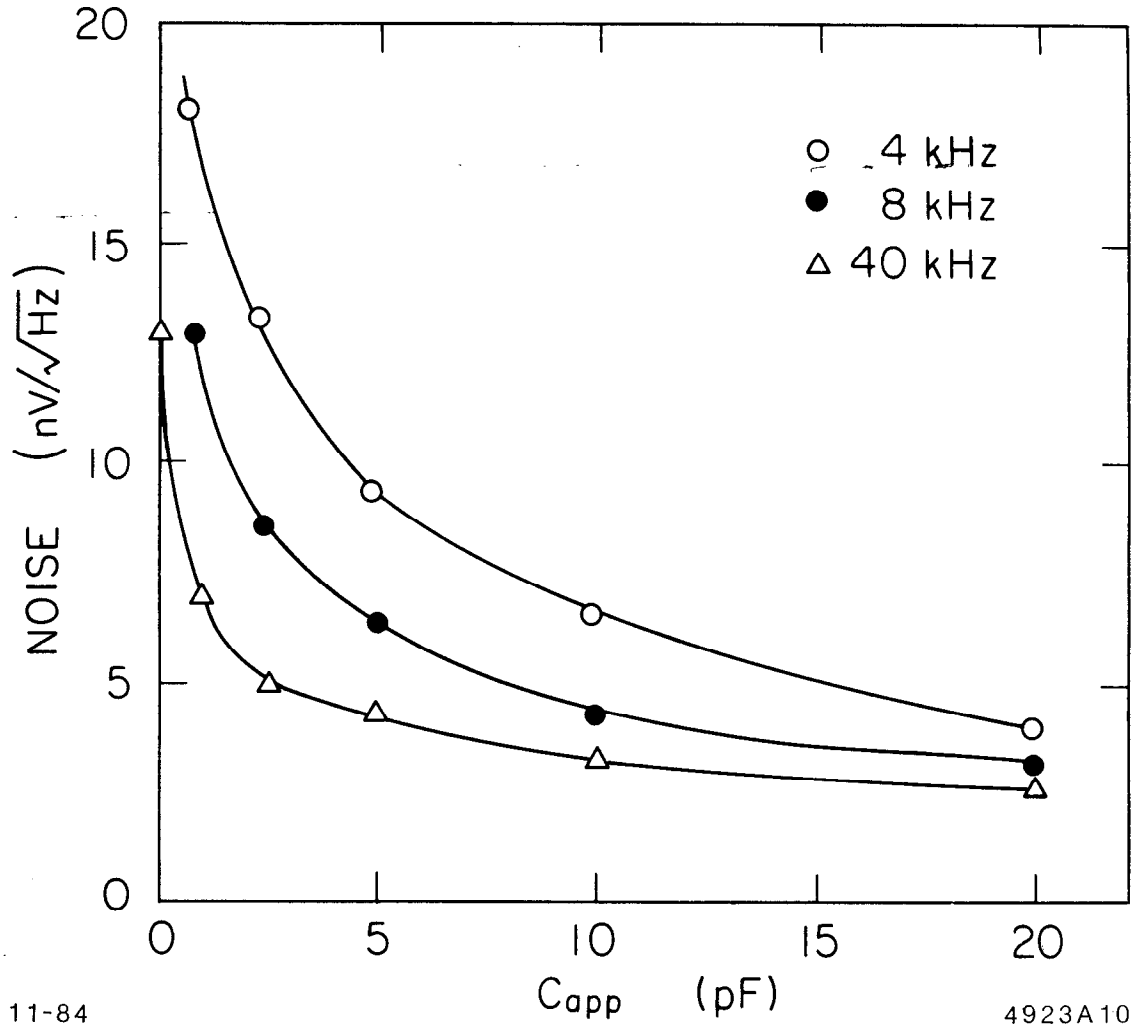
20
15
10
5
0
NOISE (nV/√Hz)
4 kHz
8 kHz
40 kHz
0
5
10
15
20
Capp (pF)
11-84
4923A10

Fig. 10

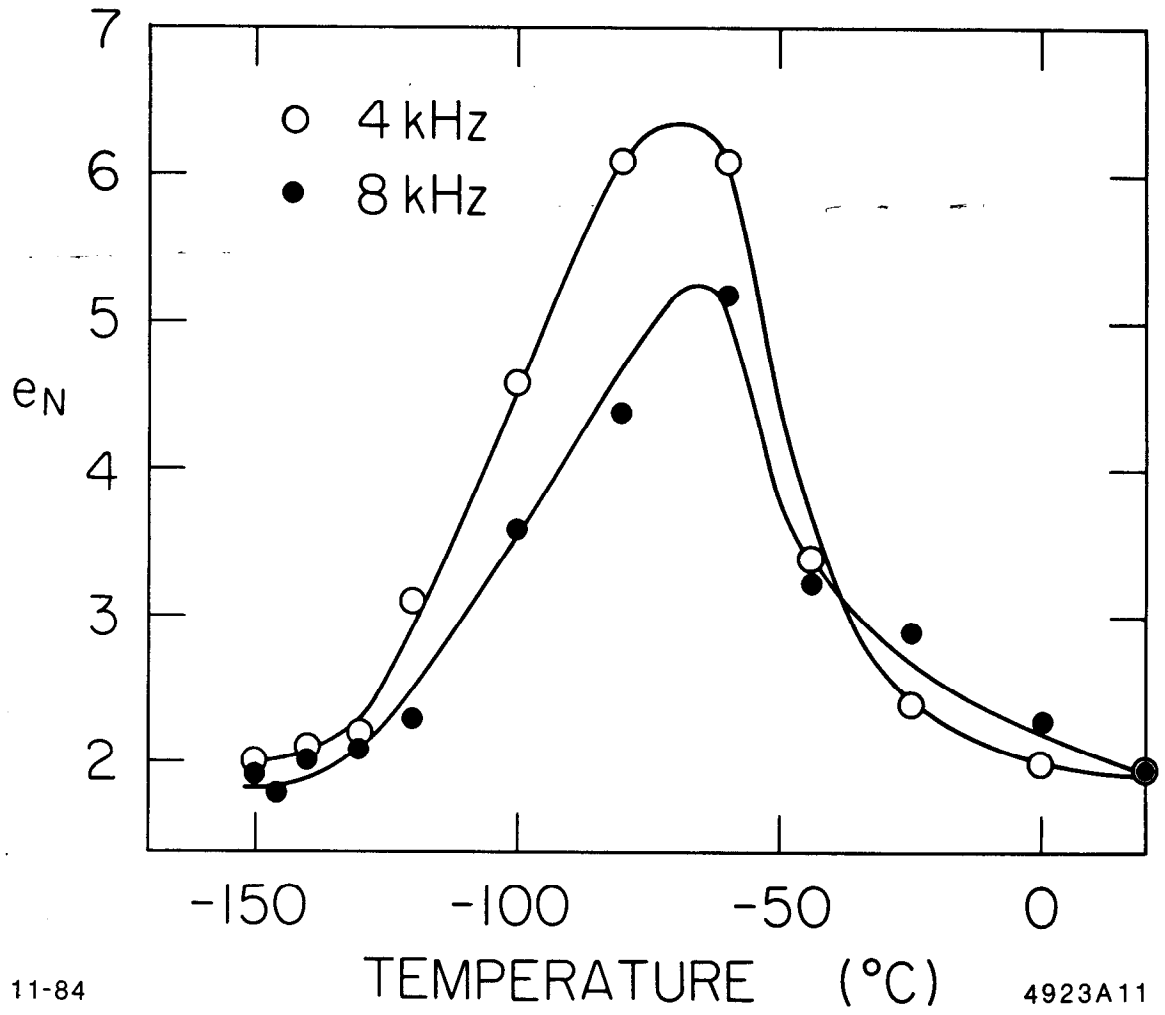

Fig. 11

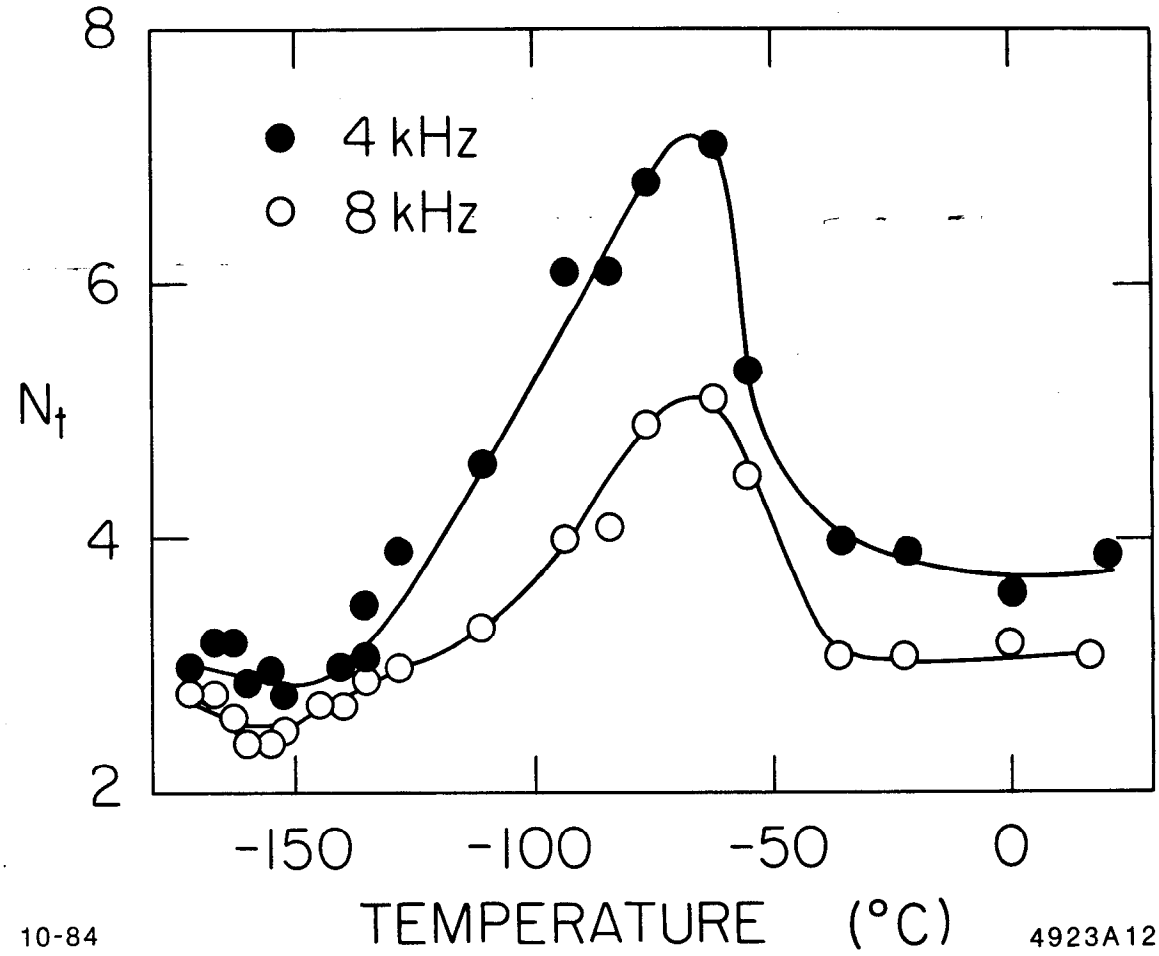

Fig. 12