SLAC-PUB-2987
October 1982
(E)

A VERSATILE SECONDARY TRIGGER FOR A MULTI-DETECTOR SYSTEM*

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Summary

The electronics of a secondary trigger for particle physics is described. The system has several desirable features that solve track recognition problems in situations where several subsystems of various cell configurations participate in the decision making. Track curvature and multiplicity are the criteria used. Versatility is attained through the use of Programmable Array Logic (PAL) and a 48-bit wide ROM-based sequencer that determines, with the resolution of a cell, the participation of each element in the decision process. Data from layers with arbitrary numbers of cells are shifted in a programmable manner through a PROM mask containing eight different track definitions. The results of any one of the eight triggering criteria are available 5.6 μs after the end of drift interval.

Introduction

Particle detectors at high-energy storage rings often incorporate a variety of subsystems, e.g., scintillation counters and drift chambers, that contribute to the trigger. While the repetition rate of the storage rings is several μs, the rate of useful physics events is less than 1/minute; thus the information determining the trigger has to be assimilated quickly to minimize deadtime. However, the trigger has to be sufficiently restrictive to not overburden the computing capabilities of the data acquisition and analyses systems. A typical solution is to form a pre-trigger from only the scintillation counters. This signal is usually available in a several hundred ns and has a rate of a few kHz. This is to be further reduced to a rate of less than a few Hz through the requirement of 1 or more tracks in the detector. Hence one needs a hardware track reconstruction device that cycles in less than 10 μs. It is important that the architecture of such a device allow for the particular details of the chambers involved and the possible non-uniformities of the magnetic field that the chambers are in. The ability to correlate tracks with scintillation counters further reduces extraneous triggers.

Electronics Circuits

A secondary trigger system was constructed for use with the cylindrical drift chambers and a bank of scintillation counters in the DELCO experiment at SLAC (see Fig. 1). The inner drift chamber is comprised of six layers having 64 cells around the cylinder while the outer drift chamber has ten layers with an equivalent of 68 to 102 cells including the gaps. The scintillation counter bank contributes 24 pairs of signals and is placed at the outer edge of the DELCO detector. Because of the non-integral relationship between the numbers of cells in each subsystem a single shift clock would not satisfy the criteria of a priori selected coincidences while the coincidence circuit scans 2π radians in the ϕ-angle. Through use of a 48-bit wide programmable sequencer that generates a number of clock and control signals several problems were solved: 1. The number of cells in ϕ was closely controlled via WIDTH CLOCKS to make the curvature of minimum momentum (200 MeV/c in this case) as close as ideally possible despite the great variety of different number of cells between layers. 2. STEERING and SAVE circuits solved the common problem of combining cells that cross the boundary of the beginning and end of the circular shift register scan. 3. ZERO control was applied to gaps where no cells were available to participate in any trigger decisions. 4. Through use of the various clocks in conjunction with PALs and shift registers, data were manipulated in such a way that one 256 × 8 PROM was sufficient to identify eight different triggering criteria as the data were interrogated around ϕ. 5. Eight different outputs are simultaneously available, each meeting a different criterion of triggering, i.e., the number of elements participating in a track definition, various combinations of the subsystems employed in the decision process and the number of tracks recorded for each definition. 6. Finally, one of the outputs is used as the secondary trigger, while the other outputs are recorded for a later analysis to determine whether the most efficient of the eight possibilities has indeed been selected as the event trigger. If required, a selection of a different output can be made via a front panel switch.

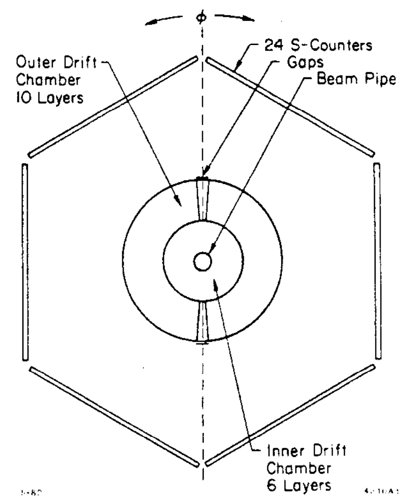

Fig. 1. Simplified end view of detector (drawing is not to scale; the gap size is exaggerated).

For a description of the system refer to the block diagram of Fig. 2. The system is composed of four kinds of modules (disregarding the clock fanout) which are: the SEQUENCER, the CURVATURE CIRCUITS (two modules), the TRACK ROM, and the S-COUNTER SHIFTER.

The Sequencer

The SEQUENCER is a 48-bit wide by 256-bit deep PROM driven by a 20 MHz clock. Through suitable programming the 48 outputs fulfill several functions by generating: 1. Non-periodic SHIFT CLOCKS to shift a total of 16 layers of the two drift chamber systems keeping a well defined momentum envelope while rotating around ϕ. 2. SAVE CLOCKS to solve the boundary problem at the beginning and end of the shift so that adjacent cells that are (artificially) divided by the boundary may be

* Work supported by the Department of Energy, contract DE-AC03-76SF00515.

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(Presented at the Nuclear Science Symposium, Washington, D.C., October 20-22, 1982.)

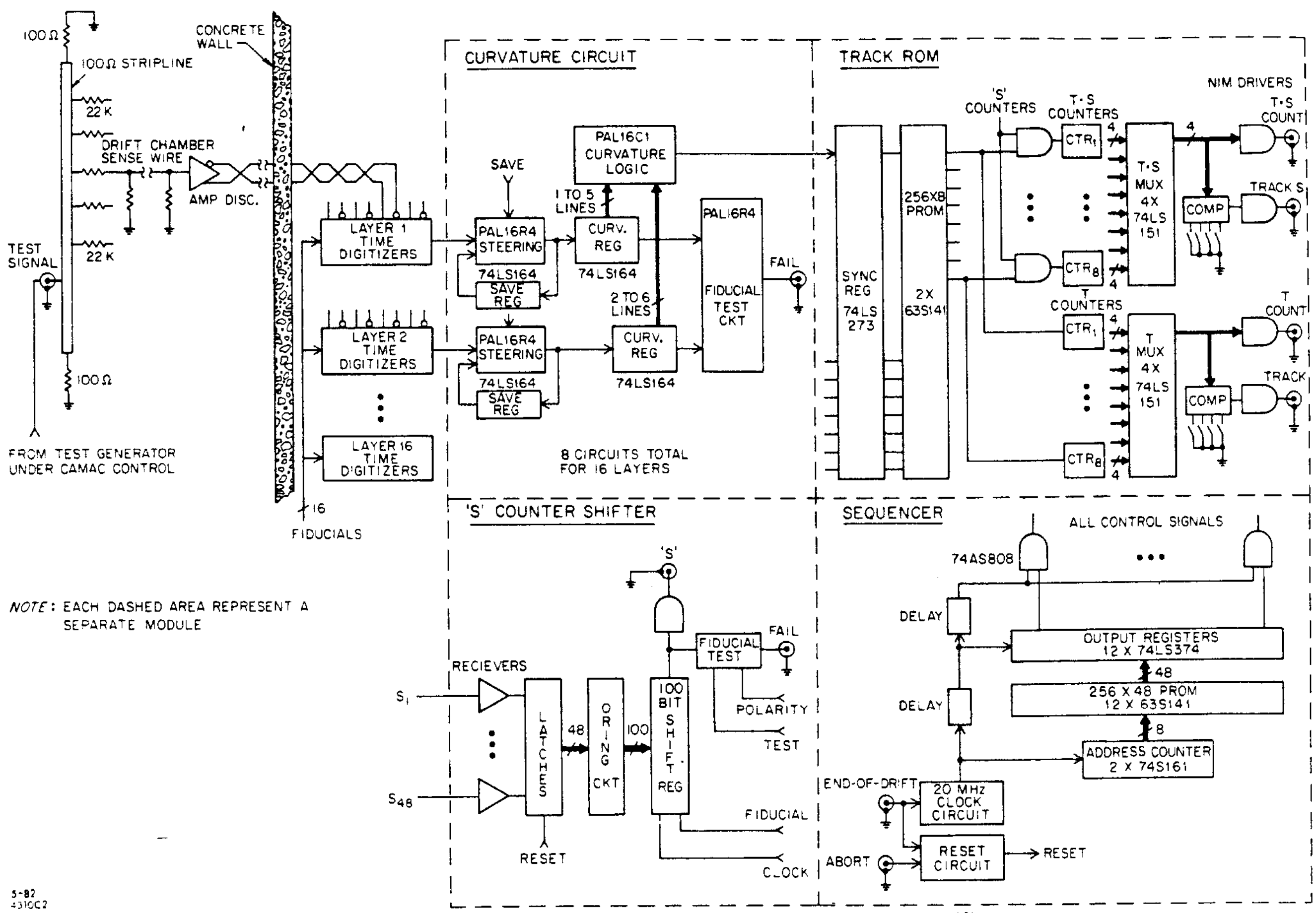

Fig. 2. System's block diagram.

combined in the determination of the momentum envelope. 3. WIDTH CLOCKS to finely tune at each step of the rotation the number of cells in ϕ that are to be combined. 4. ZERO controls as discussed above. 5. TRACK ROM CLOCKS which output the selected trigger followed by the sequential strobing of the results of all eight track definitions. 6. A FIDUCIAL bit used to test for a "stuck" condition in the shift registers. 7. A SYSTEM CLEAR.

The clock shift rate of the system has been chosen at 20 MHz to allow use of easily available LS-TTL integrated circuits and to keep the power dissipation low. The parallesism of the shifting, however, ensures that the secondary trigger is available only 5.6 μs after end of the drift interval.

The Curvature Circuits

Shift registers and PALs are used to form the momentum envelope "window" where the width of the envelope as it shifts through the circular scan is controlled. The first several bits from each layer are stored in SAVE registers to be retrieved at the end of the bit stream thus taking care of tracks that overlap the first and last cells of the scan. In order to find "stuck" shift register bits a fiducial is injected into the far end of the drift time digitizers[1] and shifted throughout the system. In the CURVATURE CIRCUITS these bits are tested for "stuck-on-0" and "stuck-on-1". PALs were found to be very useful in reducing the chip count in these circuits without sacrificing speed.

The Track ROM

A 256-word × 8-bit PROM (2 ICs) is programmed to deliver outputs corresponding to the eight different criteria of track definition. This versatility is especially desirable for establishing experimentally an optimum criterion for the secondary trigger. The eight outputs from the CURVATURE CIRCUITS are deskewed at the SYNC-REGISTER of the TRACK ROM before being applied to the address lines of the PROM. The number of tracks counted in the binary counters originate from either the cylindrical chambers only (T-COUNTERS) or from the coincidence of chamber tracks and the corresponding signals from the scintillation counter banks (T·S-COUNTERS). When tracks are "recognized" by the PROM the appropriate T-COUNTER is incremented. If there is a corresponding signal from a scintillation counter then a T·S-COUNTER is also incremented. An eight way multiplexer selects one of these binary counter states as the secondary trigger while the track counts from the other, optional, trigger definitions are recorded and analyzed to ascertain that indeed the optimum trigger has been used.

New trigger combinations are easily accommodated by inserting different PROMS.

The S-Counter Shifter

There are 24 scintillation counters positioned at the outer edge of the detector. The S-COUNTER SHIFTER allows these 24 signal pairs (two for each scintillation counter) to be combined with the drift chamber data in forming a track definition.

Testing

Testing of the complete system, including sense wires and drift-time digitizers, is accomplished via CAMAC control: trains of pulses are applied to the sense wires and processed throughout the system simulating various (programmable) track patterns.

Reference

1. D. Ouimette, D. Porat, A. Tilghman, S. Wojcicki and C. Young, IEEE Trans. NS-29, No. 1 (Feb. 1982) pp. 290-293.