SLAC-PUB-2974
NUB-2568
September 1982
(E)

A Multi-Channel Random Pulse Counter*

Laszlo Baksay

Stanford Linear Accelerator Center, Stanford University
Stanford, California

Malcolm C. Smith

Department of Physics, Northeastern University
Boston, Massachusetts

Abstract

We describe a gated 64 channel random pulse input register and controller unit. In conjuction with segments of a commonly used LeCroy qVt multi-channel analyzer, it comprises a stand-alone counter system which is useful in experiments with a large number of detectors. In particular, when hardware and software components are still in the debugging phase, this device can largely reduce the labor of data taking for diagnosis.

Input and output levels of the device are TTL for general compatibility. In its present configuration, the system can be used wherever samples of random pulses with rates up to 2 kHz per channel must be taken on up to 64 channels simultaneously, for example in cosmic ray tests. After making minimal modifications to the unit, rates to about 10 kHz can be accepted.

(Submitted to Scientific Instruments)

---

*Work supported in part by the National Science Foundation under contract No. NSF-PHY20020 and the U.S. Department of Energy under contract No. DE-AC03-76SF00515

Introduction

The main motivation to build this device lay in the desire to checkout the performance of about 3000 drift chamber channels at different stages of completion of the Magnetic Calorimeter Detector (MAC) at the Stanford Linear Accelerator Center. At a stage when the hardware and software were still being debugged, a stand alone scaler system would, for example, allow us to run cosmic ray high voltage plateau curves, identify dead or noisy channels, etc., without the need for the on-line computer. Our design is flexible enough to be useful in a variety of similar situations, for up to 64 channels at one time.

Instead of constructing a complete new system, we decided to incorporate stages of the LeCroy model 3001 qVt Multichannel Analyzer, which is available to most high energy physics research groups. Apart from the cost, the primary advantage of this was that the qVt already had output capabilities for an oscilloscope and a printer.

The internal circuitry of the qVt may be accessed through a 44 pin connector on the rear panel, allowing us to manipulate segments according to our needs.

Under this scheme, the general tasks of our auxiliary device are to:

- provide timing and control for the data collecting cycle
- buffer incoming data
- provide addresses for qVt memory locations
- transfer data
- control qVt circuitry

Overall Operation

(Fig. 1)

We use a gated system in which incoming pulses are accepted on 64 parallel input lines and held during a 500μs period (one data collection cycle). The gate duration of 500μs allows us to observe cosmic ray rates of several hundred Hertz, without significant correction for two hits during one data collection cycle. An incoming pulse flips a J-K flip-flop to its "on" position. At the end of the gate period, this bit of data is transferred to a shift register for serial shifting to the qVt. The flip-flop is immediately cleared, thus ready to accept new data.

Turning on the data-collecting switch (start/stop) will start data taking. At the start of every data taking cycle, Controller A clears the input data buffer (DS) which then can accept new data. After 500 μs, Controller A enables data transfer from the buffer to the shift registers (SR) and initializes the Address Storage Unit (ASU) to 1,which indicates to Controller B to load the data from the buffer into the SRs. Controller A's cycle now repeats starting with clearing the buffer.

While new input data is being collected in the buffer, Controller B handles the transfer of the previous data from the SRs to the qVt memory. It goes through 64 cycles and serially shifts 64 data bits into the corresponding qVt memory locations, the addresses of which are provided by the ASU. Controller B starts operating when the ASU is reset to address "1". It sends a command to the SRs to receive the data from the buffer. It disables the qVt internal control and in its n^{th} cycle, directs the qVt to accept the n^{th} data bit from the shift registers and to add it to the contents of the n^{th} memory location using the qVt's Increment Register. Before starting the $(n+1)^{st}$ cycle, Controller B

increments the address stored in the ASU to (n+1) and signals the shift registers to present the next data bit.

When the ASU reaches 64, it inhibits Controller B. These sections then lie quiescent until Controller A again resets the ASU to address "1".

The "stop" signal to Controller A ends the data collection period. The accumulated data can now be displayed on an oscilloscope using the standard front panel controls of the qVt.

The system's only deadtime, introduced when loading the data from the buffer into the SRs, is about 160ns, that is less than one permille and negligible.

Detailed operation

Controller A:

(Figures 2, 3 and 4)

Controller A has the following functions:

- time data collection cycle
- clear input buffer
- control data transfer modes of the shift registers
- initialize the Address Storage Unit

Controller A is based on four 74123 retriggerable monostable multivibrators. When the start pulse from the start/stop push-button switching circuit (Fig. 9) is received at the 7473 J-K flip-flop clock input the $\bar{Q}$ output goes low triggering timer "a". Output $a\bar{Q}$ then goes low and turns on the output of NAND gate "g" which drives a light emitting diode indicating data collection. The low to high transition of aQ triggers timer "c" which, by turning the driver NAND gate outputs to low, sends a 40 ns clear signal to the input

buffer flip-flops. Output aQ stays high for 500 µs, after which it returns to low, triggering timer "b". bQ goes high for 200 ns. This will set the output of driver NAND gate "e", which is the shift/load input line to the SRs, to low for 200 ns, which enables loading of the data present in the input buffer into the SRs. Actual loading is done by Controller B via the clock inputs of the SRs. Output $b\bar{Q}$ low triggers timer d to send a 40 ns initialize signal (low) to the ASU, resetting the stored address to "1".

Address Storage Unit

(Figure 5)

The ASU has the following functions:

- store the address of qVt memory location
- release address to qVt
- signal Controller B when address is at 64

The ASU stores the memory address to be accessed and upon signal from Controller B, presents this address to the qVt on the Memory Address Lines. It also signals Controller B, via the "High at Maximum Address" (HMA) line, when address 64 has been reached. The ASU consists of several 7473(A) J-K flip-flops in series, which merely count up to 64, and ten tristate drivers (74365) at the output, which must be disabled while not in use. This is done by Controller B which sets line ASU-4 high when needed.

At the beginning of a data collection cycle, the address stored in ASU is "64" (due to the previous cycle), so the HMA line is high . The "intialize address" signal, from Controlller A to the ASU, resets the address to "1" and HMA goes low, thereby triggering Controller B.

Controller B

(Figures 6, 7 and 8)

Controller B has the following functions:

- time the data transfer cycle
- organize data transfer from buffer to qVt
- set the ASU
- handle qVt operation

Controller B consists of seven 74123 timers and a 7473 NAND gate.

The high to low transition of the HMA line starts timers "h" and "i" to go into 64 cycles of 2 µs duration each. The first low to high transition at the NAND gate output loads the buffer data into the SRs and the first data bit is presented to the qVt. (The NAND gate is needed as a driver/fan-out for the 8 SRs. Otherise, the iQ output could have been used.) At the beginning of further cycles, the content of ASU is incremented by one and as the DS-1 line is now set to "shift" (high) by Controller A, the clock signals serially shift data one bit per cycle from the SRs to timer "l" in Controller B (DS-4 line) and from there to the correct qVt memory location. While $i\bar{Q}$ is low, it enables the output lines of the ASU and the external control feature (EXT ENB) of the qVt memory. As at the beginning of every cycle, jQ is high for 200 ns, the address at the ASU output is latched into the qVt Memory Address Latch (MAL). The "Read" mode for the memory is established by $n\bar{Q}$ being high, and the "low" signal from $k\bar{Q}$ (EXT LD) loads the contents at that qVt address into the qVt Incrementing Register. This value is incremented by one, only if the corresponding data bit is one. This is accomplished by a pulse from timer "l" over the INCR REG line. Finally, the content of the Increment Register is written back into memory by a 500 ns "low" signal from $n\bar{Q}$, setting the R/W

line to "write" mode. When address 64 is reached, the HMA line of the ASU goes high inihibiting further transfer operation by Controller B until the end of the 500 µs data collection cycle.

If data taking has been stopped, the qVt memory can be reset to zero by pushing the "clear" button, which will ground the switching circuit output (fig. 9). This will also clear the 7473 in Controller A. To allow accumulating data over several runs, clearing is not done automatically at the beginning of a data taking period.

Usage

To make the unit as generally useful as possible, all circuitry including data inputs and outputs, is TTL logic, working with a "high" of +5 V and a "low" on ground. The input signals should maintain the "high" state for at least 20 ns duration. An external power supply for 5V, 100 mA is needed.

The connection to the qVt is via a J2 connector with the pin assignments following the convention for the CAMAC data bus. 18 lines are used, 10 for address, 7 for control and 1 for ground.

Accumulated data can be displayed using the regular qVt capabilities, that is the front panel connections for an oscilloscope or the rear panel connections for a printer. For the latter the available LeCroy interface needs access to the rear panel J2 plug and therefore, the register/controller unit must be disconnected. We have, so far, mainly used the oscilloscope option. If frequent use of a printer should become necessary, one could easily build an electronic switch for the 18 rear panel lines.

At present, we use a data collection cycle of 500 µs duration, well matched to our application.Here the data transfer, taking about 128 µs, is not the

rate limiting factor. Should a faster data transfer rate be desirable in the future, then one can cut the transfer cycle time by about 25% from 2 μs/bit to 1.6 μs/bit. Thus, the possible data taking rate could be increased from 2 kHz, at present, to about 10 kHz. On the other hand, for very low event rates, the gate time can be increased from 500 μs as needed.

We would like to thank Professor R. Weinstein for suggesting such a device to us and for useful discussions.Comments by Professor W. Faissler were also helpful.

References

Technical Information Manual for Model 3001 qVt Multichannel Analyzer, LeCroy Research Systems Corp., Spring Valley, New York

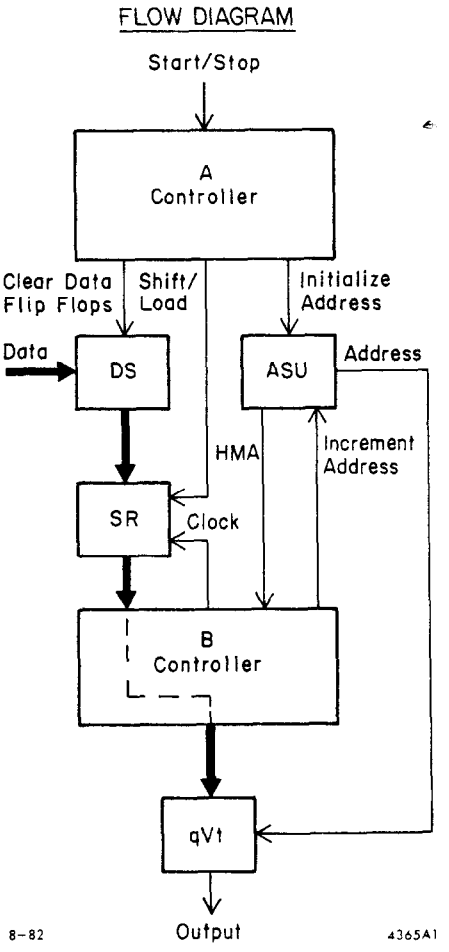

FLOW DIAGRAM
Start/Stop
A
Controller
Clear Data
Flip Flops
Shift/
Load
Initialize
Address
Data
DS
ASU
Address
HMA
Increment
Address
SR
Clock
B
Controller
qVt
Output
8-82
4365A1

Fig. 1

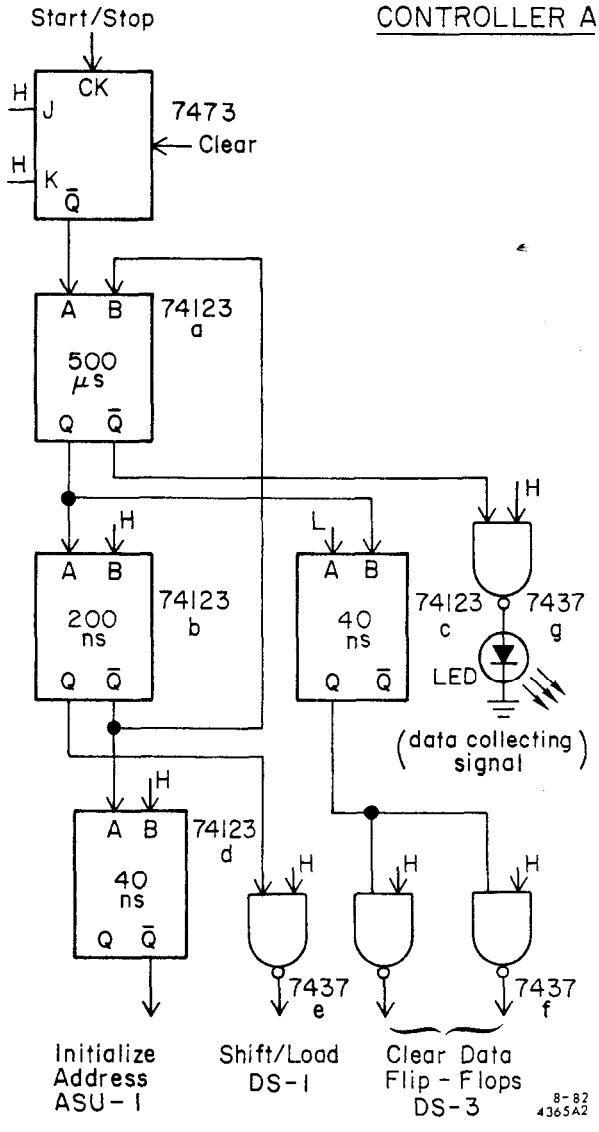

Start/Stop
CONTROLLER A
CK
H
J
H
K
Q̄
7473
Clear
A B
500 μs
Q Q̄
74123
a
H
A B
200 ns
Q Q̄
74123
b
L
A B
40 ns
Q Q̄
H
74123
c
7437
g
LED
(data collecting signal)
A B
40 ns
Q Q̄
74123
d
H
7437
e
H
H
7437
f
Initialize Address ASU-1
Shift/Load DS-1
Clear Data Flip-Flops DS-3
8-82
4365A2

Fig. 2

TIMING DIAGRAM CONTROLLER A

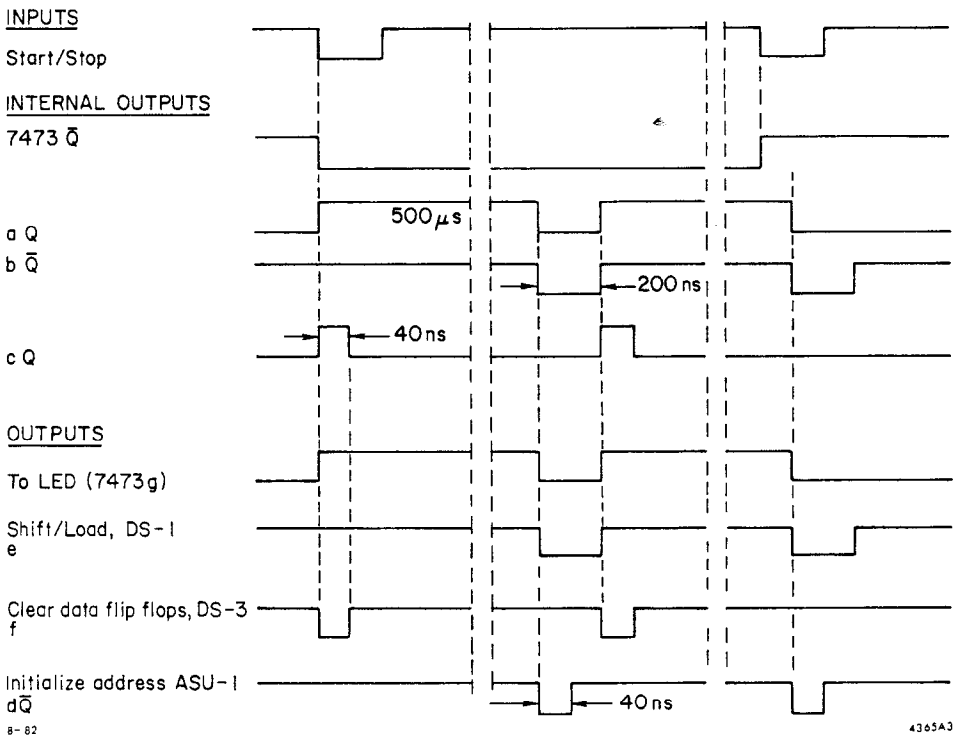


Fig. 3

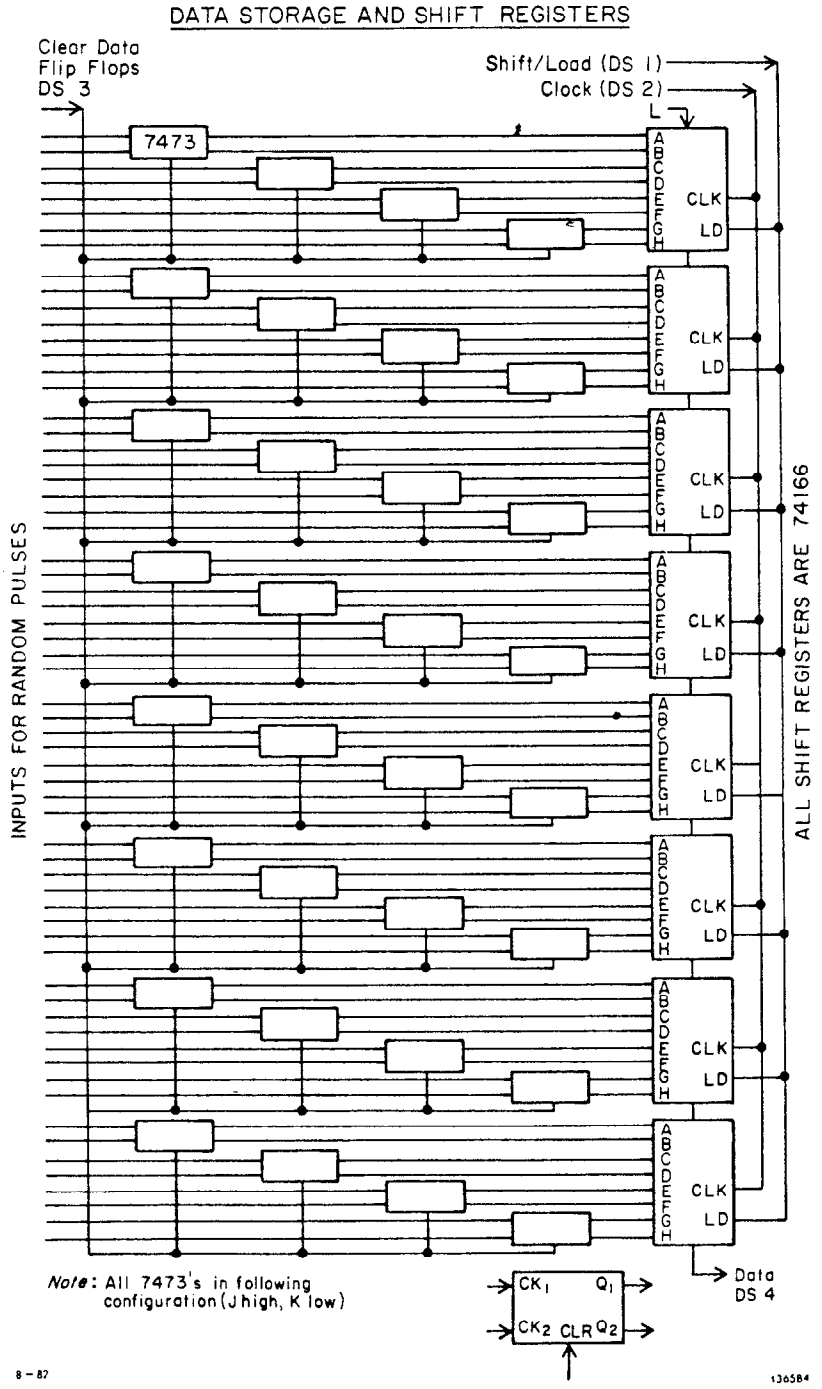

DATA STORAGE AND SHIFT REGISTERS
Clear Data Flip Flops DS 3
Shift/Load (DS 1)
Clock (DS 2)
L
7473
A
B
C
D
E
F
G
H
CLK
LD
INPUTS FOR RANDOM PULSES
ALL SHIFT REGISTERS ARE 74166
Note: All 7473's in following configuration (J high, K low)
CK1
Q1
CK2
CLR
Q2
Data DS 4
8-82
136584

Fig. 4

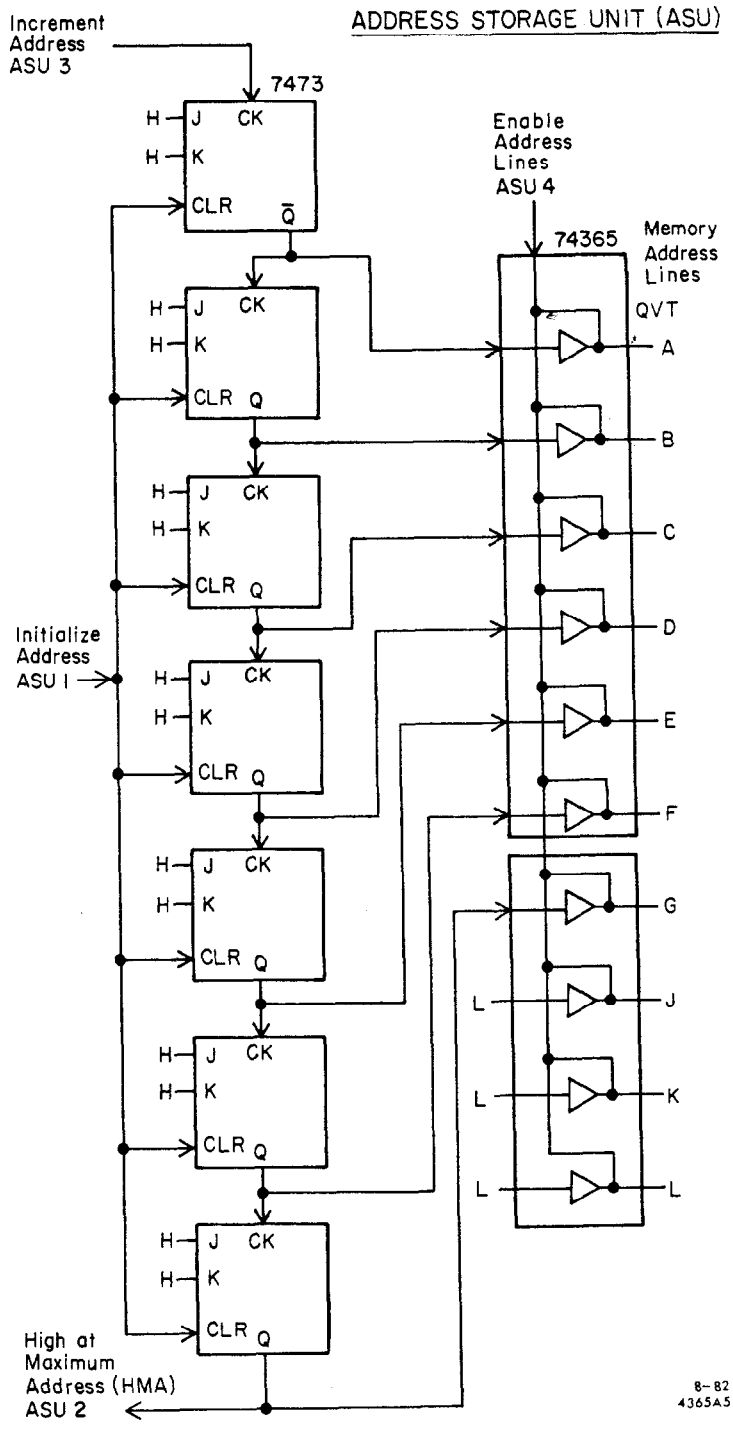

ADDRESS STORAGE UNIT (ASU)
Increment Address ASU 3
7473
H
J
CK
K
CLR
Q
Enable Address Lines ASU 4
74365
Memory Address Lines
QVT
A
B
C
D
E
F
G
L
J
K
L
Initialize Address ASU 1
High at Maximum Address (HMA) ASU 2
8-82
4365A5

Fig. 5

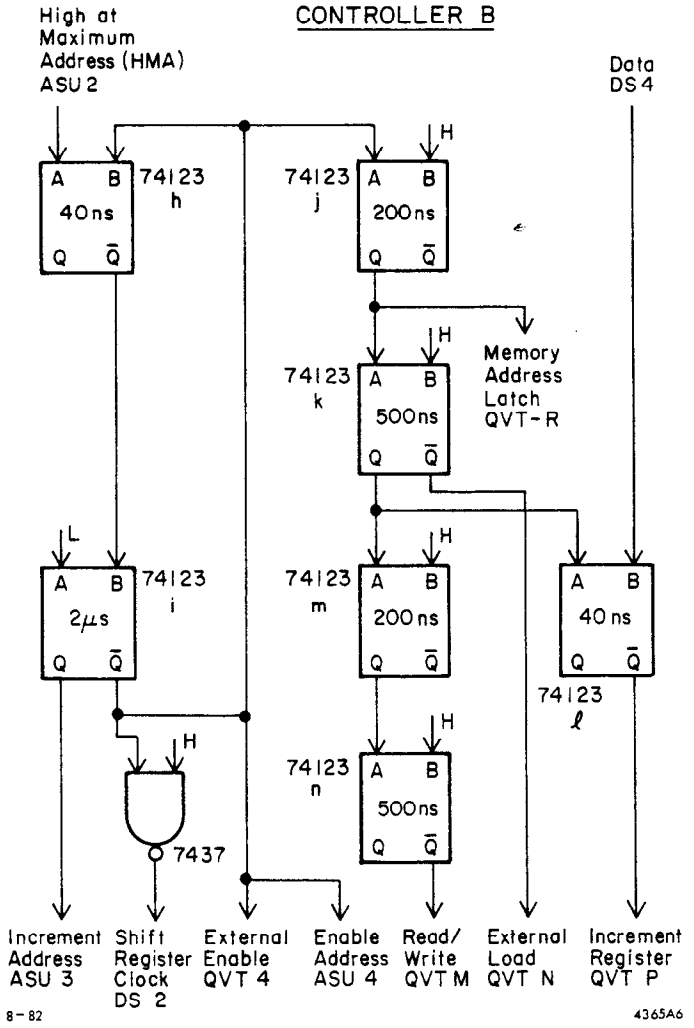

CONTROLLER B
High at Maximum Address (HMA) ASU 2
Data DS 4
74123 h
40ns
74123 j
200ns
74123 k
500ns
Memory Address Latch QVT-R
74123 i
2μs
74123 m
200ns
74123 n
500ns
74123 ℓ
40ns
7437
Increment Address ASU 3
Shift Register Clock DS 2
External Enable QVT 4
Enable Address ASU 4
Read/ Write QVT M
External Load QVT N
Increment Register QVT P
8-82
4365A6

Fig. 6

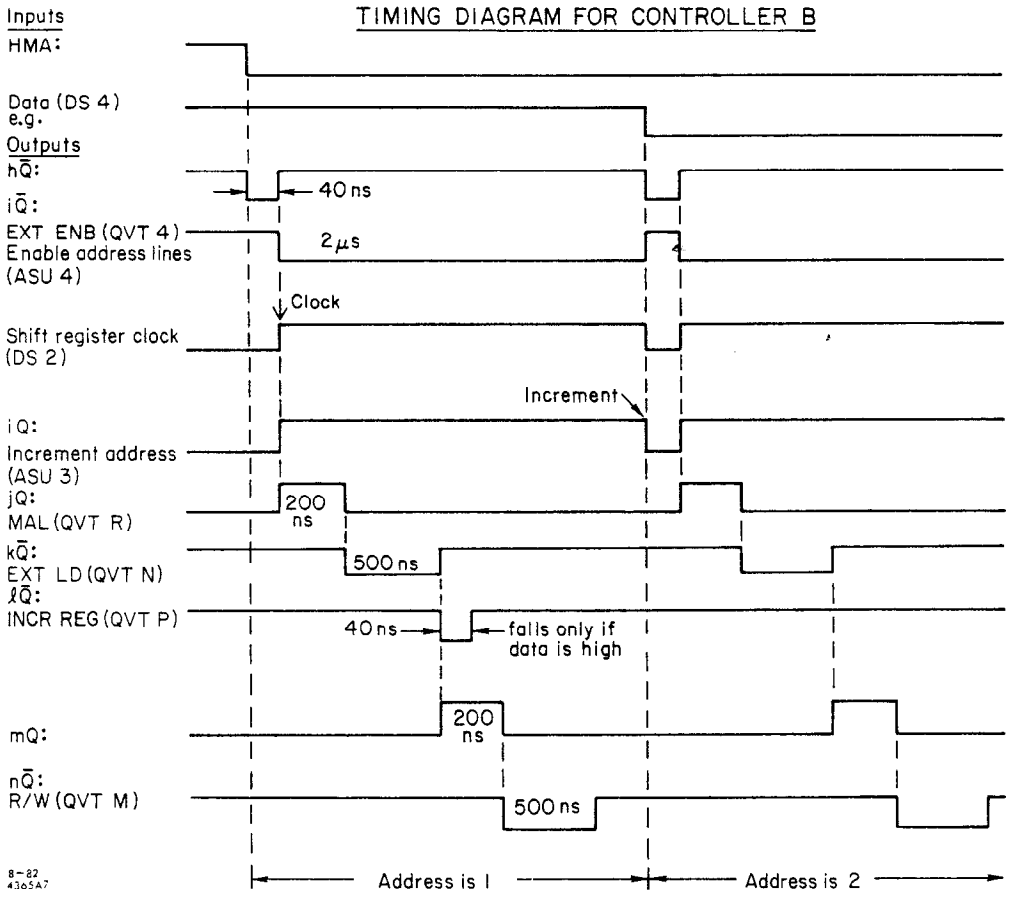

TIMING DIAGRAM FOR CONTROLLER B
Inputs
HMA:
Data (DS 4)
e.g.
Outputs
hQ̄:
iQ̄:
EXT ENB (QVT 4)
Enable address lines
(ASU 4)
Shift register clock
(DS 2)
iQ:
Increment address
(ASU 3)
jQ:
MAL (QVT R)
kQ̄:
EXT LD (QVT N)
lQ̄:
INCR REG (QVT P)
mQ:
nQ̄:
R/W (QVT M)
40 ns
2 μs
Clock
Increment
200 ns
500 ns
40 ns
falls only if data is high
200 ns
500 ns
8-82
4365A7
Address is 1
Address is 2

Fig. 7

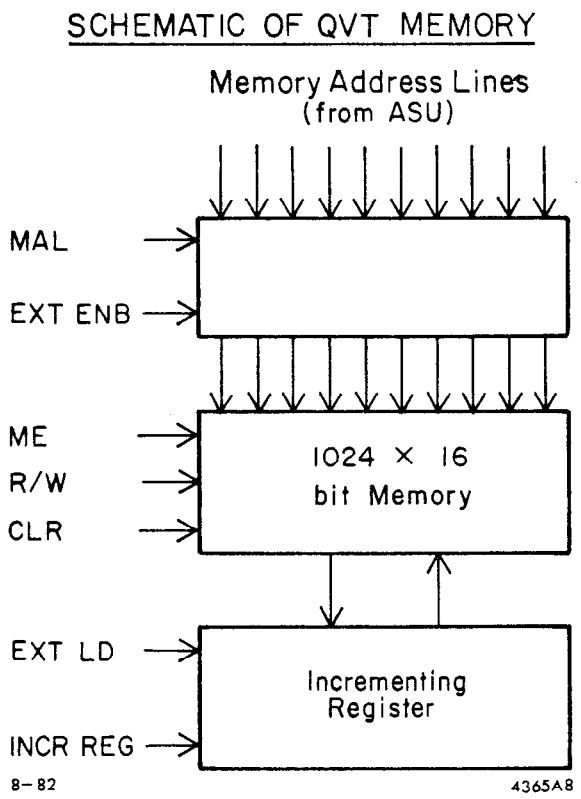
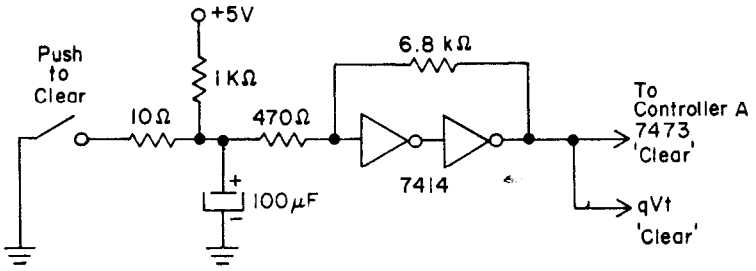

SCHEMATIC OF QVT MEMORY
Memory Address Lines
(from ASU)
MAL
EXT ENB
ME
R/W
CLR
1024 × 16
bit Memory
EXT LD
INCR REG
Incrementing
Register
8-82
4365A8

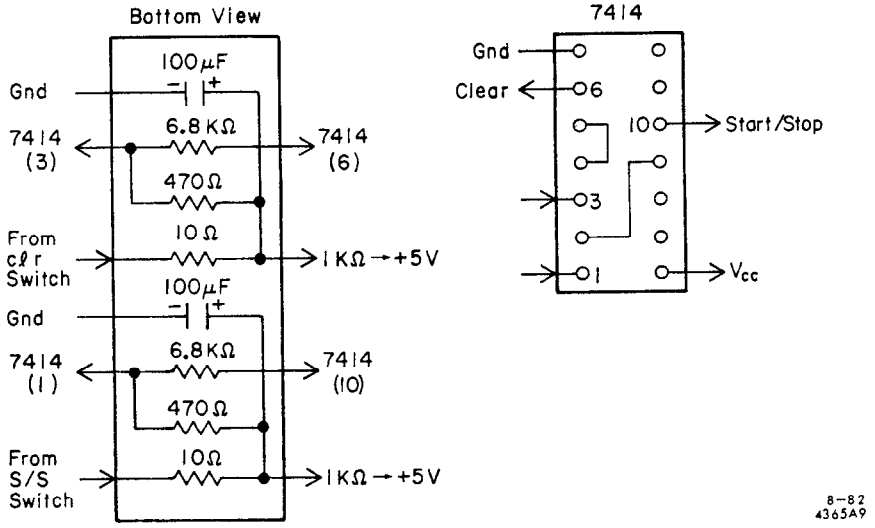
Fig. 8

PUSHBUTTON CIRCUITRY



Identical circuitry used for start/stop function, with output connected to Controller A 7473 'clock'.

CONNECTIONS



8-82
4365A9

Fig. 9