SLAC-PUB-2902
April 1982
(A)

A MICROPROCESSOR CONTROLLED PHASE MEASUREMENT SYSTEM FOR 2856 MHz PULSES*

J. D. Fox and H. Schwarz
Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

Abstract

A computer controlled phase detection system used to measure and stabilize the phase of high power RF pulses in the two mile Stanford Linear Accelerator has been developed. This system measures the phase of a 1 μsec 2856 MHz 50 MW RF pulse with respect to a CW reference signal at the same frequency at a 180 Hz rate with $<0.2^{\circ}$ resolution.

Introduction

This paper describes a phase measurement system designed to measure phase differences between pulsed RF signals and a CW phase stabilized reference line at 2856 MHz. This system utilizes remote detector heads physically close to the signals to be measured, and a CAMAC packaged signal processor module which analyses signals from up to eight remote detector heads. The design, construction, and operation of the detector head (including RF and reference line signals, mixer, and electronic stripline phase shifter) and the signal processing module are described. Basic software algorithms used in the signal processing microprocessor are described, as are the preliminary results indicating the resolution of the phase measurement.

The phase measurement uses a double balanced mixer as a nulling detector, and a voltage variable phase shifter in the signal path which is adjusted to null the mixer. If this null is achieved relative to an absolute phase reference, the nulling detector and voltage variable phase shifter can be used in a feedback system to maintain the original phase relationship between the signal and reference lines. Additionally, if the ϕ vs V characteristic of the phase shifter is known, an absolute measurement of the phase difference between signal and reference can be determined.

Figure 1 is a block diagram of the system and shows the relationships of the various components. The RF pulse to be measured is coupled out of the high power klystron waveguide used to drive the accelerator sections, and the CW reference signal is supplied through a phase stable reference line.

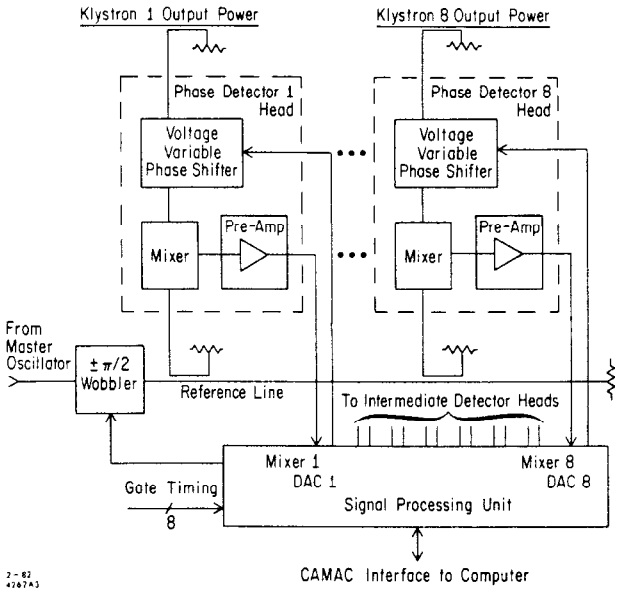

Fig. 1. System block diagram.

Principle of the Phase Measurement

The amplitude response of a double balanced mixer, given proper operating power levels, may be modeled as[1]

$$V_{out} = \alpha|\vec{R}|\left(\cos(\phi_s - \phi_r) + V_{offset}\right)$$

where

α = a linear response coefficient.

$|\vec{R}|$ = the magnitude of the reference voltage.

ϕ_s = the phase of the RF signal.

ϕ_r = the phase of the CW reference.

V_{offset} = a dc offset term.

Since V_{offset} is unique for each mixer, and is a function of temperature and power levels, the simple V_{out} is not an unambiguous measure of the phase difference. However, by taking the difference of two successive measurements and shifting the phase of the reference line by $\pm\pi/2$ radians between measurements, the unknown V_{offset} is subtracted out. Additionally, by forcing

$$V_{out}|_{+\pi} - V_{out}|_{-\pi} = 0$$

one can state that $\phi_s - \phi_r = \pm\pi/2$, or that the signal and reference signals have a fixed 90° relationship. The sign of the phase relationship can be determined by shifting the phase of the reference line by a few degrees in a known direction, and noting the algebraic sign of $V_{out}|_{+\pi} - V_{out}|_{-\pi}$.

Choice of Mixer and RF Signal Levels

To reduce possible phase errors, high isolation in the order of 40 dB between LO and RF ports of a mixer is required. Mixers meeting this requirements are commercially available.† The LO signal level is chosen large enough to saturate the mixer and this condition is independent of power levels over at least a 10 dB range. This allows some variation in the RF signal applied to the LO port without affecting the sensitivity of the phase detector. Since the high power RF pulse varies in amplitude over the 1 μsec pulse length and may vary from station to station it was chosen to supply the LO signal. The reference signal in turn can easily be provided with constant amplitude and when applied to the RF port of the mixer assures a constant sensitivity.

Functional Description-Phase Shifter

The electronic fast phase shifter uses varactor diodes in a parallel resonant circuit configuration. The reflection with variable phase from such a tuned resonant circuit is separated from the incident wave by using two resonant circuits as termination for two ports of a 4 port 3 dB hybrid. By proper selection of the capacitance value of the varactor diodes the phase shift versus control voltage can be made an almost linear function. This is possible due to the limited matching of two nonlinear functions: the capacitance change of the varactor diode with voltage

$$C_T = \frac{C_0}{(1 + V/\phi)^{\gamma}}$$

* Work supported by the Department of Energy, contract DE-AC03-76SF00515.

† Watkins Johnson, Type M1G, M63, etc.

(Presented at the 1982 IEEE MTT-S International Microwave Symposium, Dallas, Texas, June 15-17, 1982.)

(C_0... capacitance at 0 volts, ϕ... contact potential approximately 0.6 to 0.7 volts, γ... exponent approximately 0.47) and the change of phase with capacitance

$$\phi = -2 \arctan \frac{X}{Z_0}$$

with

$$X = -\frac{1}{\omega C_T} + \omega L$$

(Z_0... characteristic impedance of the transmission line, L... parallel inductance, ω... angular frequency of operation)[2].

Simple computer calculations were performed using the equivalent circuit in Fig. 2 to calculate the phase shift of the reflected signal versus the bias voltage. The parameters of available varactor diodes were used and a diode was selected with the most linear response for a 180° range. High Q diodes are essential to achieve reasonable insertion loss.

The circuit (Fig. 3) has been designed in stripline with the parallel inductance L represented by a line length somewhat larger than $\lambda/4$ terminated in an adjustable capacitance C_1. An additional pair of adjustable capacitances C_2 in front of the varactor diodes are added for fine tuning of linearity and total phase range. A low pass filter for bias input and series dc blocks C_3 are also provided.

Figure 4 shows the phase shift and insertion loss versus bias voltage. The maximum power level for the device with zero bias voltage is 50 mW, limited by the onset of forward conduction in the varactor diodes due to the RF voltage.

A more detailed description of this type phase shifter can be found in Ref. 3.

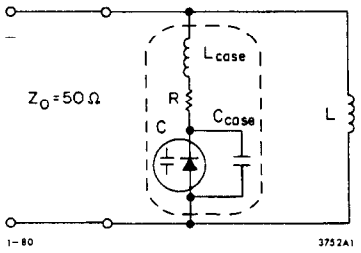

Fig. 2. Parallel resonance equivalent circuit.

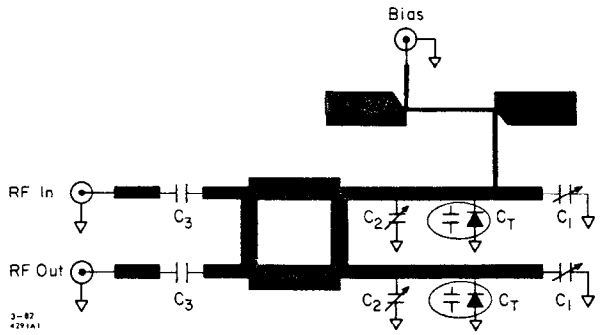

Fig. 3. Phase shifter stripline circuit.

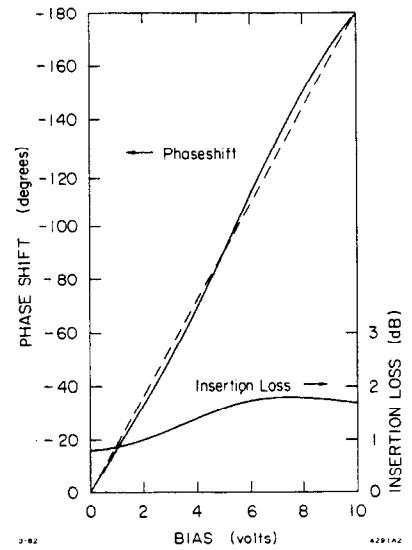

Fig. 4. Phase shifter performance.

Phase Wobbler and Reference Line

The $\pm\pi/2$ wobbler in its design and construction is very similar to the electronic phase shifter. It uses PIN diodes in the place of varactor diodes to switch between shorted and open circuit states. The open circuit condition is adjustable by variable capacitors so the device can be trimmed to produce zero or 180° phase shift. The wobbler is part of a 320 feet long reference line with eight outputs for eight detector locations. The reference line is temperature stabilized and electronically controlled in its electrical length. Details will be published in a later paper.

Functional Description - Signal Processor Module

The module may be functionally partitioned into analog signal processing components, digitization electronics, a microprocessor for digital signal processing and control functions, and a CAMAC interface. The module also includes drive circuitry for phase modulating the reference line $\pm\pi/2$ radians, and eight channels of 8-bit analog output for controlling eight voltage variable phase shifters.

Figure 5 is a block diagram of the analog circuitry. The signals from the eight mixer heads are amplified, filtered and sampled. Each mixer head has its own sample gate input, and each sample has a 100 ns sample width. These features allow phase vs time measurements to be made by varying the timing of the sample gates.

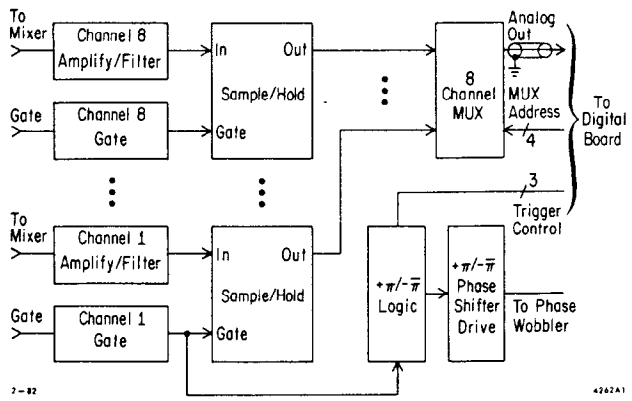

Fig. 5. Analog signal processing block diagram.

Figure 6 is a block diagram of the digital circuitry. The sampled analog signals are digitized and transferred to the microprocessor memory. A CAMAC loaded mode register specifies what operations are to be performed on the digitized data, and an appropriate output data block is formatted and written into the output data block RAM. The eight DAC channels are also noted in the diagram. Their values are set by the local processor, or by the external processor via CAMAC, as specified by the contents of the mode register.

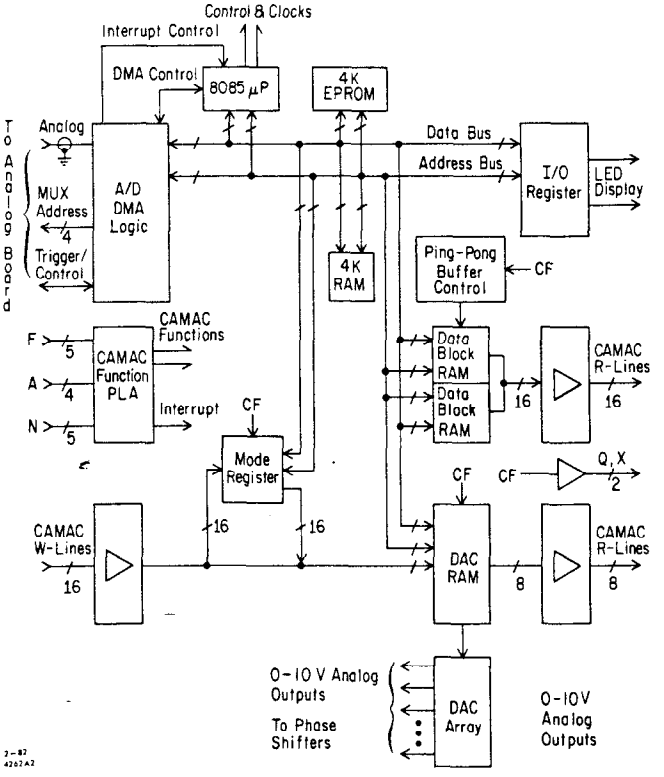

Fig. 6. Digital signal processing block diagram.

Software Description

The signals from the eight remote detector heads are sampled and digitized in the signal processing module. A computer program is executed by the system microprocessor to perform the operations of filtering, subtraction of a dc offset, and system control. A feedback algorithm is used to adjust the appropriate phase shifter to achieve a null difference, and the signal processor calculates a phase value using the voltage vs phase characteristic of the phase shifter. These calculated phase values are then formatted and transferred to the host control computer.

The feedback algorithm is of particular interest. The voltage variable phase shifters are controlled by eight-bit digital to analog converters which have a quantized phase adjustment of 0.6° per DAC unit ($180^\circ/2^8$), which might seem to imply a possible measurement resolution at null of ±0.6°. However, as the cosine function is essentially linear about zero, the microprocessor can interpolate between readings to measure the phase to much better than one DAC unit of phase. Additionally, since the phase shifter covers 180°, there are two possible zero crossings of the mixer output characteristic, and the algorithm must find the slope of the zero crossing and add 180° to the measured phase if appropriate.

At initialization, or after a discontinuous phase transient, the feedback loops are out of lock. A successive approximation algorithm is used to initially set the phase shifter control voltages to within one DAC unit of phase null. This algorithm takes eight measurement cycles (eight klystron pulses) and is necessary so that the mixer responses may be linearized about the zero crossing, and then the tracking algorithm is subsequently able to follow the phase characteristics with time and keep the feedback loops locked.

Once near zero, the tracking algorithm adjusts the phase shifter every pulse and attempts to alternate measurements about the zero crossing every other pulse. A Newton-Raphson algorithm is used to calculate the zero crossing of the phase characteristic, and for each two measurements the zero phase voltage is calculated as

$$V_{zero} = \frac{\big(DAC(J+\delta) - DAC(J)\big) * V_s\big(DAC(J)\big)}{V_s\big(DAC(J)\big) - V_s\big(DAC(J+\delta)\big)}$$

Figure 7 illustrates this interpolation. The phase vs voltage characteristic of the phase shifter is then used to convert the V_{zero} to a phase measurement. The possible 180° offset is added if

$$V_s\big(DAC(J)\big) - V_s\big(DAC(J+\delta)\big) < 0$$

The tracking algorithm sets the phase shifter control DAC to the closest value near V_{zero} and thus tracks time varying phases. If a loop loses lock, as indicated by the magnitude of the difference between the calculated V_{zero} and the present setting of the control DAC, the successive approximation code is re-executed, and the tracking code re-closes the feedback loop.

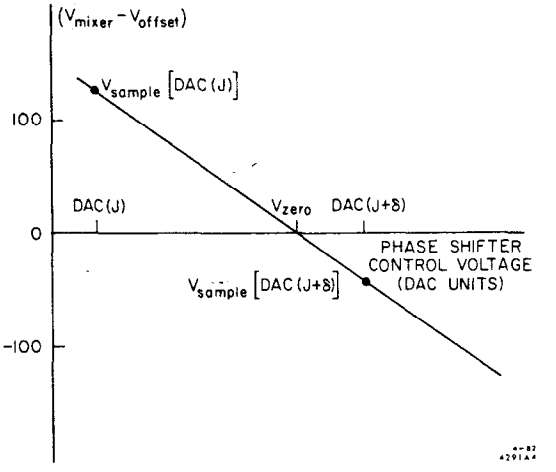

Fig. 7. Interpolation of V_{zero}.

Measured System Performance

The prototype mixer head (with phase shifter, mixer, and signal preamplifier) and prototype signal processing module have been fabricated, and the prototype system software has been developed. As of this writing, the assembled measurement system successfully measures 1 μs 2856 MHz RF pulses at a 180 Hz repetition rate with <0.2° resolution under laboratory conditions. Field testing of this prototype is underway, and the final system performance and final system specifications will be reported at the June 1982 MTT conference.

Acknowledgements

The authors wish to thank Matt Allen, Bob Melen, and Rae Stiening for their support and Bill Roster for his technical contributions. Contributions by Yong-xiang Zhao in all stages of the development are much appreciated.

References

1. S. R. Kurtz, "Mixers as Phase Detectors," Watkins-Johnson Company, Palo Alto, California.
2. R. V. Garver, "360° Varactor Linear Phase Modulator," IEEE MIT-17, No. 3, March 1969, pp. 137-147.
3. H. Schwarz, "Linear Electronic Phase-Shifter Design," SLAC-PEP-NOTE-283, November 1979.