MODULES AND SUPPORTING HARDWARE FOR FASTBUS TEST AND DIAGNOSTIC PURPOSES*

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ABSTRACT

This paper contains detailed descriptions and circuitry of some modules and supporting hardware for the FASTBUS System developed at SLAC. A fast slave-only Memory Module ("PRIMO"), a Dummy Module ("U2"), a FASTBUS Test Box ("LAIKA"), and a Bus Display Bar ("BBD") have been built, tested and used for test and diagnostic purposes for FASTBUS.

INTRODUCTION

The electronics described in this paper were designed to support the FASTBUS prototype program at SLAC. A general description of the Memory Module can be found in "Design of a FASTBUS Programmable Sequencer Module and Memory Module," discussion of the running performance can be found in "A FASTBUS Demonstration System," both in this same journal.

This paper will then be more concerned with detailed comments on the design of the Memory Module, and general description of the remaining three modules.

It should be noted, however, that since these modules were designed and built some changes in the protocol have been made. These changes, when appropriate, will be pointed out in the paper.

MEMORY MODULE ("PRIMO")

The Memory Module is a slave module that performs all the appropriate FASTBUS protocol functions. Two separate buses (IN and OUT) on the AD lines are used, with positive logic implementation. Originally two other configurations (a single bidirectional bus and a negative internal logic bus) were taken into consideration; however the one implemented was found easier to design from a hardware point of view, faster in speed, and requiring fewer IC's to be used.

Separate Parity circuits are used on the IN-BUS (Parity Check) and OUT-BUS (Parity Generate). Although only one circuit can be used (on the IN-BUS) for both Parity Check and Generate, two separate circuits are used to gain speed and to prevent any ambiguity during a read cycle when Parity is Generated.
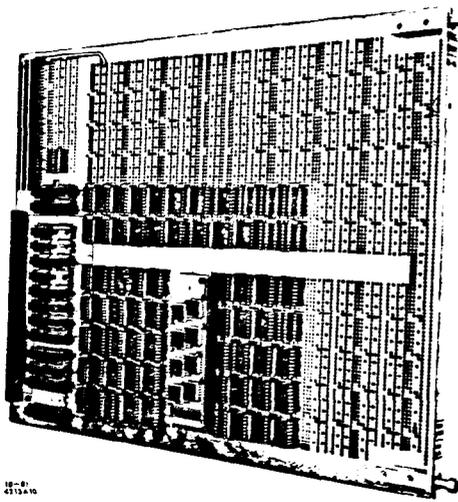
A high order bit (AD16-31) Zero Detector on the IN-BUS was needed for logical address Identification (see Format on Fig. 2). With the new protocol this has been removed, since the Module Address expands in the Group Address field.

The Memory Module use two separate registers to store the IA part of the Address, each one strictly related to its own space: the one in Data space is called MAR (Memory Address Register) and the one in Control Space is called PAR (Pointed Address Register). The use of two separate registers instead of one (NTA) was found interesting in order to give the two spaces complete symmetry, save at least one register, and simplify the hardware for block transfer implementation. The only drawback is that the content of these registers may be lost with the next Address cycle according to the protocol. This problem was solved as will be seen later.
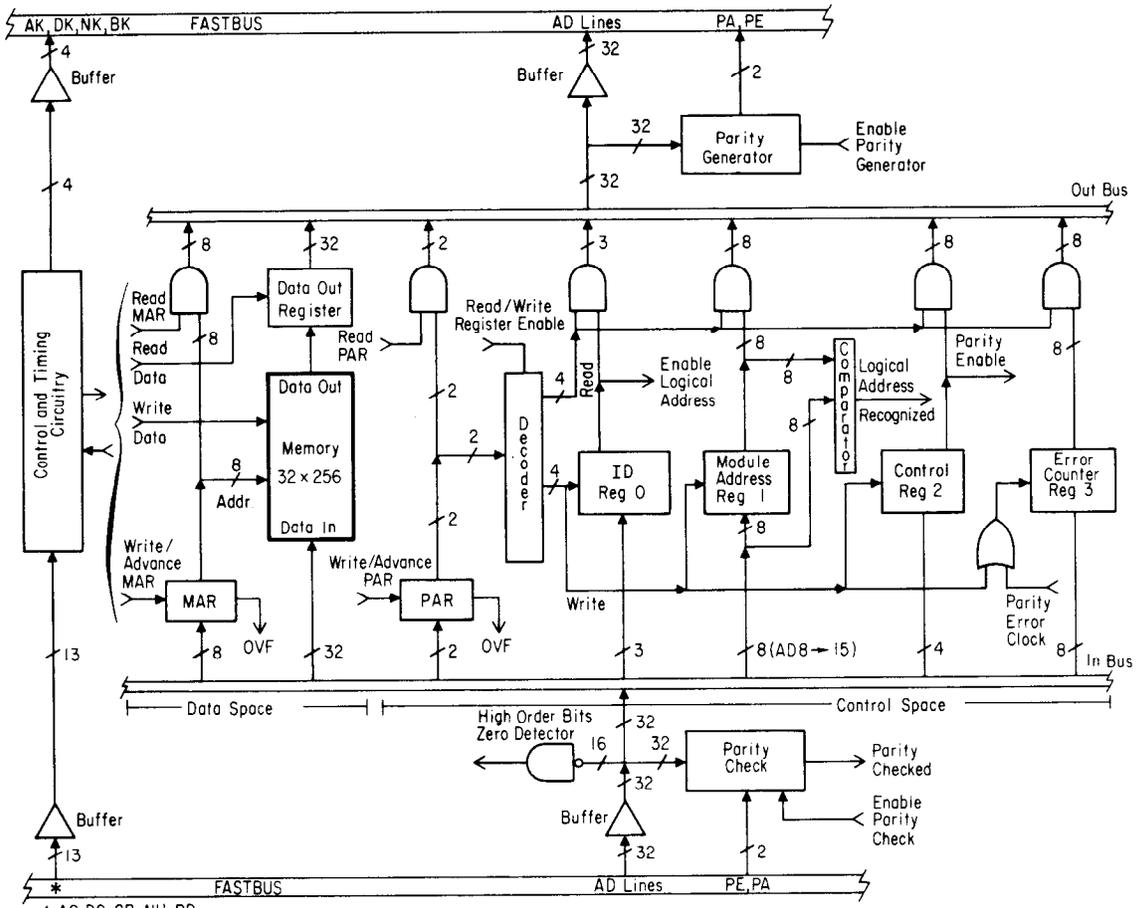
The Memory Module uses both Data and Control Space, the two spaces being completely symmetric: i.e., two cycle operation (Address – Data) or three cycle operation (Address – Extended Address – Data) are possible in both spaces. From Fig. 1 this symmetry can be seen where PAR in Control Space replaces MAR in Data space, and the four registers plus the address decoder replace the Memory. The only difference here is in the Read-Out Circuitry. In control space, AND gates controlled by the read lines from the decoder are used due to the fact that Block Transfer in Control Space was not of much interest at this stage; while in Data space the use of a Data Out Register was necessary in order to achieve proper timing in block transfer. From Fig. 3 it can be seen that without this Register during Block-Transfer Hand-Shake Read cycle it is necessary to skip the first clock pulse in order to preserve the data on the AD lines until DS changes, then the MAR should be advanced on the leading edge (corresponding to a DS transition) of the clock pulse, while in a write cycle the MAR is advanced on the trailing edge of the same pulse (the leading edge has been used to write into the memory). The use of the Out-Register removes this timing oddity. The leading edge of the pulse is now used to strobe the Data into the register while the trailing edge advances the MAR in conformity with the write cycle.

The Memory Module can be addressed in all three modes: Georgraphical, Logical and Broadcast, in accordance with the Work Format of Fig. 2. The implementation is shown in Fig. 4. The following features should be noted: the status of the control lines CB and NH (in the new protocol called respectively CL0 and CL1) at Address Time should be preserved and therefore is stored in registers, fixing for the entire operation the space to be accessed in the later cycles. During Geographic addressing bit 7 of the AD lines controls the automatic reset of the IA registers, so that information contained in the MAR or PAR is not lost, if so desired. The same result can be achieved in Logical Addressing with bit 3 (NLD) of Control Register (Reg. 2) in Control Space.

Figure 5 shows the implementation of the AS-AK lock and the DS-DK response. The double path on the DS-DK response (Normal and Delayed) is to speed up the response during normal operation, due to the fact that extra time delay is involved during a read cycle with Parity Generation (the extra delay is 10 nsec).

Figure 6 shows the schematic and timing diagram of the clock generation for the IA's. Of particular interest is the use of the double edge triggered One-

Fig. 1. Block Diagram.

AK,DK,NK,BK   FASTBUS   AD Lines   PA,PE

Buffer — 4

Buffer — 32

Parity Generator — Enable Parity Generator

Out Bus

Control and Timing Circuitry

Read MAR
Read Data
Write Data
Write/Advance MAR

Data Out Register
Read PAR
Data Out
Memory 32 × 256
Data In
Addr

Read/Write Register Enable

Decoder

Read
Enable Logical Address

ID Reg 0
Module Address Reg 1
Comparator — Logical Address / Recognized
Control Reg 2
Error Counter Reg 3

Parity Enable

Write/Advance PAR
MAR — OVF
PAR — OVF

Write

Parity Error Clock

In Bus

Data Space   Control Space

High Order Bits Zero Detector

Parity Check — Parity Checked — Enable Parity Check

Buffer

Buffer — 13

FASTBUS   AD Lines   PE,PA

* AS, DS, CB, NH, RD, WT, RB, EG, GA 4 → 0

Fig. 2. Word Format.

Addressing

Logical in Data Space: 31 ← Zeroes → 16 | 15 ← Module Address → 8 | 7 ← IA (MAR) → 0

Logical in Control Space: 31 ← Zeroes → 16 | 15 ← Module Address → 8 | 1 0   IA (PAR)

Geographical: 7 6 5 | 4 ← GA → 0
"0"=Reset/"1"=Don't Reset IA's @ Add. Time   Zero

Broadcast: 0
"1" with NH=1 @ Add. Time

Registers in Control Space

Extended Address ← ID# = 1010 X →

I.D. Reg 0: 31 | 17 | 8 | 1 0
Disable Logical Add.   Enable Logic Add.   Reset

Module Add Reg 1: 15 ← → 8

Control Reg 2: 3 2 1 0
No Load IA @ Add. Time / Parity Check / Parity Gen. / Error Counter — Enable

Parity Error Counter 3: 7 ← → 0

WORD FORMAT

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Fig. 3. Block Transfer.
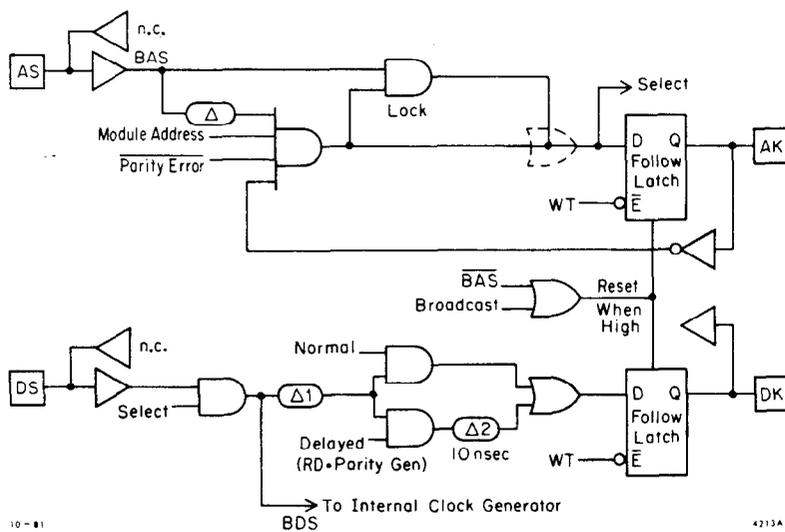

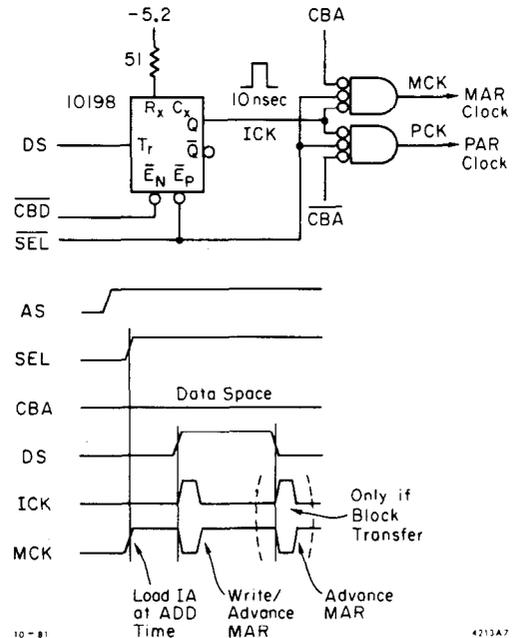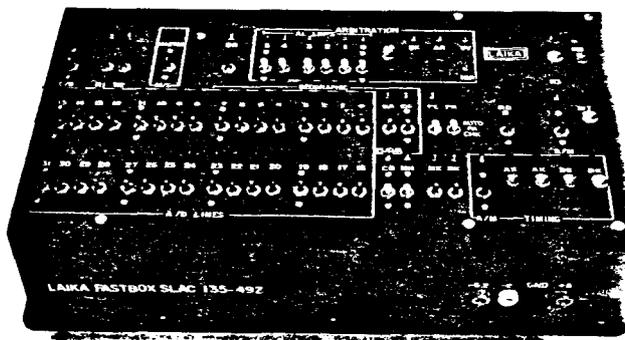Fig. 4. Addressing.

Fig. 5. Timing.

Fig. 6. Clock Generator.

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shot (MC10198). On normal operations only the positive edge control input is activated by the Select line, but in block transfer both edge control inputs are activated respectively by the Select line and CBD (control line CB at data time).

FASTBUS TESTBOX (OR FASTBOX - "LAIKA")
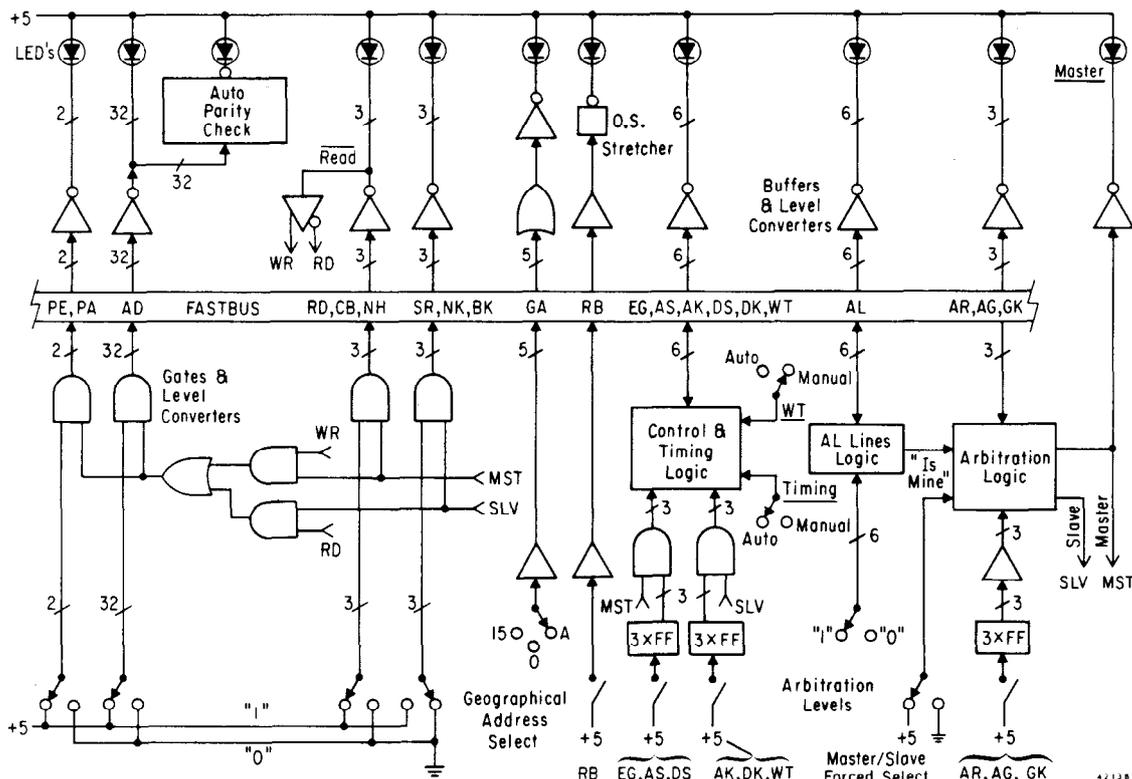

"LAIKA" FASTBOX

Fig. 7.

This FASTBOX (Fig. 7) is a mannual tester for all FASTBUS devices: Masters, Slaves, and ATC's. It can be used for a single module test (on the bench) or for test of multiple modules in a crate via a flat FASTBUS cable. It generates all of the FASTBUS signals via switches or pushbuttons and reads the state of the bus lines with LED's.

The FASTBOX can be a Master or a Slave, depending on the module under test, and can also perform as an ATC, to test the arbitration logic of a Master or an ATC unit.

An Automatic Parity Check circuit internally generates the parity to be checked against the PA light (if PE is enabled). If the two lights agree, parity is correct, if they disagree, it is incorrect.

An Automatic/Manual switch on the WT line allows WT to be set/reset manually with the WT pushbutton or

automatically set with AS and DS and reset with AK and DK. The automatic set/reset of the WT line is necessary when testing a Master in order to disable the "time-out" timer. The WT pushbutton is however never disabled, so the WT signal on the Bus can always be reversed by the use of the WT pushbutton.

Via an Automatic/Mannual Switch on the timing signals (AS, AK, DS, DK) the FASTBOX can also simulate block transfers.

The A/D, PE and PA switches are active during READ when it is a SLAVE or during WRITE when it is a MASTER. RD, CB, NH, EG switches and AS, DS pushbuttons are active only when it is a MASTER. SR, NK, BK switches and AK, DK pushbuttons are active only when it is a SLAVE.

The FASTBOX was instrumental in debugging the Memory Module and other modules built at SLAC.

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DUMMY MODULE ("U-2")   FASTBUS DISPLAY BAR ("BBD")

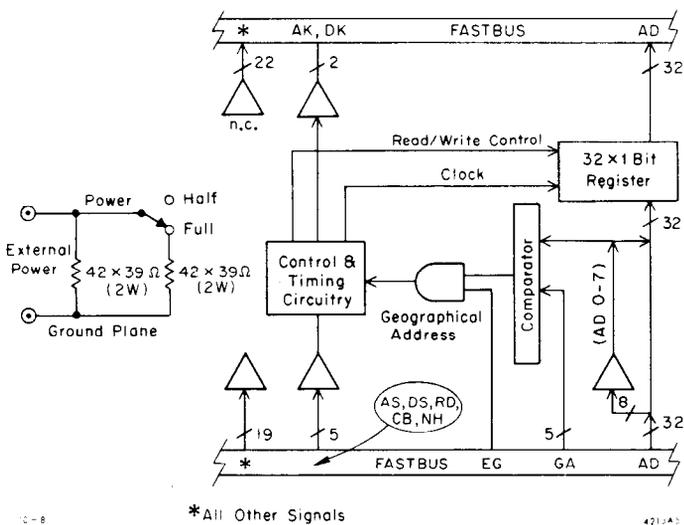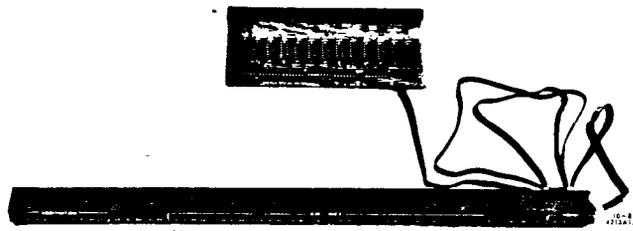BBD FASTBUS DISPLAY BAR
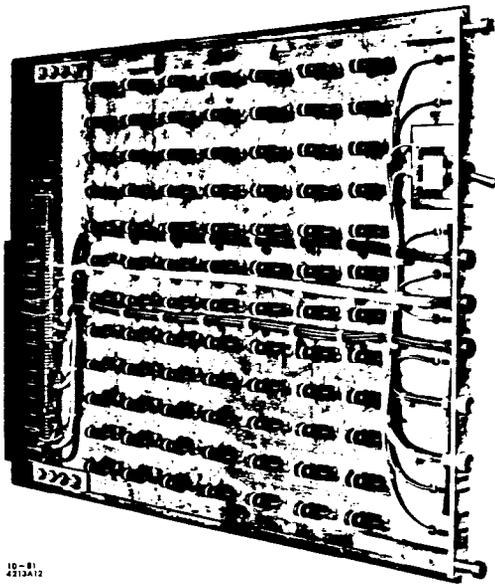
U2 DUMMY MODULE

Fig. 8.

Fig. 9.

This module (Fig. 8) is a very simple FASTBUS module limited to geographical addressing capability and one Read/Write 32 bit register. It has dummy heat loads for heat test simulation.

By filling a FASTBUS crate with 25 of these modules, two major tests can be performed: signal propagation test of the fully loaded FASTBUS backplane and power heat dissipation test, at full load.

This is a two-part system (Fig. 9): a PC card (Driver) connected directly on the bus on the rear of the FASTBUS crate, and a long thin PC card (Display) attached on the front top of the crate itself. The Driver samples the status of the bus with a 60 Hz clock and serially transmits the data to the Display at a bit rate of 1 MHz, where the data are stored in a 56 bit shift register and displayed on the LED's. It serves mainly as a diagnostic tool.