SLAC-PUB-2832
October 1981
(E/A)

STATUS AND FUTURE OF FASTBUS*

R. S. Larsen
Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

ABSTRACT

This paper primarily focuses on developments which are needed to make FASTBUS a viable option for future experiments and control systems. The basic tools available or under development are discussed.

BACKGROUND

FASTBUS is a standard data bus which has been under study since 1976, and under a development program supported by the U.S. Department of Energy since 1977. The principal goal of the original program was to develop a data bus, optimized for high speed data acquisition, which would accommodate the anticipated needs of the 1980's and beyond. The principal requirements perceived at the inception of FASTBUS were threefold:

(1) To accommodate system data throughputs of about an order of magnitude greater than systems in current use;

(2) To accommodate distributed intelligence, particularly in the form of multiple microprocessors and special purpose microcomputers, and

(3) To provide system interconnection devices and standard software for system initialization and diagnostics.

The status of development has been reported upon at each prior Nuclear Science Symposium since 1977. The purpose of this paper is to briefly review the characteristics of FASTBUS, recent progress toward finalization of the specification, and anticipated future directions. The paper will mention primarily developments in the U.S., since a separate paper at this Conference will cover European developments.

CHARACTERISTICS OF FASTBUS

The FASTBUS data bus can perhaps be most easily summarized by reference to a list of signal lines (Table 1). This table shows the various lines by name and classification. A more detailed picture is given by reference to the pin-outs of a typical module station (Table 2). This table shows the order of pins as seen on the standard connector as viewed from the front of a crate. The main features of note are, in summary:

Bidirectional Multiplexed address/data lines (AD)
Handshake timing control lines (AS,AK,DS,DK)
Control and status lines (CL,SS,WT,SR,RB,BH)
Geographic address lines and control (GA,EG)
Arbitration level and control lines (AL,AR,AG,AI,GK)
Parity (PA,PE)
Serial diagnostic lines (TX,RX)
Special lines (TP,DL,DR)
Reserved lines (R)

The description and functions of all these lines have been adequately covered in previous papers and in the draft specification (1). In this paper, only recent changes will be reviewed.

The main FASTBUS characteristics of note are:

a. The protocol allows any master to address any other device in the entire address field--i.e., each device has a unique system address.

TABLE 1. FASTBUS Signals

Mnemonic	Signal Name	Use*	No.	Comments
AS	Address Sync	T/C	1	for addressing and reporting status of connection
AL	Address Acknowledge	T/C		
EG	Enable Geographical	C	1	
CL	Control Line	C	3	for data and control of data transfers
RD	Read	C	1	
AD	Address/Data	I	32	
PA	Parity	I	1	
PE	Parity Enable	I/C	1	
SS	Slave Status	I	3	
DS	Data Sync	T	1	
DK	Data Acknowledge	T	1	
WT	Wait	I/C	1	
SR	Service Request	I	1	
RB	Reset Bus	C	1	
BH	Bus Halted	C	1	
AG	Arbitration Grant	T	1	for bus arbitration
AL	Arbitration Vector	I	1	
AR	Arbitration Request	C	1	
AI	Arbitration Request Inhibit	C	1	
GK	Grant Acknowledge	T	1	
			60	
TX	Serial Line Transmit	I/C	1	for diagnostics (not on CABLE SEGMENT)
RX	Serial Line Receive		1	
GA	Geographical Address Pins (position encoded, not bussed) - simulated on CABLE SEGMENT	I	5	CRATE SEGMENT only
TP	T-Pin (not bussed)		1	
DL	Daisy Chain Left		3	
DR	Daisy Chain Right		3	
R	Reserved		24	

* T = Timing, C = Control, I = Information

b. The total system address space is accessible both as data space and as control/status space. Control/status space is usually accessed by a three cycle operation.

c. Certain basic control/status registers are standardized in order to make possible uniform software.

d. Arbitration logic (plug-in card) on the backplane and on each master provides a mechanism for sharing the bus. This logic is very high speed ECL logic to minimize arbitration time.

e. Geographical addressing allows independent access to any device via a hard-wired address depending upon module location. This is invaluable for initialization and diagnostics.

f. A serial diagnostic network is provided to allow independent access for troubleshooting. This bussed network works into any device provided with a serial network communications capability, and particularly into a diagnostic module known as a "Snoop."

* Work supported by the Department of Energy, contract DE-AC03-76SF00515.

Invited talk presented at the Nuclear Science Symposium, San Francisco, CA, October 21 - 23, 1981.

TABLE II. Segment Connector Pin Assignments Arranged in order of pin number as viewed from front of crate

Pin No.	Mnemonic	Function	Pin No.	Mnemonic	Function
1	0V	Digital voltage return	2	0V	Digital voltage return
3	+28V	+28 volt bus	4	AL00	Arbitration Level 0
5	+28V	+28 volt bus	6	AL01	Arbitration Level 1
7	+15V	+15 volt bus	8	AL02	Arbitration Level 2
9	-15V	-15 volt bus	10	0V	Digital voltage return
11	0VA	Analog voltage	12	AL03	Arbitration Level 3
13	-5.2V	-5.2 volt bus	14	AL04	Arbitration Level 4
15	-5.2V	-5.2 volt bus	16	AL05	Arbitration Level 5
17	-5.2V	-5.2 volt bus	18	AR	Arbitation Request
19	AG	Arbitration/Grant	20	0V	Digital voltage return
21	AI	Arbitration Inhibit	22	GK	Grant Acknowledge
23	SS0	Slave Status 0	24	DK	Data Acknowledge
25	-2.0V	-2.0 volt bus	26	AD	Address Acknowledge
27	+5.0V	+5.0 volt bus	28	WT	Wait
29	+5.0V	+5.0 volt bus	30	0V	Digital voltage return
31	SS1	Slave Status 1	32	AS	Address Sync
33*	SS2	Slave Status 2	34	DS	Data Sync
35	RD	Read	36	CL0	Control Line 0
37*	CL2	Control Line 2	38	CL1	Control Line 1
39*	R39	Reserved	40	0V	Digital voltage return
41	EG	Enable Geog. Address	42	AD00	Address/Data,LSB
43	+5.0V	+5.0 volt bus	44	AD01	Address/Data
45	SR	Service Request	46	AD02	Address/Data
47*	RB	Reset Bus	48	AD03	Address/Data
49*	BH	Bus Halted	50	0V	Digital voltage return
51	R51	Reserved	52	AD04	Address/Data
53	GA00	Geographical Address 0	54	AD05	Address/Data
55	GA01	Geographical Address 1	56	AD06	Address/Data
57	GA02	Geographical Address 2	58	AD07	Address/Data
59	GA03	Geographical Address 3	60	0V	Digital voltage return
61	GA04	Geographical Address 4	62	AD08	Address/Data
63	-2.0V	-2.0 volt bus	64	AD09	Address/Data
65**	DLA	Daisy Chain In Left	66	AD10	Address/Data
67**	DRA	Daisy Chain Out Right	68	AD11	Address/Data
69**	DLB	Daisy Chain In Left	70	0V	Digital voltage return
71**	DRB	Daisy Chain Out Right	72	AD12	Address/Data
73	DAR	Daisy Chain A Return	74	AD13	Address/Data
75	DBR	Daisy Chain B Return	76	AD14	Address/Data
77	R77	Reserved	78	AD15	Address/Data
79	R79	Reserved	80	0V	Digital voltage return
81	R81	Reserved	82	TP	T pin
83	-5.2V	-5.2 volt bus	84	R84	Reserved
85	R85	Reserved	86	PE	Parity Enable
87	R87	Reserved	88	PA	Parity
89	R89	Reserved	90	0V	Digital voltage return
91	R91	Reserved	92	AD16	Address/Data
93	R93	Reserved	94	AD17	Address/Data
95	R95	Reserved	96	AD18	Address/Data
97	R97	Reserved	98	AD19	Address/Data
99	R99	Reserved	100	0v	Digital voltage return
101	R101	Reserved	102	AD20	Address/Data
103	+5.0V	+5.0 volt bus	104	AD21	Address/Data
105	R105	Reserved	106	AD22	Address/Data
107	R107	Reserved	108	AD24	Address/Data
109	R109	Reserved	110	0V	Digital voltage return
111	R111	Reserved	112	AD25	Address/Data
113	TX	Transmit Serial	114	AD26	Address/Data
115	RX	Receive Serial	116	AD27	Address/Data
117	-5.2V	-5.2 volt bus	118	AD28	Address/Data
119	-5.2V	-5.2 volt bus	120	0V	Digital voltage return
121	-5.2V	-5.2 volt bus	122	AD29	Address/Data
123	-2V	-2 volt bus	124	AD30	Address/Data
125	+5.0V	+5.0 volt bus	126	AD31	Address/Data
127	+5.0V	+5.0 volt bus	128	AD32	Address/Data
129	0V	Digital voltage return	130	0V	Digital voltage return

* Until October 20, 1981 these pins may be used as follows for special protocol for prototype purposes: Pin 33 - broadcast, pin37 - RB, pin 39 - BH, pin47 - control register, pin49 - block transfer.

** Devices shall short DLA to DRA and DLV to DRB if not used.

g. Interconnecting modules and cables (Segment Interconnect and Cable Segment) are provided to interconnect collections of crates, or remote devices having only Cable Segment connectors.

h. Special lines are provided to perform special modes of high-speed data acquisition (e.g., "T" pin, daisy chain lines). The T pin can be used to retrieve a summary pattern for interrupt servicing, for example.

i. The main bus is designed as a collection of terminated high speed transmission lines ($Z_o \approx 82\Omega$, loaded) in order to accommodate the fastest available logic families. However, since the entire system normally operates asynchronously, very slow speed devices are also quite naturally accommodated. (Synchronous operation, e.g., nonhandshake block transfer mode, is also provided for at the discretion of the controlling master device).

j. A variety of power lines is provided (+5,-5.2, -2,±15V). In addition, a pair of 28V lines allows power for on-board regulators and other special needs. Separate analog and digital returns are provided.

k. The crate hardware is modular so that systems can be customized for various cooling and power supply schemes.

l. It is planned to design custom IC's for the bus interface as well as for master and slave control logic. These will hopefully exist in both ECL-ECL and ECL-TTL format.

RECENT CHANGES IN THE SPECIFICATION

Experience gained during the prototype development program over the past year, and continued review by the various working groups, ahve resulted in some changes, most of a relatively minor nature; those are summarized briefly as follows.

a. Control/Status Lines. The nomenclature and number of control and status lines has been changed as follows:

Control: CB,NH → CL <2:0>
Status: NK,BK → SS <2:0>

The old control functions are unchanged, but a larger range of control definitions is now possible for future use. The slave responses are redefined as follows:

SS = 0	Valid address and data
1	Retry
2	End of tranfer
3	Error
4	Requested cycle impossible
5	Nonstandard
6	Nonstandard
7	Faulty data

b. Pinouts. Since the last issue of the draft specification, some problems were experienced in laying out PC boards due to the requirment for very short stub lengths to/from the bus. Therefore some pins were rearranged. This was done in such a way that the existing design of the backplane was not affected, except for labeling.

c. Daisy-Chains. An additional return line was added for each daisy chain; the two sets were relabeled as left in/out (A), right in/out (B), and return (A and B).

d. Arbitration Inhibit (AI). The old VV signal (valid vector) was deleted and replaced by AI, which is generated by the arbitration timing control logic on a segment to indicate the presence of unsatisfied requests. It is now recommended that masters be allowed to raise a request (AR) only when AI = 0. This is a fairness mechanism which, if used, precludes the highest priority master from hogging the bus indefinitely.

e. Bus Connectors. The earlier specification showed two possible 130-pin bus connectors, a box-and-header type and a brush type. It has now been agreed that the standard connector for all module and crate designs shall be the box-and-header type (i.e., staked pin backplane). An example is the AMP 87729-1 (block).

f. Auxiliary Connector. The use of an auxiliary connector is optional. The two or three rows of 44-pins conforming to the same mechanical dimensions as the bus connector, are preferred. Backplanes may be ordered or constructed with or without auxiliaries in place, or with only some of the pins in place, at the discretion of the user.

g. Module Circuit Board Dimensions. Previous issues of the specification showed two circuit boards, for various cooling schemes, with slightly different dimensions. These have been resolved into a single circuit board design.

h. Crates, Module Pitch, and Cooling. The draft specification describes crates with different module pitches of 20 and 26 per crate, and different cooling mechanics. The current goal is to design a common set of module specifications, including front panel, which would be independent of the crate design. This effort seems to be converging, and it is hoped that the final specification will be completely unambiguous insofar as the module itself is concerned. The approach under study is to use either clip-type heat sinks against a cold plate, or air cooling; thus the basic module mechanics should remain independent of the crate. It appears that the end user will have to decide between various cooling and crate mechanics. The use of a cold plate will place some restrictions on component height on every module, but this seems workable.

i. Specification. The draft specification has been edited twice in the pst six months and all of the above changes have now been entered. A new draft specification will be issued after the October Fast System Design Group (FSDG) meetings, and work will begin on the formal document for final publication.

PROTOTYPE DEVELOPMENT PROGRAM

At the outset of the FASTBUS design it was decided to begin an R & D program to test the FASTBUS concepts as thoroughly as possible prior to finalization of the specification. This effort has been continuing. Although the program has not progressed as rapidly as originally intended, some significant milestones have been reached or are close at hand. The following is a brief summary.

a. Prototype Hardware Tests. The concept of a single segment followed by multiple segment hardware tests has been outlined in previous reports. During the past year, a FASTBUS segment (crate) has been tested using a high-speed sequencer and memory module combination. The system was loaded from a programmed I/O (slow) interface connected to an LSI-11 microcomputer development system. The backplane was equipped with arbitration control circuitry. The test successfully demonstrated the basic handshake protocol functions and arbitration functions, and confirmed the basic performance of the backplane itself. These tests can be viewed at a demonstration poster paper at this conference.[2] Some of the test units are described in separate papers.[3,4]

b. Crate Hardware. A total of 50 type A crates have been received and distributed to various users for prototype programs. The users include SLAC,LASL,BNL, U. of Illinois, FNAL, SIN, DESY, CERN, TRIUMF, Northwestern, NBS, NIKHEF, and LeCroy. Additionally, the JWC corpporation of Union, Oregon, has produced a completely new crate and backplane design, which is now commercially available. BNL is building and ordering their own Type W design.

c. Miscellaneous Hardware. The I/O interface, ATC, EG and extender cards have been build at SLAC and made available to other labs. The ATC logic is due in quantity (U. of Illinois) very shortly. The EG card is

in small quantity production and some copies will be available shortly for those who have requested them (SLAC).

d. Diagnostic System. The Snoop module,[5,6] after many iterations and revisions, has been layed out and is now being digitized. The layout work is a U. of Illinois/SLAC collaboration. The first copy of this board is 8-10 weeks way. The Snoop contains, in addition to the fast front-end silo, a 68000 microprocessor and a FASTBUS master capability. Thus it can operate both via the slow serial network which emulates Ehernet, as well as over the FASTBUS segment, so as to be able to perform powerful diagnostics within a given crate regardless of the condition of the bus.

The Snoop development is accompanied by the development of a diagnostic software package, based on a multi-tasking version of FORTH. This software effort has made excellent progress and is essentially awaiting fabrication of several 68000 processor test boards in order to conduct initial tests. The first of these boards should be available by the time of this Symposium. The three boards will allow simulation of a 3-Snoop system while awaiting the availability of the full Snoop device.

e. Segment Interconect (SI), CABLE SEGMENT (CS) AND MULTISEGMENT TESTS. The key to making multisegment tests is to have available a segment interconect (SI). The SI and CS are described in a paper at this Conference.[7] The SI has been designed and is ready for wire-wrapping; unfortunately, it was delayed somewhat because of problems in getting a new kluge board fabricated. This new board (complete with 18,500 holes!) is modeled after an earlier U. of Illinois design; it contains a very convenient power bussing arrangement which allows excellent flexibility in prototyping. It is a 4-layer board, eight of which have now been built. Therefore, the SI construction should now proceed quite rapidly.

Another factor impacting the SI design is that of the Cable Segment (CS), since the SI is designed to communicate over a CS. This effort has encountered several obstacles, in particular the clean handling of arbitration signals. CERN has contributed significantly to arriving at a reasonable prototype design, which will hopefully be complete at the time of presentation of this paper.

Beyond the availability of this hardware, the multisegment demonstration involving at least two crates will require some new test software. There are two levels of software required:

(1) An extension of existing LSI-11 test software to load the SI(s) as well as the test sequencer(s), and to initialize a test operation. This level will include (hopefully) some implementation of the Snoop diagnostic hardware and software, although this is essentially an independent effort.

(2) Implementation of the more general System Initialization software, primarily as a second state test of the software. This software is in a primitive state at the moment, having been tested only in simulation, and needs the additions of various driver packages to make these tests on real hardware.

f. Further Tests Using Full Computer Interface. Early in the development proposal it was stated that a goal was to develop a functional computer interface to test the FASTBUS using a larger minicomputer. The first such interface under design is the Unibus Processor Interface (UPI) being designed at FNAL. This device is nearing completion and should be available for viewing as part of the aforementioned demonstration poster paper.[2]

It is felt that these tests will be mostly a test of the interface itself and of the efficiency of the concurrent software, as well as perhaps a measure of the software problem of interfacing to FASTBUS. The basic capabilities of FASTBUS, to support multiple masters in a distributed system, will be demonstrated on a small scale by the earlier tests. The testing of large arrays of FASTBUS will have to await further development and actual systems experience.

g. Publications. Several new papers, in addition to those cited, give additional information on FASTBUS developments.[8-12]

EXPERIMENTAL APPLICATIONS

Various groups are engaged in development efforts for specific experimental application. Some laboratories known to be developing experiments using FASTBUS are BNL, FNAL, TRIUMF, and CERN (with others). A modest implementation is planned at SLAC in collaboration with BNL and LBL.* The most interesting portions are the proposed development of a VAX interface via the DEC DR780, and the implementation of a 68000 FASTBUS Processor. The VAX interface unit will be designed at BNL and the first prototypes built there. SLAC will provide a number of modules (scanning multichannel ADC, I/O registers, dual port memory, SI, and probably a Snoop option) together with the 68000 controller and operating system. The controller will have both master and slave logic, and will execute address or data cycles in as little as one CPU instruction. The controller's memory management unit will support mapping for 16 resident processes with memory segmentation, segment protection and relocation, and demand paging. The prototype will include a Multibus interace which will be brought out on the auxiliary connector to allow access to existing disk controllers, etc. High speed serial I/O ports, multiple timers, and a low power calendar/clock will also be included.** The microcontroller language will probably be PASCAL. Budgets permitting, it is hoped to complete the development in one year.

[As a general development, SLAC is also designing a 68000 color graphics (raster-scan) unit. This is basically a fallout of the 68000 processor work. This module will have an MMU specifically designed to handle from 16 to 100 concurrent FORTH tasks, each up to 65K bytes in size.§]

Initial designs are essentially complete, and prototype construction of both the graphics unit and the processor is getting underway.

VENDOR ACTIVITY

The JWC crate design has already been mentioned. In addition, JWC is offering a modular bulk power supply package, cooling chassis, and extender cards.

Todd Engineering of Long Island has just delivered several packaged bulk power supplies capable of ±200A at ±5V, 65A at -2V, and ±15V as an option.

Several other vendors have shown interest in FASTBUS and some are believed to have development activities yet to be announced.

Elfab of Dallas is presumed to be still available as a source of backplanes, and Nuclear Specialties of San Leandro as a source of crates.

---

* Private communication: M. Breidenbach (SLAC), E. Siskind (BNL), and S. Loken (LBL).

** Private communication: S. R. Deiss (SLAC).

§ ibid.

FUTURE PROJECTIONS

For at least some of the laboratories, FY'82 is the last year for special funding requests from DOE, in anticipation that further prototype work will be done only in conjunction with specific lab programs. Thus we expect that the various demonstration programs outlined will suffice to satisfactorily demonstrate FASTBUS hardware and software, and to expurgate any serious bugs which may be lurking. It will obviously be a long time before the full specification is tested, and continued maintenance on the specification is a normal expectation.

Once the formal document is released, it is expected that vendor activity will increase. Hopefully, early versions of the SI, Snoop, Cable Segment and computer interfaces can be made commercially available. One would like to develop at least two sources of these critical system components, in addition to crates, power supplies, and the various backplane logic cards. European manufacturers can be expected to progress in parallel to make FASTBUS available to their constituents.

In addition, we would hope for the development of custom interface chips, in order to greatly facilitate FASTBUS design and utilization. The first of these will likely be a gate array (ECL) implementation. Hopefully prototypes can be completed by lab efforts in FY'82.

Finally, we might conjecture on the applicability of FASTBUS to controls field. Initially, this seems improbable because of the ECL implementaion. However, FASTBUS in another technology, e.g., TTL or even CMOS, may prove very attractive for future distributed control applications. This should be studied as soon as the current program is brought to a satisfactory conclusion. A high-speed serial link is also needed.

SUMMARY

The FASTBUS program has accomplished some of its major goals and so far the rsults are highly satisfactory. It is expected to complete the test program in FY'82 insofar as demonstrating standard hardware and software for multicrate systems. Further developments will be determined by specific laboratory needs and by industry. Optimization of a version of FASTBUS for control applications should be a future goal.

ACKNOWLEDGMENT

The team working on FASTBUS is large and it is impossible to list individual contributions. Most of the technical work either has appeared or will eventually appear in print under the names of the chief contributors.

The work and continued support of all of these people is gratefully acknowledged.

REFERENCES

1. U.S. NIM Committee, "FASTBUS Modular High Speed Data Acquisition System for High Energy Physics and Other Applications," Working Group Document-Tentative Specification (20 Aug 1981), available from L. Costrell, NBS, Washington, D.C.
2. L. Paffrath, B Bertolucci, S. Deiss, D. Gustavson, T. Holmes, D. Horelick, R. Larsen, C. Logg, and H. Walz, Stanford Linear Accelerator Center; and B. Downing, University of Illinois, "A FASTBUS Demonstration System," (Paper 2J1, this Conference).
3. B. Bertolucci and D. Horelick, "Design of a FASTBUS Programmable Sequencer Module and Memory Module," Stanford Linear Accelerator Center, (Paper 2J3, this Conference).
4. B. Bertolucci, "Modules and Supporting Hardware for FASTBUS Test and Diagnostic Purposes," Stanford Linear Accelerator Center, (Paper 1B8, this Conference, Title Only).
5. Helmut V. Walz, Stanford Linear Accelerator Center, and Robert Downing, University of Illinois, "FASTBUS Snoop Diagnostic Module," IEEE Trans. on Nucl. Sci., NS-28, No. 1, (Feb. 1961), p. 380.
6. D. Gustavson, Terry L. Holmes, L. Paffrath, John P. Steffani, "A 'Front Panel' Human Interface for FASTBUS," IEEE Trans. on Nucl. Sci., Vol. NS-28, No. 1, (Feb. 1981), p. 380.
7. R. Downing and M. Haney, University of Illinois, "The FASTBUS Segment Interconnect and Cable Segment," (Paper 2J2, this Conference).
8. L. Paffrath, Stanford Linear Accelerator Center, "The FASTBUS Standard - A Review of the Current Status," Contributed to the Topical Conference on Computerized Data Acquisition in Particle and Nuclear Physics, Oak Ridge, Tennessee, May 28-30, 1981.
9. D. Gustavson, Stanford Linear Accelerator Center, "FASTBUS Status from a System Designer's Point of View," contributed to the Topical Conference on Computerized Data Acquisition in Particle and Nuclear Physics, Oak Ridge, Tennessee, May 28-30, 1981.
10. C. A. Logg, L. Paffrath, B. Bertolucci, and D. Horelick, Stanford Linear Accelerator Center, "FASTBUS Introduction and Demonstration," contributed to the Topical Conference on Computerized Data Acquisition in Particle and Nuclear Physics, Oak Ridge, Tennessee, May 28-30, 1981.
11. S. R. Deiss et al,. Stanford Linear Accelerator Center, and R. Downing University of Illinois, "Applicability of the FASTBUS Standard to Distributed Control," presented at 1981 Particle Accelerator Conference, Washington, D.C., March 11-13, 1981.
12. R. W. Downing, University of Illinois, "FASTBUS Slaves - A Designer's View," contributed to the Topical Conference on Computerized Data Acquisition in Particle and Nuclear Phusics, Oak Ridge, Tennessee, May 28-30, 1981.