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# A MULTI-HIT DRIFT TIME DIGITIZER*

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## SUMMARY

We describe electronics for a drift chamber which measures drift times and has multi-hit capability. The system is based on a stable (±0.005%) 125 MHz clock which eliminates the need for frequent calibrations. The times are digitized according to a Gray code in order to restrict transition errors to the least significant bit. The least count is 4 ns which contributes an rms error of 58 μm to the measurement of drift distance.

## 1.0. INTRODUCTION

This paper reports on the electronics system developed for the drift chambers which were built for the DELCO detector at PEP. Three drift chamber systems were constructed: a cylindrical chamber of 384 sense wires placed close to the beam axis; another cylindrical drift chamber of 830 wires placed coaxially with the first chamber; and a planar chamber system of 900 wires for the outer part of the detector.

The time structure at PEP, where the beams cross every 2.4 μs, led to two important system features. Firstly, the beam-crossing pulse obtained from the pickup electrode ahead of the interaction point provides the start time. Secondly, after the data have been collected, a track finder analyzes the data and provides trigger information before the next beam crossing.

Physics considerations dictated the need for electronics with a multi-hit capability. In order to minimize cost, 8 sense wires were multiplexed at the memory. This causes no extra inefficiency in recording hit wires but produces a loss of precision in a small number of cases as discussed in sec. 2.2.

Finally, we designed a totally digital system to avoid the burdens of calibrating a large analog system. With presently available electronics we found it possible to achieve a 4 ns resolution at reasonable cost while not compromising the accuracy required in large drift chamber systems.

## 2.0. ELECTRONIC CIRCUITS

Figure 1 shows the block diagram of the electronics for the cylindrical drift chambers. The circuitry for the planar drift chamber differs only in the mechanical construction of the the amplifiers which are single-channel and mounted directly on the chambers. In the case of the cylindrical chambers the raw signals are carried 5 m along flat coaxial cables to 16-channel amplifier modules.

The electronics circuits described in this section have been designed predominantly using ECL 10000 components to achieve good timing resolution and minimize propagation delay times.

Following the block diagram of Figure 1, a signal generated on the sense wire passes an amplifier-discriminator circuit (sec. 2.1) and is applied to an 8-channel drift time digitizer module, DTD (sec. 2.2). This module also has an 8-bit digital input, $G_0$-$G_7$, representing the time elapsed from $t_{start}$, the beginning of the drift interval. Words which contain the wire number and its associated time are stored in local memory. This is eventually read into a PDP11/45

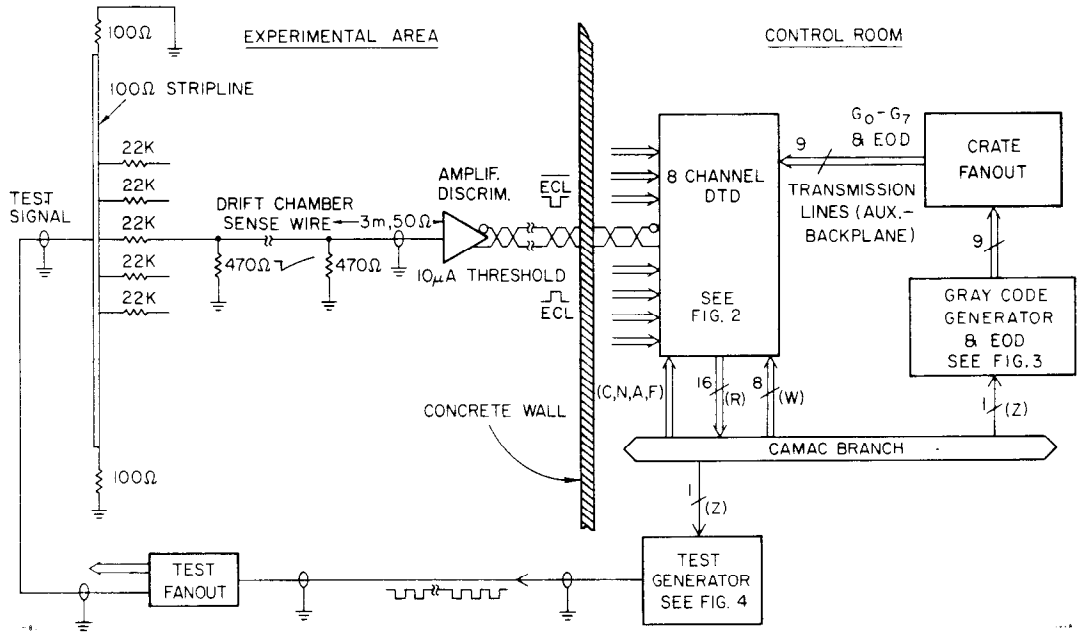


Fig. 1. Multi-hit electronics for drift chambers.

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computer and simultaneously to an LSI-11 microcomputer via a CAMAC branch and interface circuits which include buffer memories.

The Gray code generator (sec 2.3) produces an 8-bit timing code in which the lsb represents 4 ns. The stability of the timing information is determined by a crystal clock of 125 MHz ± 0.005% which is common to the complete system thus eliminating the need for corrections on individual channels.

The test generator (sec. 2.4) produces a sequence of pulses at digitally selectable intervals. This pulse train is applied to all drift chamber planes via fanouts of matched characteristic impedances to minimize reflections.

A detailed description of each major component of the system is given in secs. 2.1 through 2.4.

## 2.1. Amplifier-Discriminator

The input consists of a PNP-NPN feedback amplifier followed by two stages of amplification provided by an ECL receiver, type 10216, used in a linear mode. The discriminator, conveniently using the third amplifier of the ECL 10216, is of the width-over-threshold type with a minimum width of approximately 40 ns. The output stage, ECL type 10101, drives differentially a 45 m twisted and shielded pair[1] of 100 Ohm characteristic impedance with excellent frequency response and a rise time (to 50%) of better than 5 ns. The amplifier, which is a modification of a CERN design (type 4241, Ref. 2), has a minimum threshold referred to the input of 250 μV; in this experiment the threshold is set to 500 μV.

## 2.2. Drift Time Digitizer (DTD)

The block diagram of the DTD is shown in Fig. 2. It accepts 8 channels of wire data, assigns to each signal a drift time and stores the time and wire information in a 16 word × 16 bit memory. The time information is expressed in an 8-bit Gray code thus limiting the transition errors to ±1/2 least count while latching the information "on-the-fly", i.e., from a running clock. The rationale of using a Gray code and details of its generation are given in Ref. 3. With a 4 ns resolution and an 8-bit capacity the drift times that can be measured span an interval up to 1024 ns.

The DTD has a multi-hit capability with certain limitations that will be discussed later. At most 15 of the 16 memory words can be used to store information since the word immediately following the data words is used as a flag (all zeros in the upper 8 bits). Using a "stop-mode" CAMAC block transfer, the scanner is directed during the read cycle to access the next module whenever the flag is encountered.

Returning to the write cycle, data are written in consecutive address locations of the memory, the memory address register (MAR) being incremented at each end of memory cycle (EMC). Should the number of words during one drift time exceed the memory capacity in the module then all words above the 15th word are lost and the flag word is written into the 16th memory location. This phenomenon is observed in << 1 percent of the accessed memories.

Since the memory in the module is shared by eight wires, a conflict arises when two or more wires generate hits within the same memory cycle (≈32 ns). When this situation arises, the circuitry deals with the second hit in two different ways depending on the arrival time of the second hit with respect to the first. (i) If the second hit arrives 0 to 10 ns later, the two hits are recorded in the corresponding memory bits that represent their wire identities and this byte is attached to a single time (that of the first hit). The resultant time error is 5 ns and only one memory word is generated. (ii) If the second hit arrives

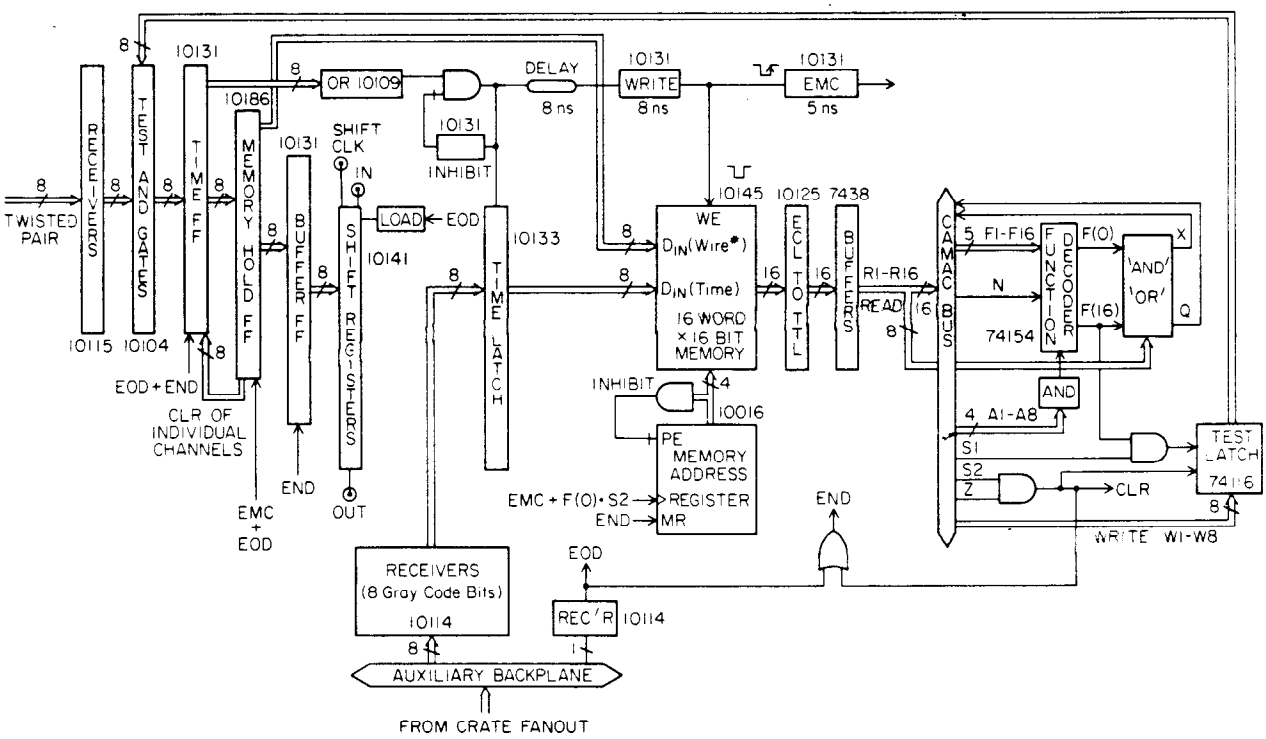


Fig. 2. Drift time digitizer module.
EMC = End of memory cycle.
EOD = End of drift cycle.
END = EOD + CLR.

during the latter part of the memory cycle (i.e., from 10 to 32 ns) then two words are written in the memory. The first word, corresponding to the earlier hit, will have the correct time associated with it. The second word, representing the second hit, will start a new memory write cycle immediately upon completion of the previous memory write cycle and will thus have an rms error of 7 ns. The errors in both cases were accepted as a reasonable compromise between price plus complexity vs a small loss in accuracy for about 10% of the hits. Note that all such hits are flagged and can be treated separately in the subsequent data analysis.

The buffer FFs and eight bits of shift register are used to store wire data during one event and shift them out at the end of the drift time. The information from the 16 planes is then processed by a track recognition circuit (to be published) and serves as a secondary event trigger.

The TEST LATCH with the TEST 'AND' GATES are used in testing procedures as described in sec. 2.4.

## 2.3. Gray Code Generator

The block diagram of the Gray code generator is shown in Fig. 3. It consists of a 125 MHz ±0.005% clock (Ref. 4), a synchronizer, a binary-to-Gray-code converter, a phase detector and auxiliary circuits.

$t_{start}$ is determined by the $e^{+}\,e^{-}$ crossing in the detector. Since the clock is free running, a synchronization circuit is required to start the Gray code at the next positive transition of the clock after $t_{start}$. This synchronization produces an offset that is different for each event. The offset is measured in the phase detector that yields a charge proportional to the timing error. This charge is recorded in an ADC and a common correction factor is later applied to all drift times in that event.

The module also produces an end-of-drift signal, EOD, which is used to inhibit the DTDs outside the drift time intervals.

## 2.4. Test Generator and Test Procedure

This circuit generates a train of pulses to test most major components of the system, including the sense wires, the amplifier-discriminators, the DTDs and their multi-hit capability and, finally, the CAMAC branch. The block diagram of the test generator is shown in Fig. 4. An 8-bit Gray code is produced from a free running clock and a synchronous binary counter in a similar manner to the Gray code generator described in sec. 2.3. The start of the timing code is initiated by CAMAC "EXECUTE" command, F(25), while the end of the timing code is generated on the 9th bit of the synchronous binary counter. The module is initialized by loading into the 16 word × 8 bit memory, 16 eight-bit words that represent the leading edge times of the pulses that ultimately constitute the pulse train. The 16 words appear in the memory in Gray code due to the combinational binary to Gray code converter that is interposed between the CAMAC write lines and the memory. The time intervals between the pulses in the pulse train can be specified with a resolution of 4 ns, the only limitation being that the codes must be monotonically increasing in time.

As soon as F(25) is executed, the time code starts changing at the A inputs to the digital comparator. When the input is identical to the B input (which is derived from the output ports of the memory) the comparator generates a pulse that is shaped and applied to the output terminal. At the same time the MAR is incremented, making the next timing pulse request available at the B inputs of the digital comparator. When the Gray count reaches this value, the next pulse of the train is generated, etc.

To test the system, the pulse train is fanned out and applied to the center of a motherboard in a network that retains the characteristic impedance. It is then further attenuated by a factor of 100 before being fed to the sense wires. The latter are terminated at both ends via 470 Ohm resistors to minimize reflections and thus allow measurements of the multi-hit property.

In the test mode it is sometimes desired to disable selected inputs to each module. This is accomplished by the TEST LATCH and TEST 'AND"' gates (Fig. 2) via a CAMAC write command.

Since the test signal is applied at the far end of the sense wires (i.e., away from the amplifiers) the test procedure also tests continuity of the sense wires.

## 3.0. PERFORMANCE

The system has been in operation for 18 months and performed to specification. The 4 ns electronic resolution did not degrade measurably the resolution of the

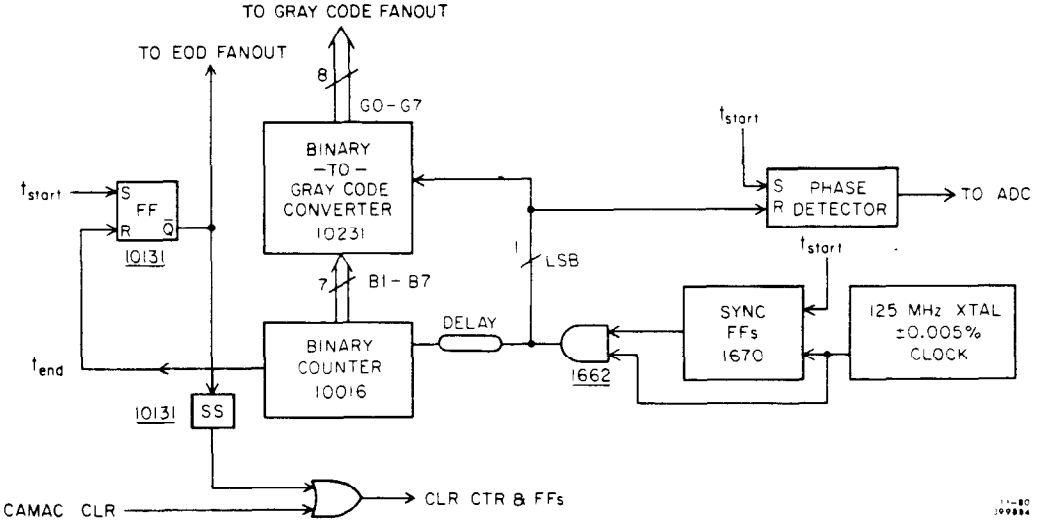


Fig. 3. Gray code generator.
$t_{start}$ = start of drift time.
$t_{end}$ = end of drift time.

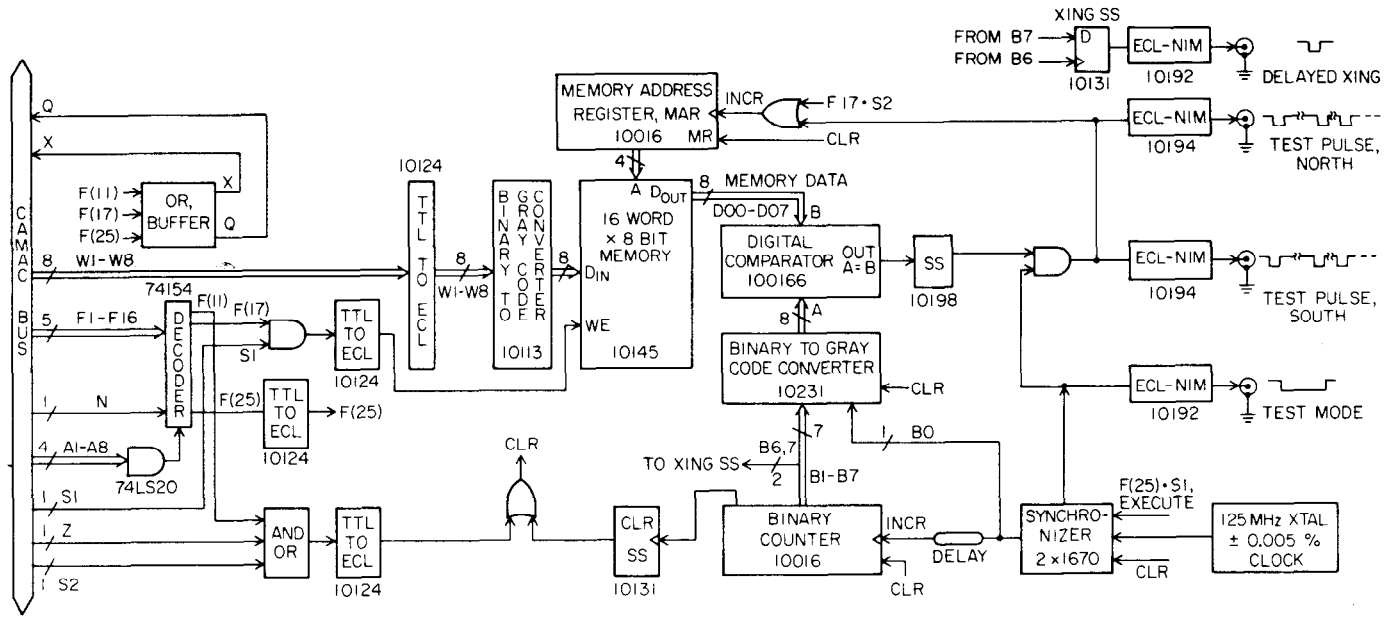


Fig. 4. Test Generator.

complete system as was verified by measurements with LRS DC201A amplifiers and the LRS2770A Time Digitizers having a resolution of 2.5 ns. Data obtained with both systems showed the same rms resolution of 180 μm.

### 3.1. Advantages and Disadvantages of the Electronic System

Since there is a single clock for the drift time digitizers, channel-to-channel variations are reduced to the variable delay through different ICs. In the case of the ECL 10000 series these variations are minimal as a function of temperature; in addition, since each of the clock bits is bused separately and has its own particular path, there are differences in the phase of the various bits up to 1 ns. These differences were removed by cable trimming during initial setup of the system.

The electronics is capable of accepting and independently digitizing multiple signals on a single wire. The system introduces no additional hit inefficiency but does somewhat degrade the time resolution under certain circumstances as discussed in sec. 2.2.

The multi-hit capability, taken together with the desire for high efficiency (and hence large signal-to-threshold ratio) can lead to fake multiple hits. These hits make the subsequent analysis more cumbersome and could obscure real hits. This problem is, of course, common to other designs with multi-hit capabilities.


## ACKNOWLEDGEMENTS

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## REFERENCES


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