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AN INTEGRATED AMPLIFIER AND SAMPLE-AND-HOLD ANALOG MULTIPLEXER MODULE*

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ABSTRACT

The integrated amplifier and sample-and-hold analog multiplexer-ISHAM, is a proportional wire chamber analog readout module. It includes the front-end amplifier, the gated integrator and the sample-and-hold analog multiplexer. A density of 24 channels per module was achieved in a nonstandard multilayer P.C. board. Besides the above mentioned functions, the module provides: the control circuits for the Read-In and the Read-Out of the wire signals, the control circuits for the calibration of the 24 amplifiers, and the neutral trigger information. As an additional feature, the high voltage required by each wire is also supplied. The gain is 5 V output voltage @ 20 pC input signal charge. The equivalent input noise charge is 4×10^{-15} C for the channel only and 6×10^{-15} C for the entire system. The nonlinearity is better than 0.1% f.s. and the crosstalk is less than 1%. The Z-position resolution achieved is 1%.

Submitted for Publication

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INTRODUCTION

The ISHAM electronics was designed for two major constituents of the MARK III wide angle detector: the Barrel and the End-Cap shower counters [1].

The Barrel shower counter consists of 24 layers; each layer contains 320 proportional wires. The wires are read individually for the first 6 layers and in groups of 3 radially, for the outer 18 layers, Fig. 1. This structure mainly determined the configuration of the printed circuit board: six channels specified for single wires alternating with six channels specified for triple wires. Each P.C. board processes the signals originating from two adjacent radial sections of the chambers. The Barrel shower counter wire is 47 μm stainless steel, permitting Z-position measurements by measuring the pulse height at both ends.

The End-Cap shower counters have the same characteristics as the Barrel shower counter, being made of 24 layers of proportional counters, each layer having 94 cells. Position along the wire is obtained by charge division, the same as for the Barrel counter. The sense wires are of 37 μm diameter stainless steel. As in the Barrel shower counter, the first 6 layers are read individually and the outer 18 layers in groups of 3. For the End-Cap counters, the ends of each wire (single or triple) are connected to the corresponding amplifiers which are located on the same P.C. board, while for the Barrel counter the corresponding amplifiers for the same wire are located in different crates.

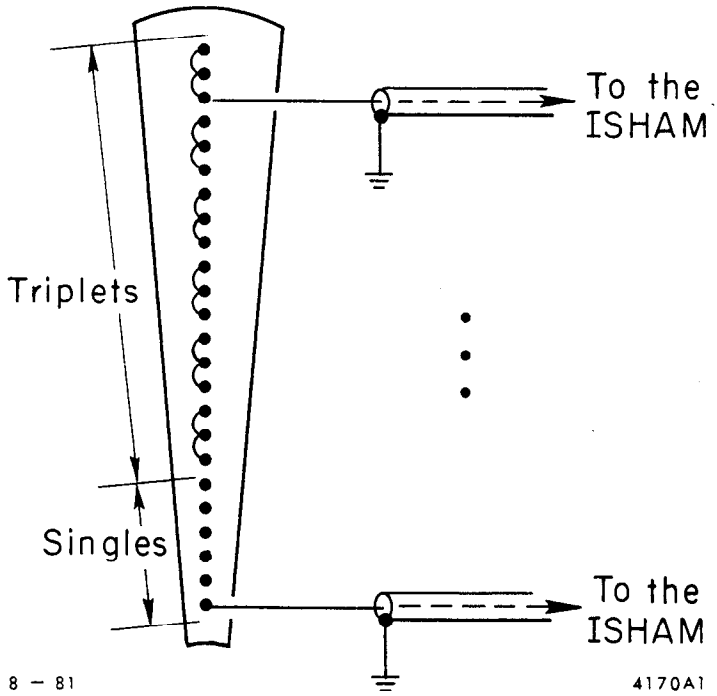

Fig. 1. The Barrel Shower Counter Section; 320 sections like this constitute the chamber.

As the Z-position measurement requires an ISHAM-channel at each end, a total of 12,192 channels must be provided: 7,680 for the Barrel counter and 2 × 2,256 for the End-Cap counters. To carry this huge number of signals to the control room, the cost of the cables required becomes a real limitation of the system. This expense was avoided by integrating the whole electronics, i.e., the front-end amplifier, the gated integrator, the sample-and-hold analog multiplexer and the logic circuitry as well, onto the ISHAM module. The crates accept up to 20 ISHAM-modules and one Control-module and are located in the proximity of the detector itself. This solution reduced the length of the cables to 14 ft each.

THE ISHAM DYNAMIC RANGE [2]

Assuming the pulse height is read by a SLAC-BADC (Brilliant Analog-to-Digital Converter) [3] with 4,096 channels @ 5 V f.s., the optimal amplifier gain for the ISHAM is defined by the following principal considerations:

1. The discreteness of the digitization should not degrade the signal-to-noise ratio.
2. The optimal dynamic range for high energy showers should be achieved; we wish to calibrate up to 3.7 GeV e^-'s.
3. Also, the amplifier should not saturate before we reach channel 4,000 on the BADC.

Bearing in mind these considerations, it follows that:

(a) Criterion (1) requires that the amplifier noise should have a σ = 2 channels on the BADC. The amplifier gain should be designed to provide this value. The discreteness of the BADC then contributes $1/\sqrt{12}$ ch to σ which is negligible. A pedestal of 10-15 channels would be optimum for this noise value.

(b) Given (a) above, the signal-to-noise ratio of 100 for a single particle gives, at most, 200 channels on the BADC (if it hits near one end of the wire; one gets 100 channels in the middle).

(c) The smallest pulse height for a single particle is then 10 to 20 channels (depending on Z-division intercept). This can be separated from the noise value of 2 channels.

(d) With the value for a single hit given in (b), one can accept up to 20 hits per wire-pair, at extreme Z-position, before one hits channel 4,000 on the BADC.

(e) To prevent the amplifier from saturating before reaching 20 hits, the maximum current accepted without saturation must be:

$$\text{20 hits} = 150\ e^-\text{'s} \times 20 = 3{,}000\ e^-\text{'s collected.}$$

$$\text{Gas gain} = 5 \times 10^4.$$

The signal charge at the input of the amplifier is:

$$q_s \leq \text{20 hits} \times G_{gas} \times q_e = 3{,}000\ e^-\text{'s} \times 5 \times 10^4 \times 1.6 \times 10^{-19} = 24\ \text{pC}$$

The pulse would probably be fairly long in duration as the particles would fill a cell. It would probably be reasonable to

assume a pulse duration of 200 ns. Thus, the maximum input current would be about:

$$i_s = \frac{20\ pC}{200\ ns} = 100\ \mu A$$

Into 50 ohms preamplifier input impedance, this will result in a 5 mV signal voltage. To avoid saturation, the overall voltage gain should be 1,000. With this gain, channel 4,000 in the BADC will correspond to 5 V; therefore, the BADC calibration with respect to the input charge is 5 fC/channel.

Z-MEASUREMENT DESIGN CONSIDERATIONS

A. Circuit Configuration

Z-position measurements by the charge division method require low-input impedance preamplifiers. This value must be low in comparison with the wire resistance in order to maximize the position sensitivity and to minimize the effect of small variations of the wire resistance on the position measurements. The most convenient way to implement this requirement is to take advantage of the bipolar transistor, in the grounded-base configuration, as the front-end preamplifier. This solution provides:

- a low dynamic input impedance which is easy to control.
- a reasonable low noise factor.
- the lowest cost per channel.

Each end of the wire is provided with a current-to-voltage amplifier, which consists of the grounded-base preamplifier followed by a feedback amplifier, and a gated integrator, Fig. 2.

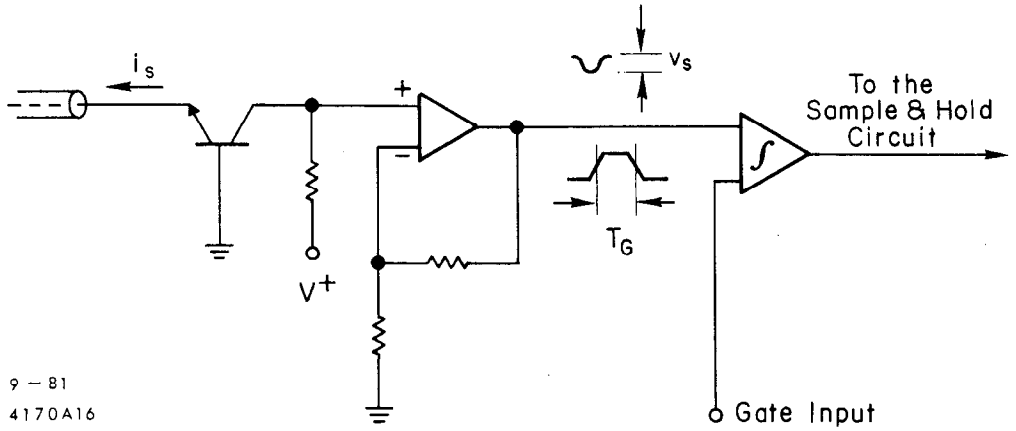

Fig. 2. ISHAM: The Front-End Amplifier.

The whole electronics is implemented onto the same P.C. board; thus the remote amplifiers are connected to the chamber via 50 ohms high-voltage coax cables, each 14 ft long.

The system configuration is shown in Fig. 3.

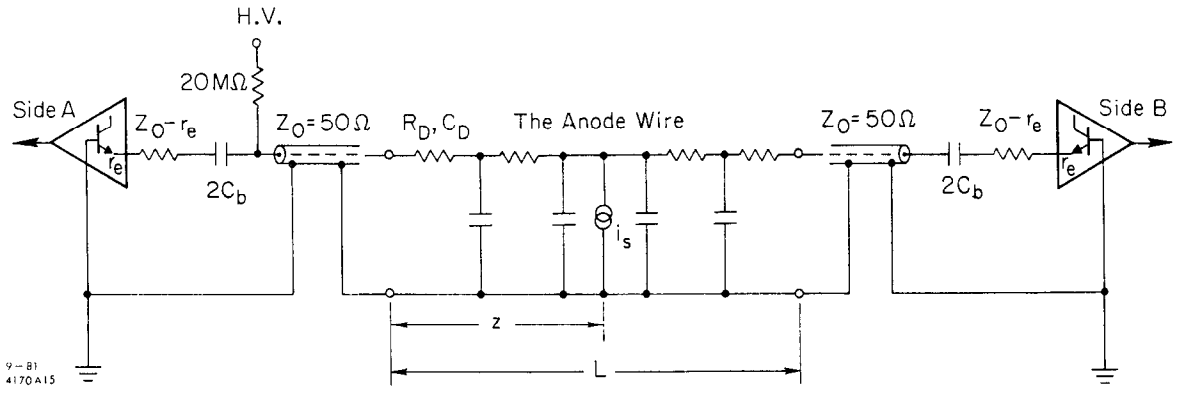

Fig. 3. ISHAM: The System Configuration.

B. Linearity

1. Due to the diffusive nature of the line $(\tau_D = R_D C_D)$, it takes time, after a charge impulse is delivered, until the ratio $Q_A/(Q_A + Q_B) = z/L$ is established. The charge collected at one end of the wire (assuming that each end of the wire is connected to a zero input impedance amplifier) as a function of time and position is given by V. Radeka [4]:

$$\frac{Q_A}{Q_A + Q_B} = 1 - \frac{z}{L} - \sum_{m=1}^{\infty} \frac{2}{m\pi} \, Si\left(\frac{m\pi z}{L}\right) \exp\left(-\frac{m^2\pi^2}{\tau_D} t\right) \quad (1)$$

For a linear relation between $Q(t,z)$ and the position, the sum in Eq. (1) should be negligible. The time required for the position non-linearity to be less than 0.2% is

$$t \geq \frac{1}{2} \tau_D \quad (2)$$

In our case:

$$\tau_D = R_D C_D = 3 \times 10^3 \times 33 \times 10^{-12} \simeq 100 \text{ ns}$$

Based on the multihit charge collection time, the integration time (gating time) in our detector was set to $T_G = 1$ μs; this satisfies the above condition (2), even if one takes into account the propagation time due to the 14 ft coax cable required by each end of the wire.

2. In our configuration, the total charge (energy) signal has to be obtained by summing amplifiers or by summing the digitized output signals from the ends of the wire [5]. We use the latter method;

in this case an accurate knowledge of the amplifiers' gain is required, otherwise a nonlinearity in the ratio $[Q_A/(Q_A + Q_B)]$ with position is introduced.

3. The presence of the high voltage on the anode wires implies a decoupling capacitor ($2C_b$) at each wire end, Fig. 3. As a result, the configuration is also subject to a position nonlinearity due to the decoupling capacitors. In this system, the charge initially divides according to the ratio of the resistances with respect to the point of charge interception. For equal decoupling capacitors the charge is eventually distributed correctly to the two preamplifiers. The error is proportional to $\tau_F/R_D C_b$, where τ_F is the time width of the unipolar trapezoidal filter, which in our case might be assimilated with the gating time T_G = 1.0 μs. (In our system the weighting function of the time-variant filter is rectangular, but based on the transition time of the CMOS FET-switches, we can consider it a unipolar trapezoidal weighting function.) This error can usually be made small using high value capacitance such as 0.1 μF. However, for practical reasons, i.e., high voltage, stored energy, space, and cost, lower values for the decoupling capacitors are desirable.

The minimum value of the decoupling capacitors is determined by the signal charge feedback. The result of this approach led to the following expression given by V. Radeka and P. Rehak [6]:

$$\frac{Q_A}{Q_A + Q_B} \simeq \frac{z}{L}\left(1 + \frac{C_D}{C_b}\right) - \frac{1}{2}\frac{C_D}{C_b} \qquad (3)$$

With this approximation (3), the effect of the decoupling capacitor is stable if C_b is stable, and it only requires a correction of the position data. $(Q_A + Q_B)C_D/C_b$ also represents the total maximum amount of crosstalk from one cell to all adjacent cells. C_D/C_b of one percent, with C_D = 33 pF, requires C_b = 3 nF ($2C_b$ = 6 nF). We decided a higher value $2C_b$ = 25 nF, based on position resolution considerations [7].

C. Position Resolution

According to A. Seiden approach [7], for our system, Fig. 3, the plot charge measured is:

$$\gamma = \frac{Q_A}{Q_A + Q_B} = (1 - 2\beta)\frac{z}{L} + \beta \qquad (4)$$

where

$$\beta = \frac{1}{2}\left[\frac{(1 - e^{-t/\tau})R_D + 2r}{R_D + 2r}\right] \qquad (5)$$

r = cable and amplifier input impedance (r ≃ 50 ohms)

$\tau = (R_D + 2r)C_b \simeq 40$ μs (for our system parameters)

t = the integration time, or the equalization time; t = 0.8 μs as an average.

The position resolution therefore is:

(a) $$\sigma_z = \frac{L\sigma_\gamma}{1 - 2\beta} \qquad (6)$$

assuming for a moment that β is known. If the noise on each pulse height measurement is given by σ_p, and the measured pulse heights are P_1 and P_2 channels, then:

$$\sigma_\gamma = \frac{\sigma_p}{P_1 + P_2} \left[\frac{P_1^2 + P_2^2}{(P_1 + P_2)^2} \right]^{1/2} \tag{7}$$

Note that the best measurement is in the middle of the wire, by a factor of $1/\sqrt{2}$. This expresses σ_z in terms of the measured pulse heights, amplifier noise and the degradation factor $1/(1 - 2\beta)$. For the chosen value $2C_b$ = 25 nF, the position resolution for a single particle hit in the middle of the wire is σ_z = 0.538%.

(b) If β is uncertain because gate sandwiching of pulse is uncertain, then one has an added error:

$$\sigma_z = \frac{L}{(1 - 2\beta)} \left[\sigma_\gamma^2 + \sigma_\beta^2 \left(1 - \frac{2z}{L}\right)^2 \right]^{1/2} \tag{8}$$

where

$$\sigma_\beta = \frac{\sigma_t}{\tau} e^{-t/\tau} \frac{R_D}{2(R_D + 2r)} \tag{9}$$

D. Noise Considerations

Noise added to the charge signals determines the position resolution. One source of noise originates in the resistive wire. This noise source appears in parallel with the input of the amplifier [4]:

$$\overline{ENC^2}_{parallel} \simeq \frac{2kT\, a_{F2}\, \tau_F}{R_D} \quad \text{for} \quad \tau_F \geq \frac{1}{2}\, \tau_D \tag{10}$$

where

R_D = the wire resistance; 3 kohm in our case, for unganged wires.

τ_F = time width of the weighting function; for a unipolar trapezoidal function we assimilate this time with the integration time which is 1.0 μs in our case.

a_{F2} = nondimensional form factor; $a_{F2} = 0.733$ for the assumed unipolar trapezoidal function.

Thus

$$\overline{ENC}_{parallel} = 1.41 \times 10^{-15}\ C$$

The amplifier noise can be represented by a series voltage source and a parallel current source due to the shot noise in the transistor base. The noise is increased due to the capacitance contributed by the coax cable (30 pF/ft) to the input of the amplifier.

For the series noise [4]:

$$\overline{ENC_s^2} = \frac{1}{2}\, \bar{e}_n^2\, C_{in}^2 \left(\frac{a_{F1}}{\tau_F} + \frac{a_{F2}\tau_F}{\tau_{in}^2} \right) \tag{11}$$

where

e_n = RMS eq. series noise voltage per $Hz^{1/2}$; for a low noise transistor $e_n = 10^{-9}$ $V/Hz^{1/2}$.

$C_{in} = C_{det} + C_{amp} + C_{cable} = 33 + 10 + 420 = 460$ pF.

a_{F1} = 40 and $a_{F2} = 0.733$ for the assumed unipolar trapezoidal weighting function.

$\tau_F = 10^{-6}$ s.

$\tau_{in} = R_D C_{in} = 3 \times 10^3 \times 4.6 \times 10^{-10} = 1.38 \times 10^{-6}$ s.

Hence,

$$\overline{ENC}_s = 2 \times 10^{-15}\ C$$

For the shot noise one has [4]:

$$i_n^2 = \frac{2q_e I_e}{h_{fe}}$$

$$\overline{ENC}_p^2 = \frac{1}{2}\, i_n^2\, a_{F2}\, \tau_F \qquad (12)$$

$$\overline{ENC}_p = 1.1 \times 10^{-15}\ C$$

$$\overline{ENC}_{in} = \left[\overline{ENC}^2_{p(Det)} + \overline{ENC}^2_{p(shot\text{-}noise)} + \overline{ENC}_s^2 \right]^{1/2} = 2.68 \times 10^{-15}\ C$$

To this result, the thermal noise due to the emitter resistance R_{E1} and the load resistor R_{C1}, should be added. The collector current shot noise is negligible if the impedance connected to the emitter is much higher than the equivalent series noise resistor $kT/2q_e I_E = r_E$ at all the frequencies in the passband of the filter.

The equivalent noise charge measured in the system, including the environmental pick-up and the ground loop effects, is 6×10^{-15} C.

CIRCUIT DESCRIPTION

A. The Analog Circuit

The amplifier circuit is shown in Fig. 4. The input stage, a grounded base transistor, converts the signal charge into a signal voltage which is amplified by the feedback amplifier which follows it. The input impedance matches the 50 ohm coax cable. The 24 ohm resistor (R1) also limits, to some extent, the discharge current of the HV-decoupling capacitor in case of a spark or short-circuit occurring on the chamber wire. In such a case, the 100 ohm resistor (R4) limits the discharge current through the base-emitter junction of the input transistor (T1) to 7 mA maximum, forcing the discharge current through the diodes' path (D1 and D2). The D3 diode provides the charging path for the HV-decoupling capacitor (C_b).

The value of the resistor R5 is a compromise between the S/N ratio and the signal rise-time. The main purpose of the transistor T2 is to reduce the Miller effect; this allows a higher value of the resistance R5, improving the noise figure without deteriorating the rise-time. As a result, the overall rise-time of the amplifier is 40 ns.

The frequency response and the phase characteristic of the amplifier show a gain margin of -10 dB, and a phase margin of 45^{o} approximately. The calculated voltage gain is 1086.

The amplifier is followed by a gated integrator and a sample-and-hold circuit, Fig. 5. The third stage is a current source which, together with the sampling capacitor (C_{11} = 180 pF), integrates the signal during the sampling time. Assuming a parasitic capacitance of

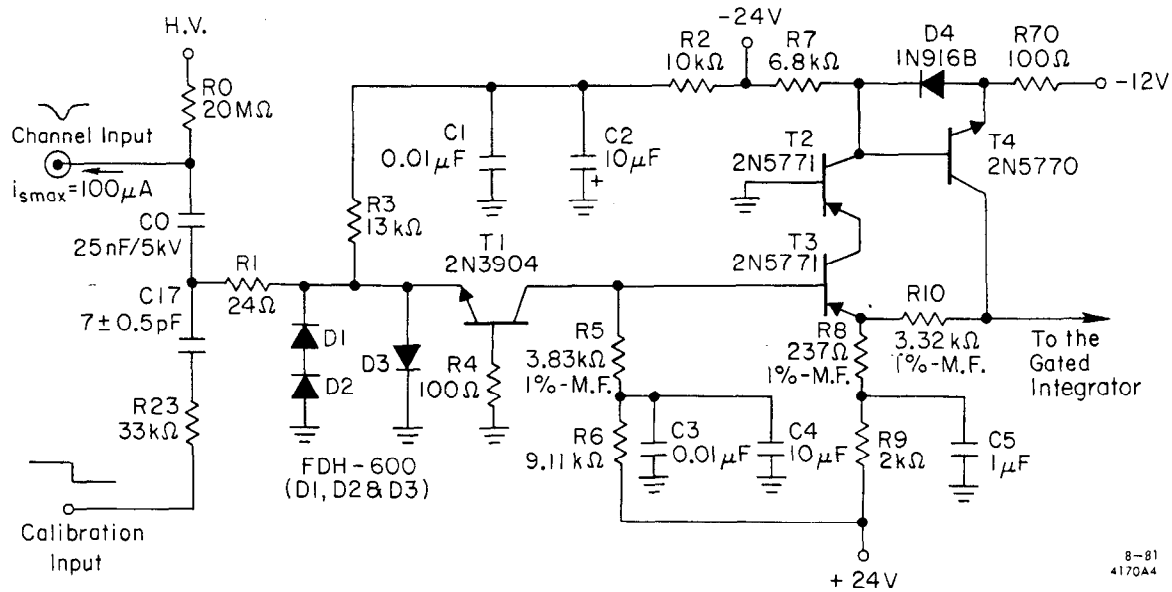

Fig. 4. ISHAM: The Front-End Amplifier Scheme.

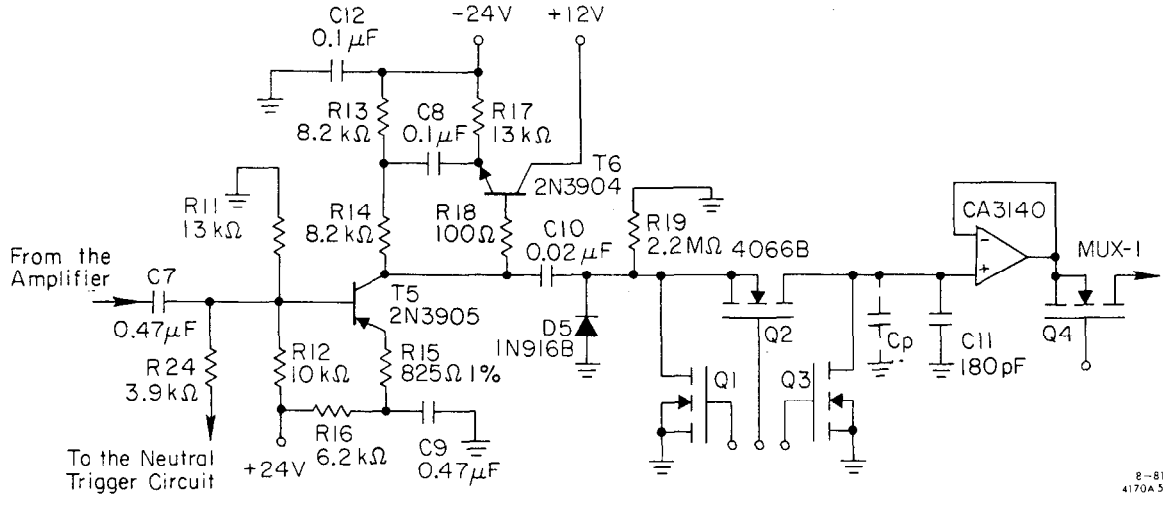

Fig. 5. ISHAM: The Gated Integrator and the Sample-and-Hold Scheme.

the rail C_p = 70 pF and a rectangular pulse of 200 ns width, the output voltage is

$$V_o = \frac{G_{amp}}{C_s R_{15}} \int_o^{t_w} v_s \, dt = \frac{V_s \times G_{amp} \times t_w}{C_s R_{15}} \qquad (13)$$

where $C_s = C_{11} + C_p$ = 250 pF. Hence, the overall gain is 1000.

The current source output impedance (T5) is increased by the bootstrapping stage (T6) which results in a better linearity and a smaller sag during the sampling time.

The sample-and-hold circuit is based on Q1 and Q2 FET-switches (Type 4066B, four switches in a package), operated at 12 V. Q1 is normally closed, thus it clamps the integrator output to ground through a relatively low impedance (R_{ON} = 100 ohm typical) during the READ-OUT cycle. In this way, the feedthrough of the signal into the storage capacitor, via Q2 FET-switch, is avoided. Q2 is normally open; it is operated during the READ-IN cycle and for the externally applied RESET pulse. Q3 FET-swtich is normally open. It is closed after each READ-OUT of the channel analog data and while an external RESET pulse is given to the system. When an event is aborted, by the trigger-decision logic, the storage capacitors are discharged via Q3 and Q1-Q2 in parallel with it; this combination brings the discharge path to an impedance of 66 ohm typical. Since the trigger-decision is achieved after 640 ns of the 780 ns beam-cycle, a RESET pulse of 100 ns is supplied to the whole system. As the discharge time constant is $\tau_{discharge}$ = 16.5 ns, the storage capacitors are discharged to 0.2%.

During the READ-OUT cycle of 2,000 channels, which requires 8.0 ms for our BADC, the contribution of the buffer amplifier (CA 3140) bias current to the charge already stored in the storage capacitor is, for the worst case:

$$\Delta V = \frac{I_{bias}\, t_{READ-OUT}}{C_s} = \frac{50 \times 10^{-12} \times 8 \times 10^{-3}}{2.5 \times 10^{-10}} = 1.60 \text{ mV}$$

This value is about one channel for the BADC.

B. The Logic Circuits

The simplified logic scheme is shown in Fig. 6. To ease the brief explanation which follows, we emphasize the two distinct cycles: the READ-IN cycle and the READ-OUT cycle.

1. The READ-IN cycle

This cycle is based on the timing diagram shown in Fig. 7. The time delay t_{d1} is necessary to avoid the feedthrough of the 12 V control pulse, which operates the parallel switch Q1, into the storage capacitor. The time delay t_{d2} is required to prevent the stored charge to leak via Q1 and Q2. The charge fed through during the leading and the trailing edge transition of the Q2 control pulse averages to zero. A RESET pulse preceeds by one beam-cycle (780 ns) the READ-IN cycle to make sure that any charge which might accumulate in the storage capacitors, due to the bias current of the buffer amplifiers, is cleared.

If the trigger decision is to abort the event, a RESET pulse is sent to the system 640 ns after the start of the READ-IN cycle, which discharges the storage capacitors and resets the READ-IN cycle.

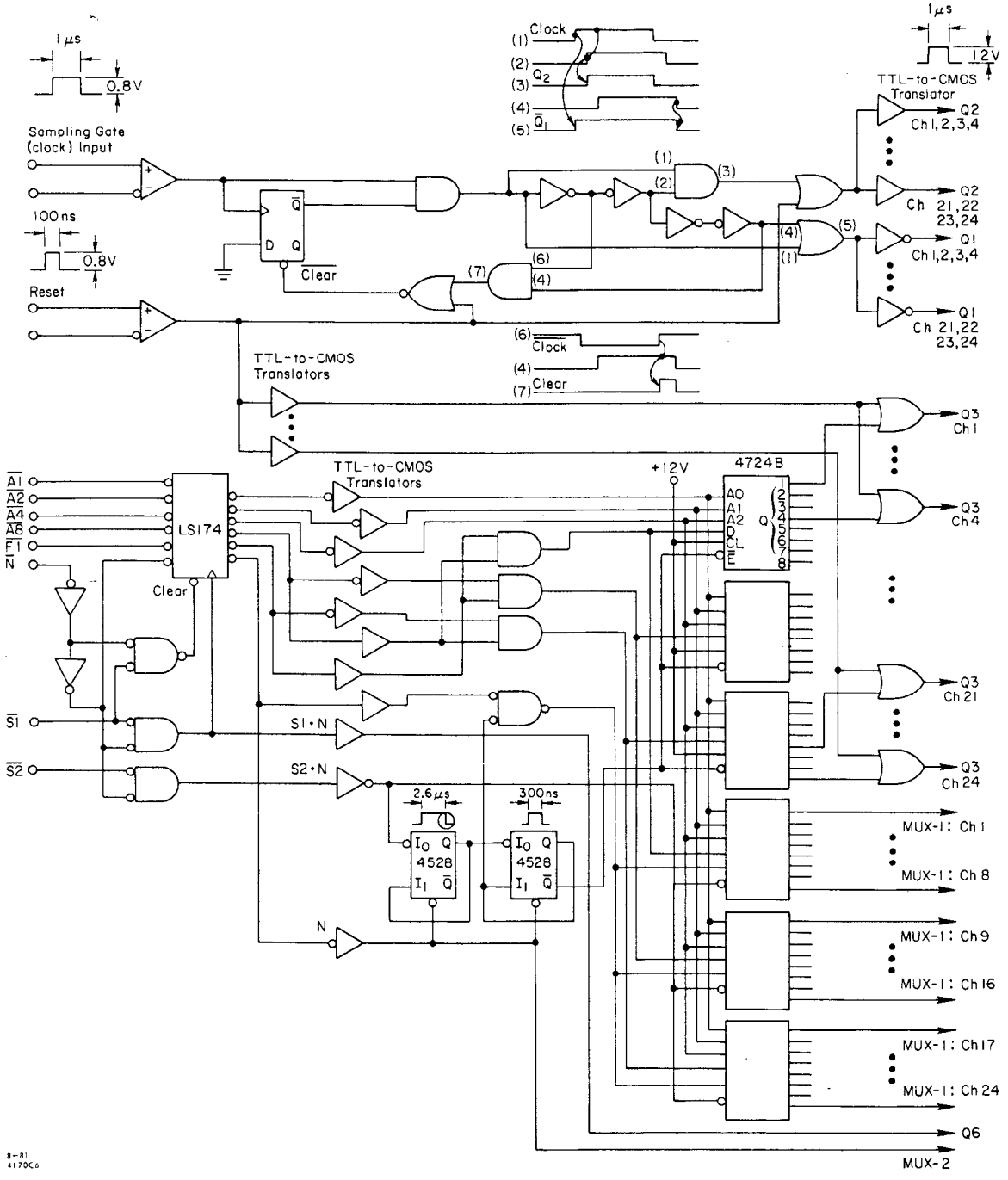

Fig. 6. ISHAM: The Logic Scheme.

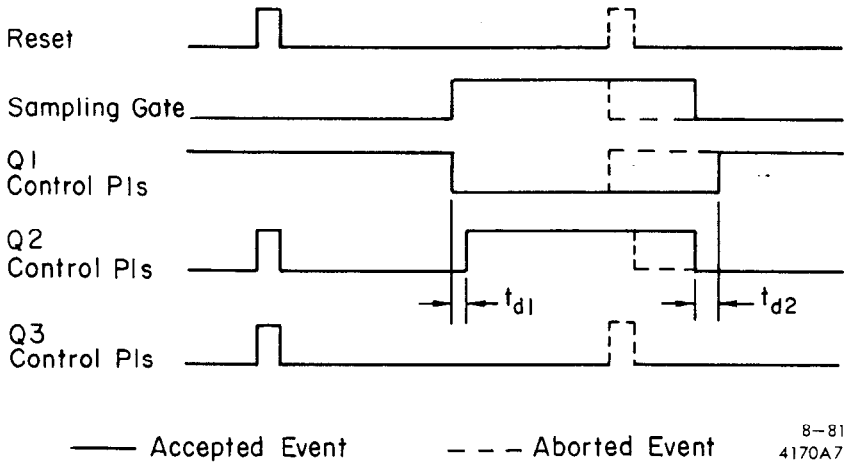

Fig. 7. ISHAM: The READ-IN Timing Diagram.

2. The READ-OUT Cycle

Two multiplexers are involved in this cycle: (a) the module multiplexer, MUX-2, which is under the control of the CAMAC N-lines during the READ-OUT of the 24 channels implemented onto the P.C. board; (b) The channel multiplexer, MUX-1, which is controlled by the CAMAC subaddress lines, including F1 line.

The scheme of these two multiplexers is shown in Fig. 9. Each 4066B FET-switch has a parasitic capacitance C_{out} = 8 pF typical. Therefore MUX-1 is loaded by a total parasitic capacitance C_{p1} = 200 pF; hence, when one channel is addressed, the buffer amplifier is required to drive this capacitive load to the signal value, which affects the settling time. In order to improve the settling time, the signal already stored in this parasitic capacitance is cleared by Q5 before the next channel is addressed. This FET-switch is operated by an INTERNAL RESET pulse, just immediately after the READ-OUT of the current channel. This speeds up the settling of the analog data line.

The MUX-2, which is OR-ing 20 modules, presents a total capacitive load C_{p2} = 200 pF. To keep the load of the MUX-1 in reasonable limits, an extra fast buffer amplifier (one per module, $t_{settling}$ = 250 ns) separates the two parasitic capacitances C_{p1} and C_{p2}.

To make the task of this buffer/driver amplifier easier, the analog line is discharged by Q6 each time a CAMAC pulse S1 • N reaches the ISHAM module. The READ-OUT timing diagram is shown in Fig. 8.

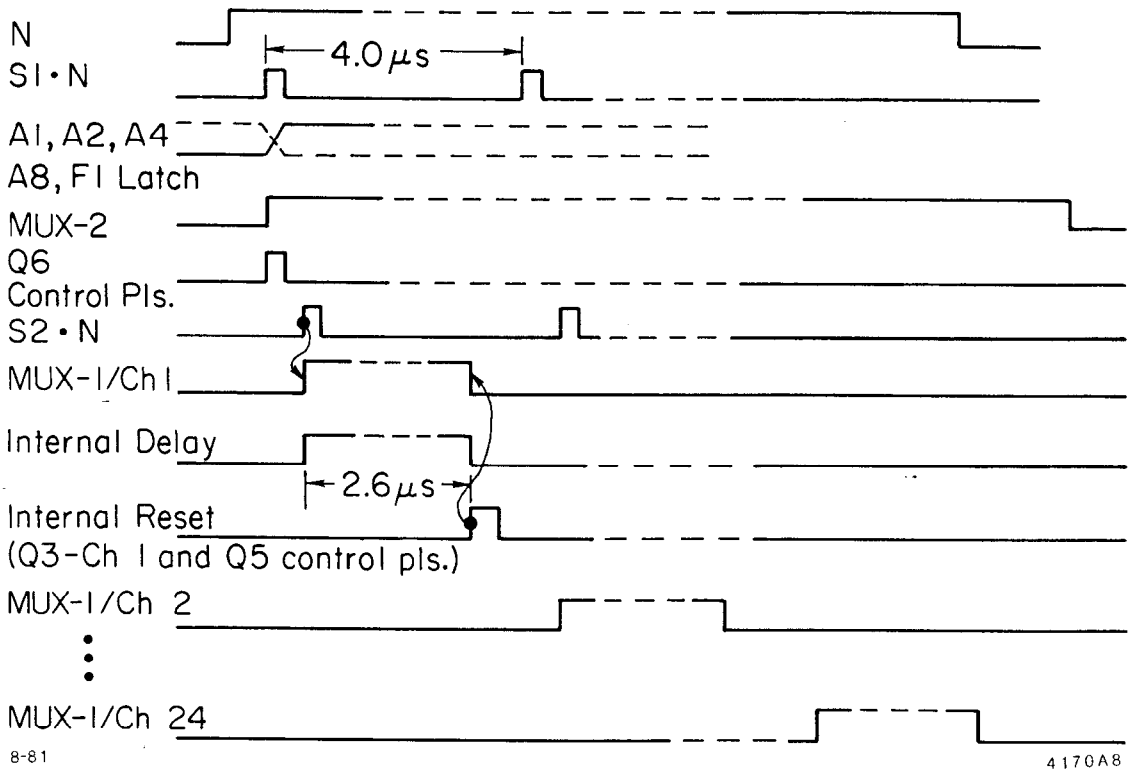

Fig. 8. ISHAM: The READ-OUT Timing Diagram.

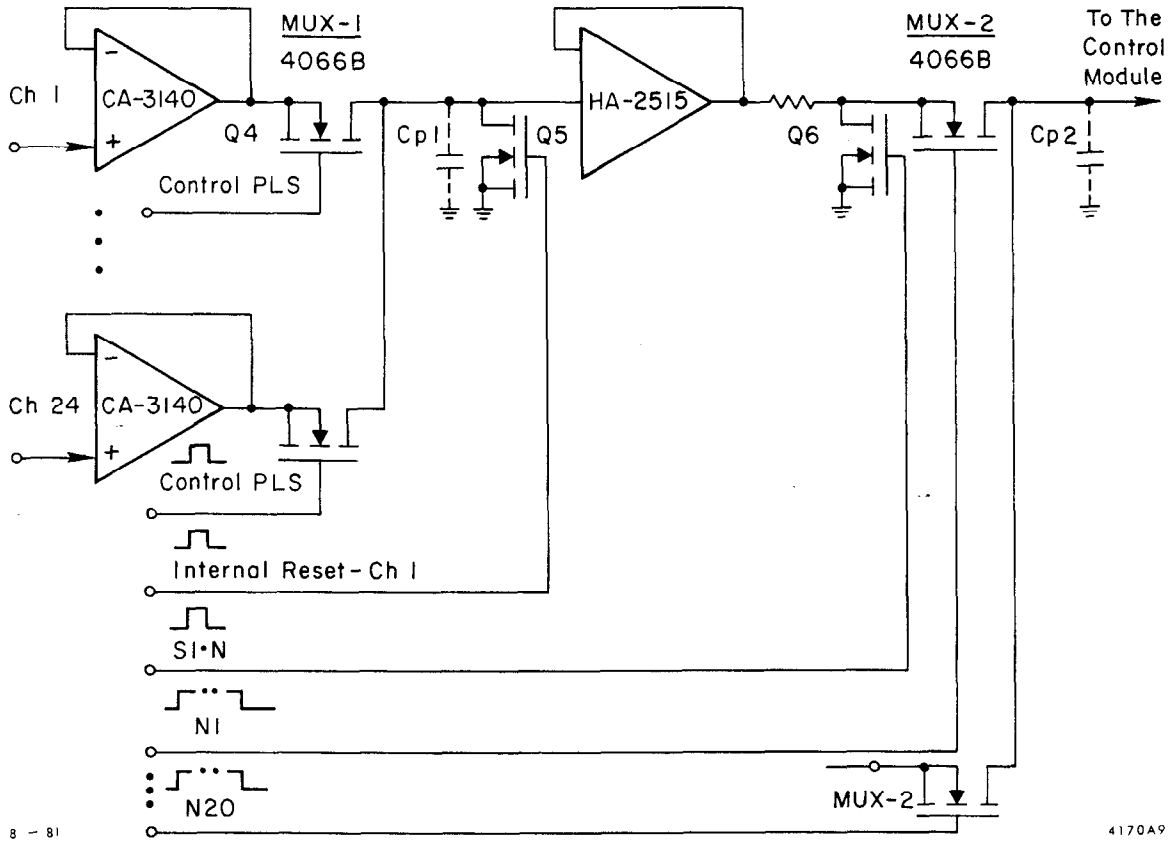

Fig. 9. ISHAM: The Analog Multiplexer.

C. The ISHAM Calibration

The calibration scheme is based on a 4-bit serial/parallel shift register, Fig. 10. The 24 channels are organized in four groups of ODD channels and four groups of EVEN channels, three channels each. These four groups of ODD and EVEN channels are addressed by the 4-bit shift register. By using two extra control lines -- ODD and EVEN -- the calibration mode is selected by the pattern loaded into the shift register combined with the state of the ODD and EVEN control lines. A step function, whose height is set by the computer program, is supplied to the calibration capacitors. In this way, a known amount of charge is transferred to the selected channels. The step function is generated by fast FET-switches.

D. The Neutral Trigger Circuit

Two signals are provided by the neutral trigger circuits for the purpose of trigger decision:

1. An analog signal which is proportional with the total charge collected by the 24 wires connected to an ISHAM module, each beam-crossing cycle.

2. A digital signal of a constant level is generated each time the charge collected by the 24 attached wires is greater than a minimum presetted value. The threshold corresponding to the minimum amount of charge is remote controlled.

The block diagram of the Neutral Trigger circuits is shown in Fig. 11.

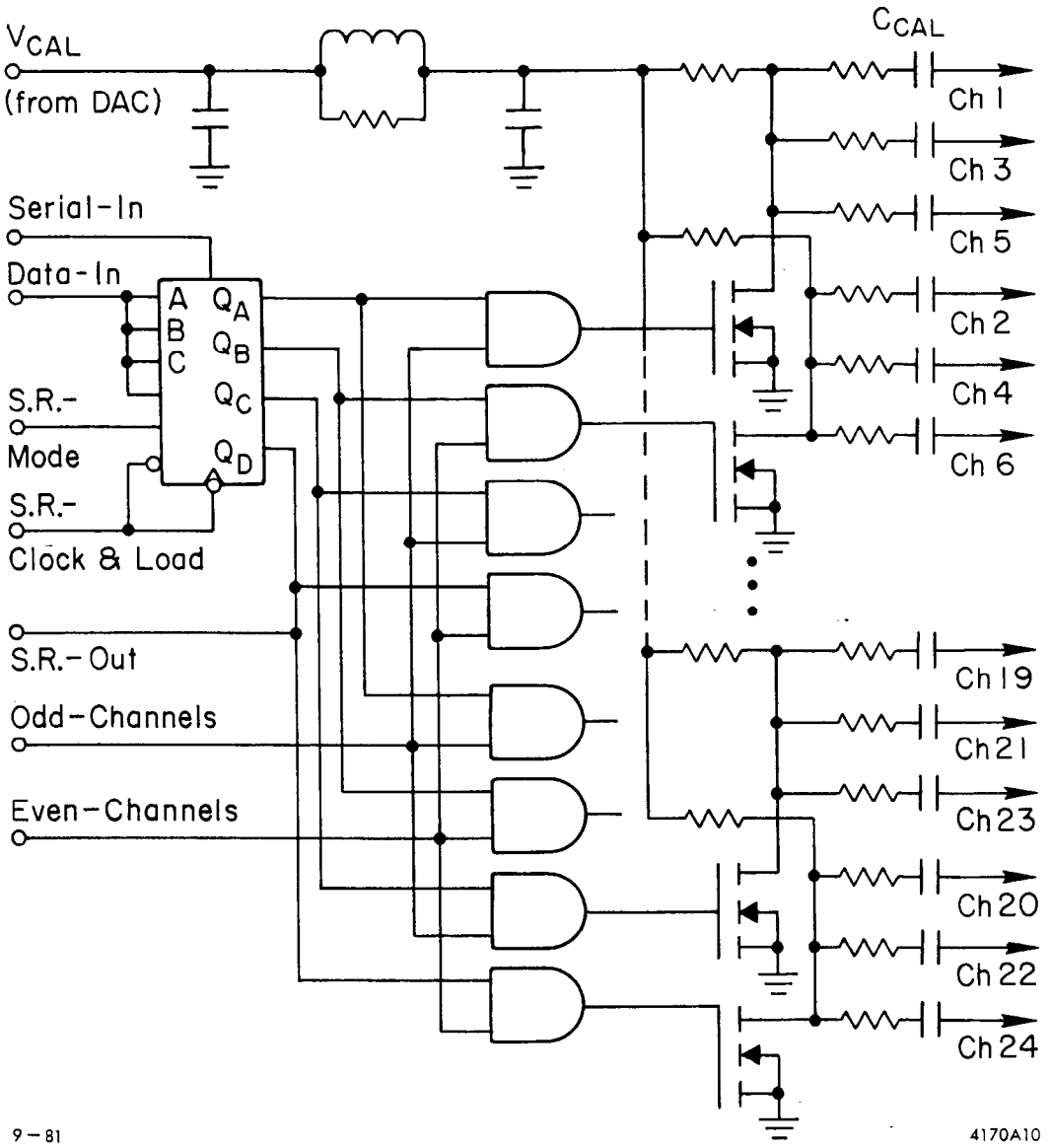

Fig. 10. The Calibration Scheme.

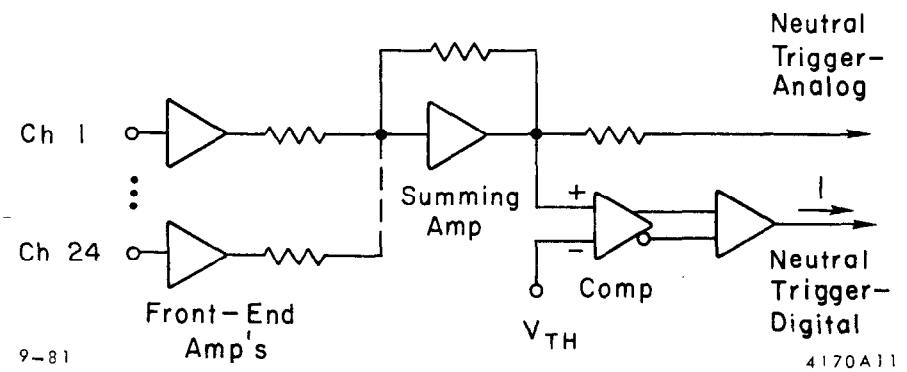

Fig. 11. The Neutral Trigger Block Diagram.

The ISHAM Performances

1. Voltage Gain : 1,000 (5 V output voltage @ 20 pC input charge).
2. Charge Gain : 60.
3. Linearity : better than 0.1% f.s.

   The gain characteristic, Fig. 12, measured with the BADC, shows that quadratic correction might not be necessary. The characteristic fitted to a straight line shows $\sigma_{fit} \leq 4$ channel. Therefore the integral non-linearity is better than 0.1% f.s.
4. Noise : A typical histogram is shown in Fig. 13. $\sigma_{noise} = 1.15$ ch ($\sim$ 6 fC) for the whole system.
5. Crosstalk : less than 1%.
6. Z-position Resolution : 1%.
7. Density and Size : 24 ch/module, multilayer P.C. board 20" x 17.58". A module view is shown in Fig. 14.

ACKNOWLEDGEMENT

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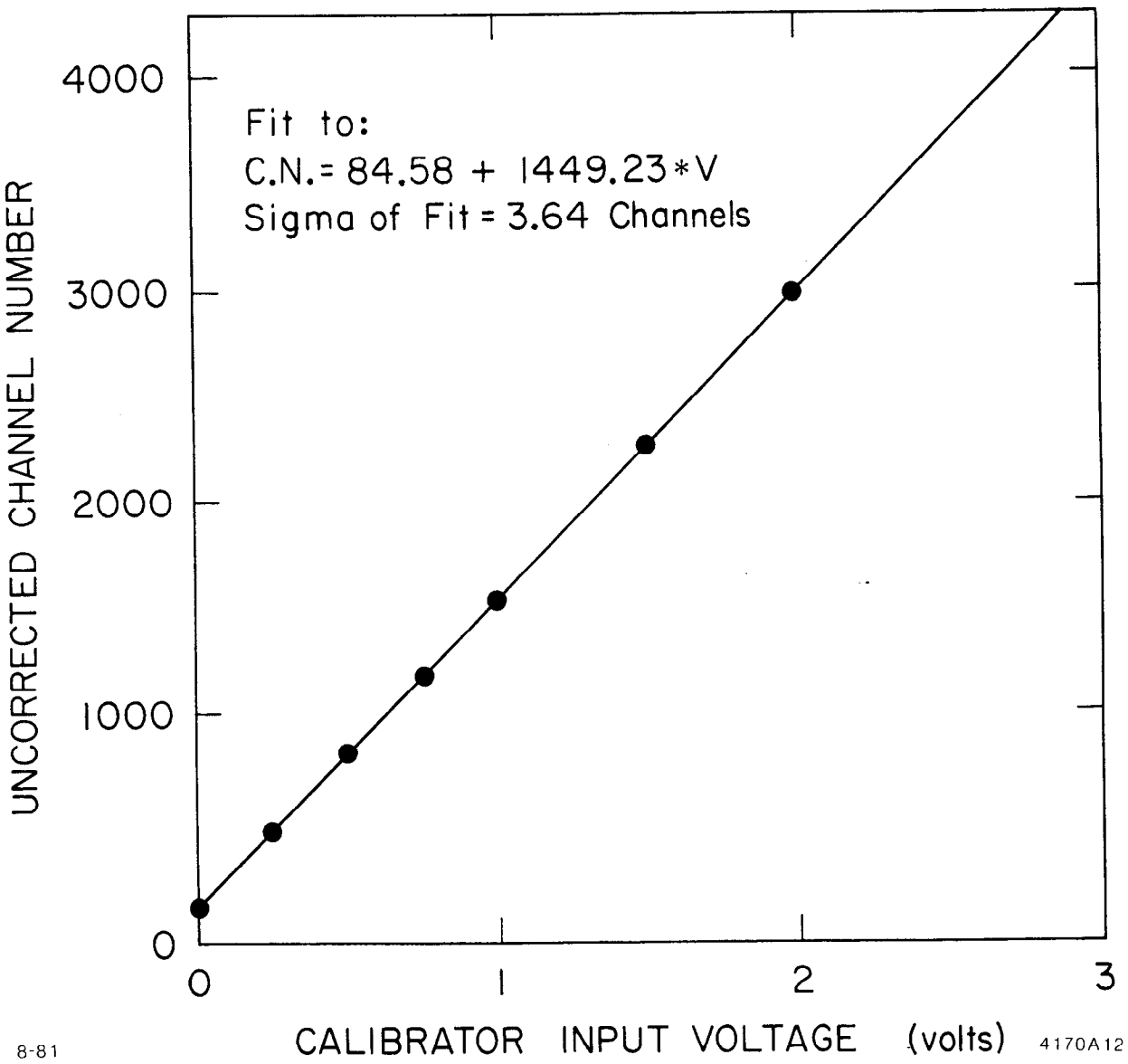
Fit to:
C.N.= 84.58 + 1449.23*V
Sigma of Fit = 3.64 Channels
UNCORRECTED CHANNEL NUMBER
4000
3000
2000
1000
0
0
1
2
3
CALIBRATOR INPUT VOLTAGE (volts)
8-81
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Fig. 12.

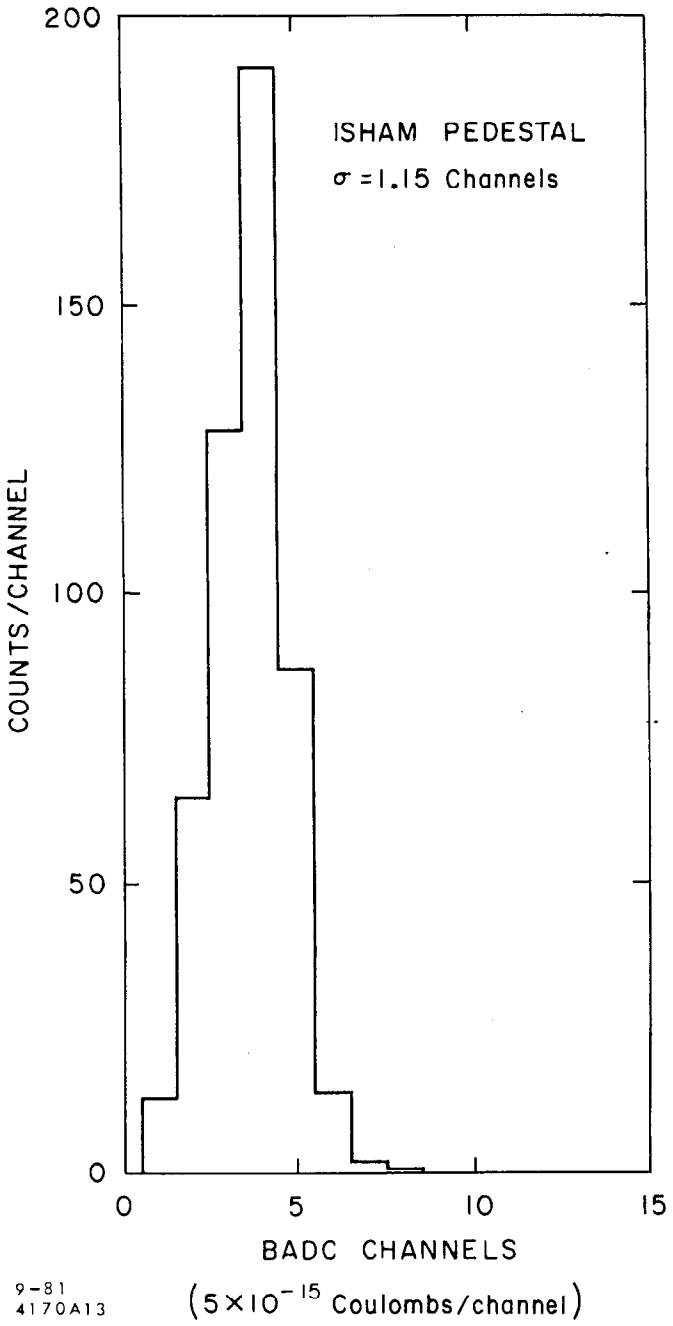

Fig. 13. ISHAM: Noise Measurement.

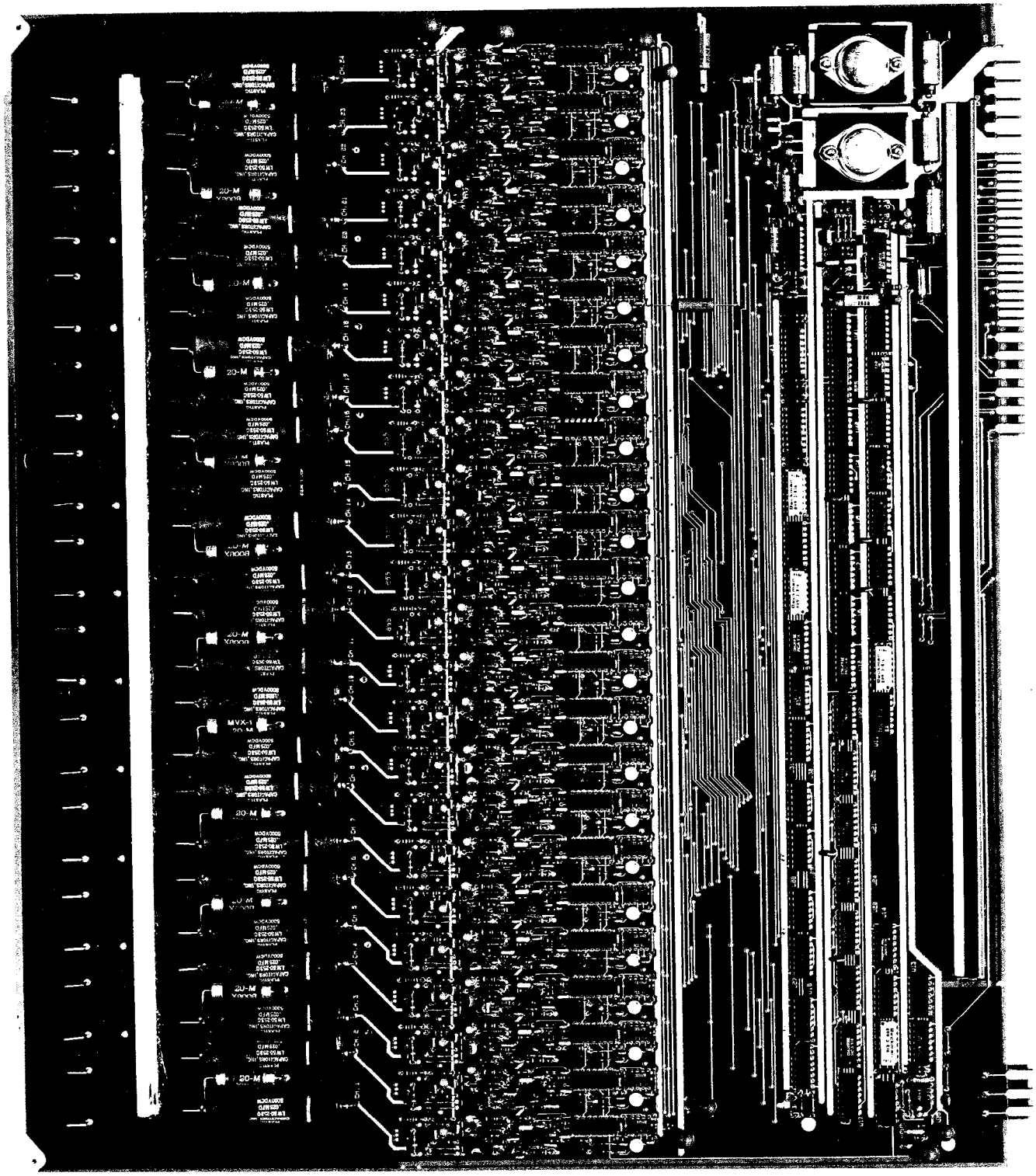

Fig. 14. ISHAM: The Module View.

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