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THE FASTBUS STANDARD - A REVIEW OF THE CURRENT STATUS*

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Abstract

The new FASTBUS standard is nearing finalization, and a prototype test program has been underway for the past 18 months. This paper reviews the objectives, current status and future directions of the FASTBUS standard.

Introduction

In 1976, a group of physics laboratory users studied the need for a next generation data acquisition system and issued a report[1] outlining the performance goals for such a system. The Fast System Design Group (FSDG), under the auspices of the U.S. NIM Committee, the standards group responsible for NIM[2] and CAMAC[3], has since then been developing a new standard, the FASTBUS, which will meet the original design goals. Progress of this activity has been reported at regular intervals.[4-7] This standard will be complete in October of this year. Prototypes have been built and tests of the system protocols, speed and hardware are proceeding.

Design Goals

The principal goals were set and met as follows:

(a) Highest possible speed - at least an order of magnitude improvement over CAMAC. Current tests indicate that the bandwidth is at least 80 megabytes/sec in block transfer mode and approximately 20 to 40 megabytes/sec in a random address mode.

(b) Variable speed - the system in general operates in a full handshake mode which allows different speed devices to be used, but also allows synchronous transfers to be used for maximum transfer speed.

(c) Multi-processor capability - multiple masters (up to 31 within any segment) are accommodated which allows data to be processed at any level within the system, which in turn reduces the overall quantity of data which must be transmitted through the system. The arbitration scheme which enables the multiple-master scheme is position independent.

(d) Uniformity of protocols - the protocols are uniform system wide and are not based on any specific technology. The protocols also permit macro operations which are essential in a multiprocessor environment.

(e) Logical addressing - a device's address is independent of its position on a segment.

Essential Features of FASTBUS

(1) The Segment

The smallest piece of a FASTBUS system is called the Segment. It may be implemented in a backplane or a cable. A collection of Segments which may be virtually arbitrarily interconnected make up a total FASTBUS system. Each segment may contain up to 32 devices which may be either Masters (31 maximum) or Slaves.

(2) Arbitration

In order to facilitate the potential use of multiple processors within Segments, an arbitration scheme has been provided which allows devices to arbitrate amongst themselves for the use of the bus. The arbitration protocol permits overlapping of the arbitration with an operation already in progress. A voluntary fairness protocol is available to ensure as far as possible that every potential master eventually gets to use the bus.

(3) Protocols

FASTBUS protocols are specified in logical form, i.e., the protocols are technology independent. The protocols are uniform, whether used on a backplane or a cable (this is very different for example from CAMAC, where the protocols vary depending on whether a Dataway or a Branch Highway is used).

Table I lists the signal lines required to implement the FASTBUS protocol.

TABLE I

FASTBUS Signals

Mnemonic	Signal Name	Lines Required	Comments
AR	Arbitration Request	1	For bus arbitration
AG	Arbitration/Grant	1	
AI	Arbitration Request Inhibit	1	
AL	Arbitration Level	6	
GK	Grant Acknowledge	1	
AS	Address Sync	1	For addressing and status of connection
AK	Address Acknowledge	1	
WT	Wait	1	For data transfer control and status
CB	Control/Block	1	
NH	No Handshake	1	
BK	Busy Acknowledge	1	
NK	Negative Acknowledge	1	
RD	Read	1	
AD	Address/Data	32	
PE	Parity Enable	1	
PA	Parity	1	
DS	Data Sync	1	
DK	Data Acknowledge	1	
RB	Reset Bus	1	
BH	Bus Halted	1	
EG	Enable Geographic	1	
SR	Service Request	1	
TX	Transmit Serial	1	For diagnostics
TR	Receive Serial	1	
TP	T-Pin (not bussed)		For special purpose protocols

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The bus uses 32 lines for time-multiplexed address and data. Parity and parity enable are available at the discretion of the designer. The defined protocols include fully handshaked and some non-handshake operations; operations may be to a single listener or to multiple listeners (Broadcast). Table II is a list of currently defined FASTBUS operations.

TABLE II

FASTBUS Operations

CYCLE Address CB	CYCLE Address NH	CYCLE Data CB	CYCLE Data NH	Function
0	0			Single Listener (Data Space)
		0	0	Single Word, Handshake (HS)
		0	1	Block Transfer HS
		1	1	Block Transfer Non-HS
		1	0	Extended Address, HS
1	0			Single Listener (Control Space)
		0	0	Single Word, Handshake (HS)
		0	1	Block Transfer HS
		1	1	Block Transfer Non-HS
		1	0	Extended Address, HS
0	1			Broadcast (Data Space)
		0	0	Single Word, System - HS
		0	1	Block Transfer, System - HS
		1	1	Block Transfer, Non-HS
		1	0	Extended Address, System - HS
1	1			Broadcast (Control Space)
		0	0	Single Word, System - HS
		0	1	Block Transfer, System - HS
		1	1	Block Transfer, Non-HS
		1	0	Extended Address, System - HS

(4) The Segment Interconnect (SI)

A device, called the Segment Interconnect, is specified which permits a message originating in one segment to be passed on to or through any other segment. The protocol is such that the passage of such a message is transparent to the device sending it. A prototype SI is being built at the University of Illinois, and will be tested in the near future.

The SI performs the message routing by means of look-up-tables which are set by the system initializer. Each SI has two such tables, one for outbound messages and one for inbound messages. By suitably setting up the tables in all the SI's, one can readily visualize that any segment can be connected to any other, thus providing unique and optimum paths for all transactions.

(5) Address Space Allocation

FASTBUS has a 32-bit address field and all devices are normally logically addressed and therefore position independent in the system. In addition, devices can be geographically addressed using the lowest 5-bits of the address field on each segment. This allows access for initialization of a system where logical addresses are loaded by software.

A 32-bit address space is certainly quite large, especially since it may be arbitrarily extended. An important feature of FASTBUS is the concept of a protected control space, which is defined by the state of the Control/Block line at address time. This helps to prevent an overrun of data addressing to inadvertedly altering some control register.

For purposes of address space allocation, the most significant bits are used to define the range of address being used within each segment. Initial implementations will have an 8-bit segment field which permits a FASTBUS system to be segmented into 256 segments, each having an address range of 2^{24}. Within each segment, the lowest 256 addresses are reserved, and the first 32 are assigned for Geographic Addressing. By virtue of this address allocation, it is possible for every slot in a system to be uniquely accessed.

(6) Hardware

(a) The Module

A standard printed circuit card for the module is specified. It uses a box type, 1" grid 2 × 65 (130) position connector for connection to the FASTBUS and power. Space is also available for an auxiliary connector of up to 3 × 44 (132) positions. The card dimensions are approximately 12.70" × 16.26".

This standard module will be used independent of cooling method chosen. It is most important that all modules be truly interchangeable within any FASTBUS system.

(b) The Crate

A standard Type A (air-cooled) crate is specified for use in a 19" rack. This crate permits 26 modules to be installed on a .65" pitch. In this configuration, the maximum component height is .4". A Type W (conduction cooled) crate will also be specified, which accommodates 20 modules on a 0.85" pitch.

(c) The Backplane

Fifty (50) prototype backplane have been built. Tests have been performed on the signal transmission quality and also on the power distribution. These backplanes can readily handle 3 KW power without any significant voltage drops (< 2 mV worst case) between any pins.

(d) Cooling

Prototype air handler units have been built and tested for air cooled systems. These units are capable of readily removing up to 5 KW of heat in a rack system. Evaluation tests are proceeding on various configurations of closed loop systems, and some results are available. Currently design and construction is proceeding to evaluate several possible conduction cooling and heat exchange methods, both at SLAC and at BNL. Individual integrated circuits with up to 2 watts of power can be readily accommodated with current techniques. For very high power IC's, such as gate arrays, etc., more work will have to be done using possibly heat pipes, special refrigeration techniques, or special heat-sink arrangements.

(e) Power

In the standard connector, pins are designated for the standard voltages, i.e., +5V, -5.2V, -2V, 0V, ±15V, and a bulk +28V. The prototype backplanes include studs for connecting appropriate power supplies, according to the choice of the system designer. However, standard recommended power supply combinations are being developed.

Plans are under way to make backplanes, crates, power supplies and cooling hardware available from commercial suppliers.

(7) Software

An integral part of the process of developing the FASTBUS standard has been the contribution made by the Software Design Group (SWDG). This has led to not only the definition of bits in registers, etc., but also the

creation of a defined diagnostic capability including an Ethernet-like serial link. For details see D. Gustavson's paper at this conference.

Prototype Test Program

For the past 18 months a prototype test program has been underway to demonstrate the functionality of the system. In conjunction with this, some specialized hardware has been built, the major units being a high speed sequencer module, memory module, I/O module, and arbitration logic. These devices have been used to perform single-segment tests of the various protocols. Tests have been successful within the expected limitations of the devices (e.g., 125 nsec per word transfer rate). Some minor refinements (look-ahead) will be implemented in the sequencer which should approximately double this speed. The sequencer, memory and arbitration logic all use very high speed ECL logic throughout.

Two other important modules, a Snoop (diagnostic module) and Segment Interconnect are designed but not completely built. Although some hardware has been built for the Ethernet-type serial link, the Snoop is the major component necessary to complete a diagnostic system with independent access to any segment to which the Snoop is connected. The Segment Interconnect is the fundamental component needed to test the arbitration and addressing mechanisms across the segment boundary.

Both the above prototypes are close to completion. Once built, a multi-segment series of hardware and software tests will be performed. The hardware will include at least two FASTBUS Segments and an SI. Software will include initialization and route-map generation packages, as well as the diagnostic system software using the Snoop. The goal is to have this test operational by late summer of 1981.

Following the prototype tests, and subsequent early finalization of the specification, efforts will be made to make the basic information available to other laboratories and potential manufacturers.

Future Developments in FASTBUS

As time and manpower permit, further efforts will be initiated on several additional system components, including a high speed parallel computer-to-FASTBUS port (most likely candidate: VAX 11/780) and a high speed serial link. Although FASTBUS was initially designed to accommodate very high-speed data acquisition systems, the architecture of the system readily supports a wide variety of systems, especially in distributed control.[8] One of the most important developments in the near future will be the standardization of serial links, both for point-to-point and for multi-drop connections. The future Ethernet devices under development by manufacturers will support a 10 MHz bit-serial baseband system which makes this a good candidate for intermediate speed serial applications. A higher speed version using some other transmission medium may be the next logical development for FASTBUS.

Conclusion

The FASTBUS development is nearing completion, and will be available as a tentative standard in October 1981. FASTBUS offers an extremely versatile way of implementing future systems requiring distributed processing or control as well as very high-speed data acquisition.

Acknowledgements

The FASTBUS effort involves a very large contingent from most of the major laboratories, including some European laboratories. The contributions of the prototype team at SLAC and U of I are especially acknowledged.

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