SLAC-PUB-2742
May 1981
(I/A)

# SLAC CAMAC CRATE CONTROLLER CCU2 WITH AUXILIARY CONTROLLER BUS INTERFACE*

H. Walz and J. Olsen
Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

## Abstract

The development of a new CAMAC type U crate controller, compatible with the SLAC parallel branch highway, is described. The controller also provides an interface for the Standard Auxiliary Controller Bus, control and timing logic to implement a handshake system between the host computer and the crate controller, an internal timing generator for Dataway cycles, and a LAM handling facility with priority arbitration along the parallel branch highway. A highly integrated module implementation was achieved through extensive use of firmware and finite state logic machine realizations of many crate controller functions.

## I. Introduction

When the first multicrate CAMAC systems were implemented at the Stanford Linear Accelerator Center (SLAC), a simple parallel branch highway was defined, connecting up to 7 crates. In contrast to the standard CAMAC branch, this SLAC branch utilizes binary coding of crate addresses, direct transmission of strobe signals S1 and S2 from the branch driver to the crates, common Clear (C) and Inhibit (I) signals, and signal transmission with single wires only. This SLAC branch reduced cabling and connector requirements and permitted development of a simple, transparent crate controller[1] containing only drivers and receivers and two decoding circuits. Since no handshaking is used and the strobe signals are transmitted along the branch, the CAMAC cycle duration is lengthened as required for reliable control of the most distant crate. The majority of CAMAC systems in operation at SLAC today are based on this SLAC branch and operate with cycle periods of 4 to 10 μsec typically.

The specification of the Auxiliary Controller Bus (ACB), which allows the use of several controllers in each crate, has led to the development of a new SLAC crate controller and the addition of 2 handshake signal lines to the SLAC branch. This crate controller, CCU2, retains compatibility with existing CAMAC systems at SLAC. By utilizing 2 new handshake signal lines on the SLAC branch and a standard ACB interface, the use of standard, commercially available auxiliary controller modules is possible. The handshake logic combined with an internal timing generator for Dataway cycles, provides a substantial speed increase over very long branches. A LAM handling facility with priority arbitration along the branch, and programmable control flags for local execution of CIZ commands are among other new features available.

## II. Crate Controller Description

A block diagram of CCU2 hardware is shown in Fig. 1. The branch interface is shown across the top, the crate Dataway interface across the bottom, and the ACB connection at the left side of the diagram. All interface receiver inputs have hysteresis for noise rejection. All driver outputs are of the open collector type. Logic levels on branch, Dataway, and ACB are low true; required pull-up resistors are omitted from the diagram for clarity reasons. From left to right, the block diagram first shows request-grant logic, encoded N inputs and buffered, parallel L outputs for the ACB. The Dataway N decoder derives its input from the branch or the ACB, based on who is in control of the crate. A special N25 decoder, driven by the branch only, is provided to address the programmable features of the crate controller itself. Interfacing of branch read-write data lines to Dataway R and W busses is handled by re-

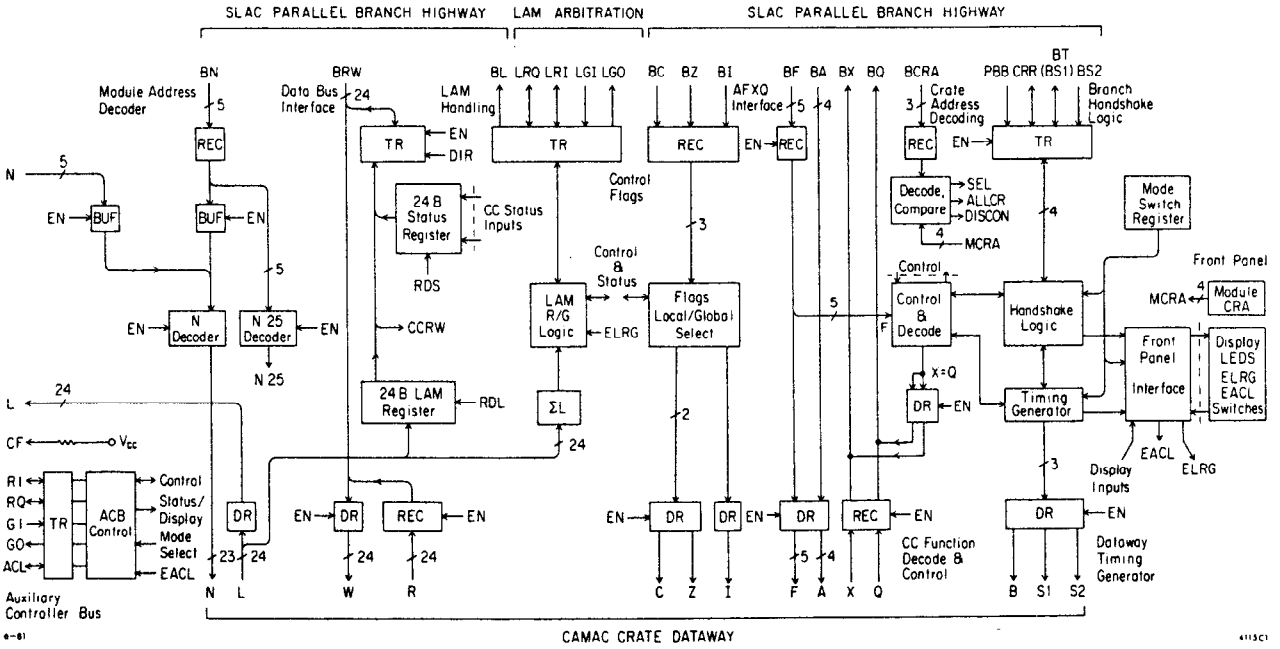


Fig. 1. CCU2 Block Diagram

* Work supported by the Department of Energy, contract DE-AC03-76SF00515.

(Contributed to the Topical Conference on Computerized Data Acquisition in Particle and Nuclear Physics, Oak Ridge, Tennessee, May 28-30, 1981.)

ceivers and drivers; connection of the internal CCU2 bus is by transceivers. The internal data bus serves a LAM read register, a status read register and a distributed control word write register. LAM handling logic with request-grant connections to other crates, and programmable flags for local execution of CIZ commands are shown in the center of Fig. 1. The interface for Dataway F lines uses 2 levels of gating, such that internal control and decoding logic is accessible from the branch without gaining control of the crate. Finally, crate address decoding, branch handshake logic, the internal dataway timing generator, and front panel interface hardware complete the crate controller. The major functional parts of the CCU2 module are described next.

## A. Branch Handshake Logic and Dataway Timing Generator

Proper timing and synchronization, with autonomous controllers at the crate level and with long branch cable delays, is achieved with the use of 2 new handshake signal lines, Parallel Branch Busy (PBB) and Crate Ready (CRR). A typical branch and Dataway cycle is shown in Fig. 2. At the start of each cycle the

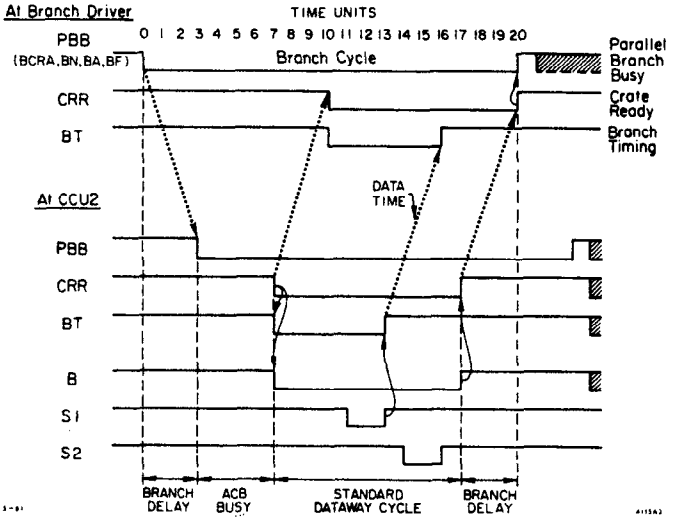


Fig. 2. Timing of Branch Handshake and CCU2 Dataway Cycle.

host computer branch driver issues a PBB. After PBB is received by the addressed crate and after the crate controller has gained control of the crate through ACB priority arbitration, it returns CRR to the host computer. Now a standard CAMAC cycle is executed by the timing generator. The Branch Timing (BT) line is asserted at the start of the cycle and reset at the end of S1 strobe time. This signals data time to the branch driver. A special LAST CRATE feature of CCU2, set by a manual mode switch in the module, allows the generation of CRR and BT by the most distant crate along the branch highway during operations addressed to all crates and global control commands. Also timing cycle durations of 1 μsec or 2μsec may be selected by the manual mode switch. Hardware implementation of this handshake system and the timing generator is shown in Fig. 3. All combinatorial and sequential state logic for the handshake control and the timing generator is realized with firmware programming of a field programmable logic sequencer (FPLS) circuit.

## B. ACB Control

The standard ACB interface for distributed controllers at the crate level has been implemented according to DOE/EV-0007. The parallel branch gains control of

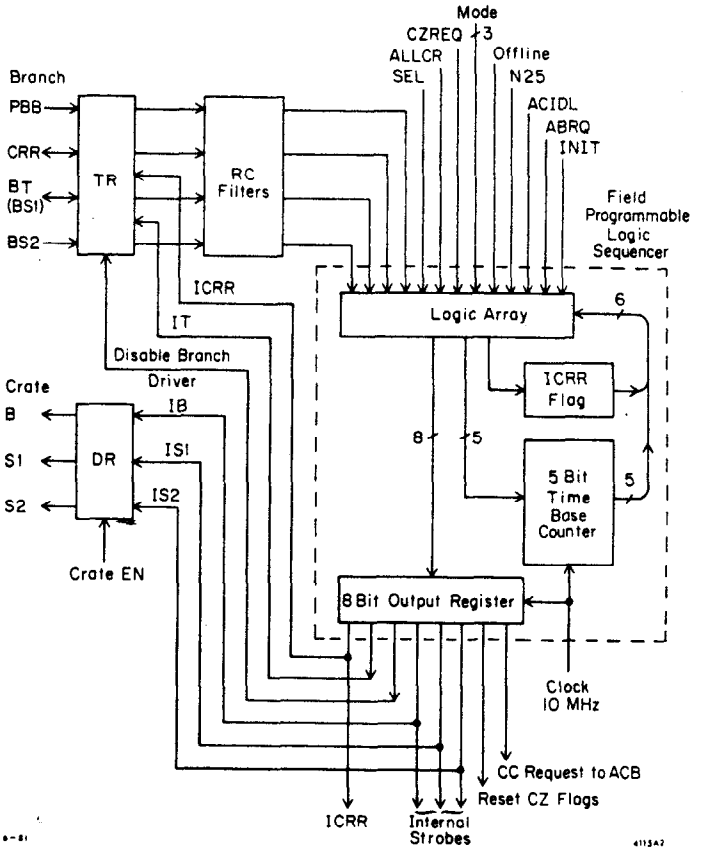


Fig. 3. Branch Handshake Control and Crate Timing Generator.

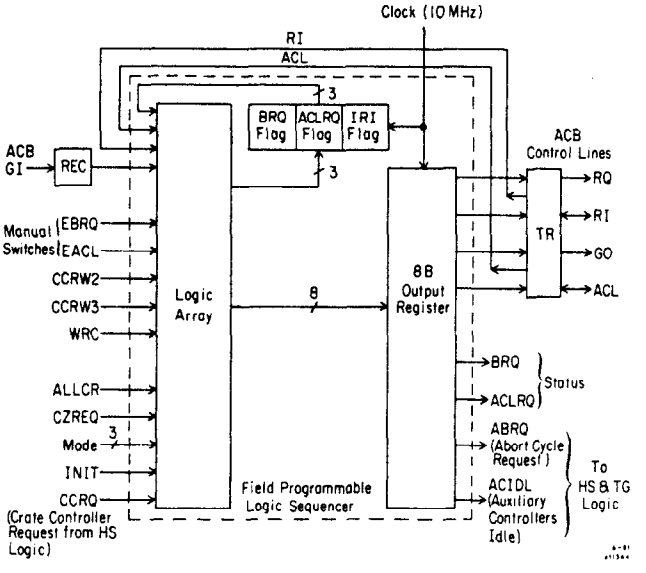


Fig. 4. ACB Control Logic.

the crate Dataway through the ACB request-grant logic. This is shown in Fig. 4. Four arbitration modes selected by 2 program flags, Branch Request (BRQ) and Auxiliary Controller Lockout Request (ACLRQ), are available:

| BRQ | ACLRQ | Arbitration Mode |
|---|---|---|
| 0 | 0 | Normal Request-Grant Each Cycle |
| 0 | 1 | ACL Arbitration Each Cycle |
| 1 | 0 | Request-Grant Arbitration with Control Maintained for Block of Cycles |
| 1 | 1 | ACL Arbitration with Control Maintained for Block of Cycles |

Both flags have to be anabled by manual switches before they may be set under program control. After a Crate Controller Request (CCRQ) from the branch handshake logic is received, an ACB arbitration is performed. Once the Request Inhibit (RI) line has been asserted and auxiliary controllers have released control of the Dataway, the ACIDL signal is returned to the handshake logic and timing generator. Now Dataway cycles by CCU2 may commence. Branch cycle requests addressed to all crates and global and local clear and initialize (CZ) cycle requests will cause a forced ACL arbitration, independent of the status of the control flags.

## C. LAM Handling System

All Dataway LAM lines are staticized in the LAM register and readable from the host computer with a standard CAMAC read cycle addressed to the crate controller as a module (N25). After buffering they are also available as part of the ACB interface. For implementation of a LAM system, comprised of several crates along the branch and the host computer, the CCU2 crate controller provides a LAM sum output, a LAM sum masking flag, and a LAM request-grant priority arbitration circuit (Fig. 5).

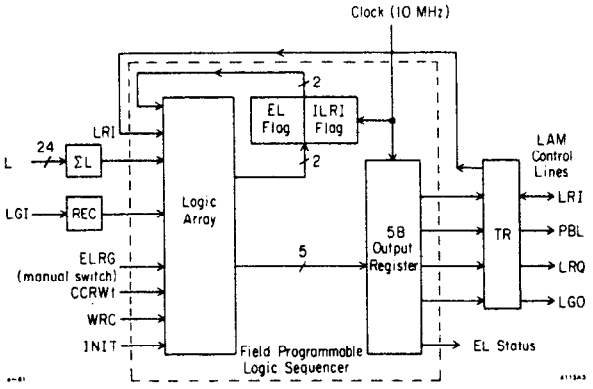


Fig. 5. LAM Crate Priority Logic.

Under control of the programmable EL masking flag, the ΣL signal is enabled onto the branch LAM bus line and into the LAM request-grant logic. With rear panel connections a ΣL priority arbitration scheme can be set up between several crates along the branch. Three signal lines (LRQ, LRI, LGI-LGO) have to be bussed or chained between crates in order of crate controller priority. The front panel switch ELRG enables or disables participation of a crate in the arbitration process.

Crate controllers post ΣL signals on the branch BL line and resolve priority with the request-grant system. The highest priority CCU2 will establish the LAM request inhibit signal (LRI). To obtain the LAM source information the following steps are taken:

a. The host performs a read cycle to <u>all crates</u> with a special read status word command. The highest priority CCU2 will respond with its status word on the data bus, which contains the crate address.

b. A LAM data read cycle to the highest priority crate returns the LAM source data.

c. A control word write command masking the BL signal in CCU2 or an equivalent operation to all active LAM sources in modules will remove the ΣL input to the request-grant logic and allow a new arbitration cycle.

## D. Programmable CIZ Control Command Flags

The use of branch CIZ command lines and 3 programmable flags in CCU2, provides a choice of global or local execution.

a. <u>Inhibit Control</u> - The Dataway Inhibit signal I is generated in response to the branch BI signal and the internal I flag. The branch BI input can be disabled by an internal manual mode switch. An initialize cycle generated by the crate controller will also set the I flag.

b. <u>Clear and Initialize Control</u> - The Dataway Clear (C) and Initialize (Z) signals are generated in response to the branch BC and BZ signals or 2 programmable flags. Execution of branch BC and BZ commands requires crate address CR7 (all crates) and utilizes a forced ACL mode to gain Dataway control. Generation of Dataway C and Z signals is accompanied by a standard timing cycle as supplied by the branch or the internal timing generator. Execution of C and Z flags utilizes a forced ACL mode and an internal timing cycle. Both flags are reset at the end of this cycle. Power-up initializes the crate.

# III. Operational Description

The operation of CCU2 may be programmed by control word flags, front panel manual switches, and internal PC board switches. The control word flags for ACB arbitration (BRQ, ACLRQ), for LAM handling (EL), and for local CIZ control commands have been described in Sect. II.

Front panel switches are easily accessible for setup changes and diagnostic work:

| Crate Address MCRA | Description |
|---|---|
| 0 to 6 | Crate Address |
| 7 | All Crates |
| 8, 9 | Branch Disconnect |

Branch Disconnect settings 8 and 9 will logically disconnect the crate from the branch.

ELRG - Enables crate for LAM priority arbitration
ACLRQ - Enables programmable ACLRQ flag
OFFLINE - Crate Dataway is offline; host may access CCU2 internal features.

Internal PC board switches are provided for mode selection prior to crate controller installation:

EBRQ - Enables programmable BRQ flag
EBI - Enables branch BI input for global inhibit control.

| de Switch egister | Description |
|---|---|
| 0 | Old SLAC branch mode; no handshake; |
| 1 | Old SLAC branch mode; no handshake; Last Crate; |
| 2 | PBB-CRR handshake; branch driver timing; |
| 3 | PBB-CRR handshake, branch driver timing; Last Crate; |
| 4 | PBB-CRR handshake; Timing generator 1 μsec cycle; |
| 5 | PBB-CRR handshake; Timing generator 1 μsec; Last Crate; |
| 6 | PBB-CRR handshake; Timing generator 2 μsec cycle; |
| 7 | PBB-CRR handshake; Timing generator 2 μsec cycle; Last Crate; |

The setting of all manual switches is readable om the status register. Some of the switch and pro-am flag settings are also displayed on the module ont panel.

The following set of CAMAC codes may be used by the st computer to operate the internal features of the ate controller:

| | | |
|---|---|---|
| 25·F0) | - | Read Status Word |
| 25·F1) | - | Read LAM Data Word |
| 25·F4) ILRI | - | Read Status Word; CCU2 with LRI asserted will return data; |
| 25·F8) | - | Test LAM Sum; |
| 25·F16) | - | Write Control Word; |
| C+CFLAG) | - | Crate Clear Command |
| Z+ZFLAG) | - | Crate Initialize command; resets flags EL, BRQ, ACLRQ; sets IFLAG; |
| I+IFLAG) | - | Asserts crate Inhibit line; |

## IV. Prototype Hardware

A prototype module has been fabricated and is being sted extensively. Firmware and finite state logic chine realizations of most crate controller functions sulted in a highly integrated, state-of-the-art dule implementation with only 50 integrated circuit ckages. Figure 6 shows the wirewrap S24 board of the prototype module, which carries most of the logic. Production models will utilize simple, 2-layer PC boards. To eliminate all discrete wiring to the front panel and for board-to-board connections, the front panel assembly is based on a 4-layer PC board and staked pin connectors. Figure 7 shows the multilayer board with all components loaded and the complete assembly.

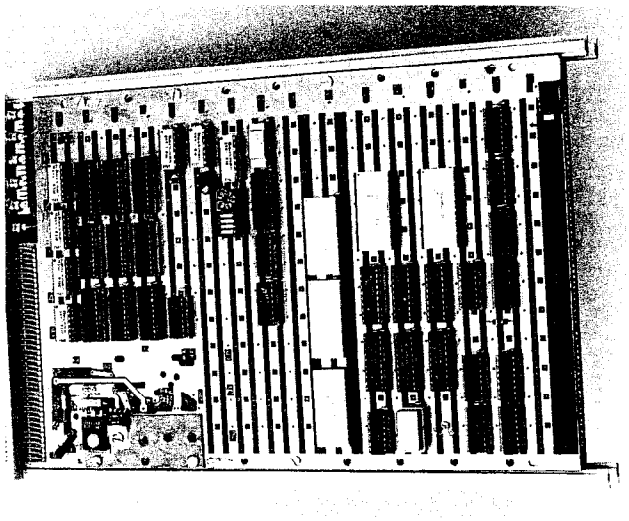

Fig. 6. CCU2 Prototype S24 CAMAC Board.

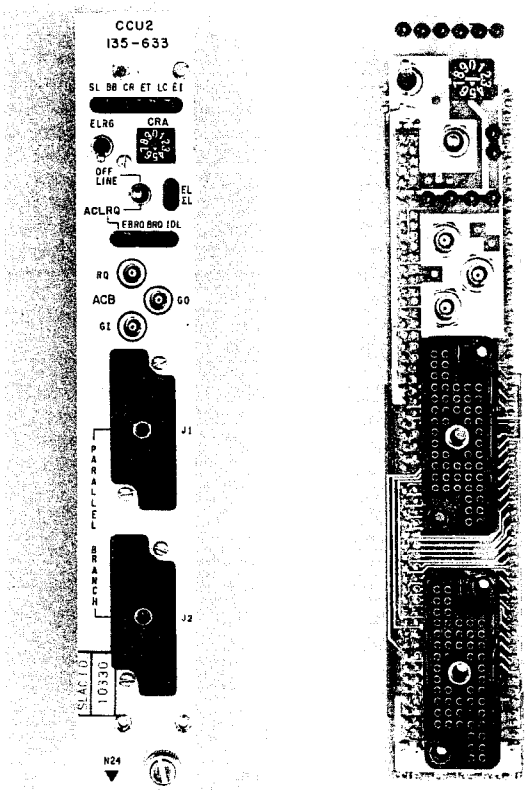


Fig. 7. CCU2 Front Panel PC Board and Assembly.

## V. Summary and Acknowledgments

The new SLAC CAMAC crate controller CCU2 has been described. This unit remains compatible with the SLAC parallel branch and first generation SLAC crate controllers, while offering many new features and capabilities. Included are a standard ACB interface, a branch handshake system, an internal timing cycle generator, a LAM handling system, and programmable CIZ control flags. Advanced design and packaging concepts have kept the expected production cost comparable to presently used crate controllers. In order to fully exploit CCU2 in future CAMAC systems, host computer interfaces, branch drivers, and other system modules will have to be upgraded in a similar fashion.

Basic specifications for CCU2 are summarized in Table I.

Finally, we would like to acknowledge ideas contributed by L. Paffrath and the support of this development effort by R. Larsen.

## References

1. Simple, Versatile CAMAC Crate Controller and Interrupt Priority Encoding Module, Dale Horelick, Stanford Linear Accelerator Center; IEEE Nuclear Science Symposium, Washington, D.C., Dec. 1974.

Table I. CCU2 Features and Basic Specifications

- CAMAC type U crate controller compatible with SLAC parallel branch.
- Branch handshake logic for synchronization with auxiliary controllers and timing of Dataway cycles over branches with long cable delays (PBB, CRR, BT).
- Last Crate feature for branch handshake during global C and Z cycles and operations to all crates.
- Standard ACB interface based on DOE/EV-007.
- 4 Arbitration modes with ACB, utilizing 2 programmable flags (BRQ, ACLRQ).
- Internal Dataway timing generator with selectable cycle duration (1 μs or 2 μs).
- 24 Bit LAM latch.
- LAM OR sum and masking flag (EL) to generate branch LAM output.
- LAM request-grant logic for arbitration between several crates with front panel enable switch.
- Crate controller internally addressable from branch while ACB is busy.
- Internal registers for control and status data.
- Choice of global or local execution of C, I, Z commands by use of 3 control word flags.
- Mode of operation selection by manual switches on front panel and inside module; setting of all switches readable with status word.
- Special Offline and Branch Disconnect modes.
- Hysteresis inputs at all branch and crate receivers for noise rejection.
- Firmware and finite state logic machine realization of most crate controller functions.
- 4-layer PC board and staked pin connectors for front panel and all needed connections.
- Simple 2-layer PC boards with 50 IC packages in standard 2-unit wide CAMAC module.