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A NEW GENERATION CONTROL SYSTEM AT SLAC*

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Abstract

The proposed SLAC Linear Collider (SLC) project will require an Instrumentation and Control system that provides integrated automatic monitoring and control functions. The present SLAC LINAC Instrumentation and Control system will be totally revamped and it will be expanded to include the support of all of the additional accelerator components that will be required for the whole SLC project. This paper will describe the functional operation of the new system.

1. Introduction

The proposed SLAC Linear Collider[1,2] (SLC) project will provide electron-positron colliding beams at a center-of-mass energy of 100 GeV with a luminosity of 10^{30} $cm^{-2}sec^{-1}$. The SLC general layout in Fig. 1 shows that the existing SLAC LINAC will be combined with several additional accelerator components to produce colliding beams.

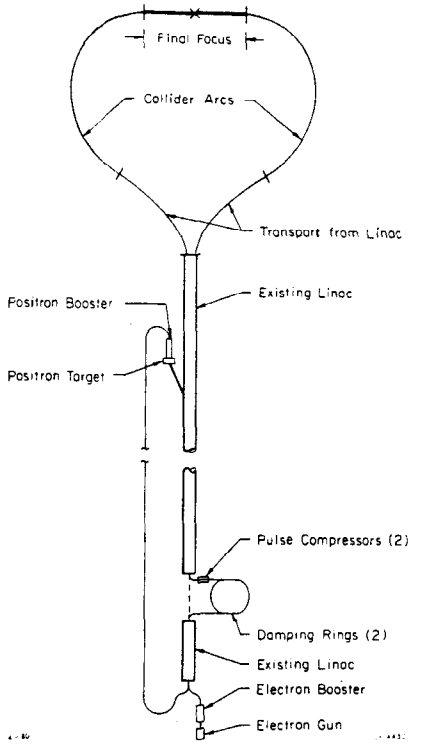

Fig. 1. Layout of the SLAC Linear Collider.

An accelerator cycle will begin with the assumption that the electron and positron damping rings each contain two equally spaced high-intensity low-energy bunches. One of the positron bunches will be extracted from the damping ring, passed through a bunch-length compressor, and injected into the LINAC. Then both electron bunches will be extracted from the electron damping ring, passed through a bunch-length compressor, and injected into the LINAC. The typical spacing of the three bunches in the LINAC will be about 15 meters.

The three bunches will be accelerated along the LINAC. The third bunch, an electron bunch, will be extracted from the LINAC at the two-thirds point and directed at a positron production target. The first two bunches, a positron bunch followed by an electron bunch, will continue to the end of the LINAC where they will have attained an energy of 50 GeV. At the end of the LINAC, the two bunches will be separated by a DC magnet and they will then pass through matching transport sections, colliding arcs, and a final focusing section before colliding at the interaction point.

In the mean-time, the positrons produced by the third "scavenger" electron pulse will be focused and accelerated and then brought back to the beginning of the LINAC. These positrons will then be accelerated through the first LINAC sector and injected into the positron damping ring to replace the positron bunch that was previously ejected. Then two bunches of electrons, created by the electron gun and electron booster, will be accelerated through the first LINAC sector and injected into the electron damping ring to replace the two electron bunches previously ejected.

The following cycles will continue in the same manner with the positron bunch, that is extracted then replaced, alternating between the two positron damping ring bunches.

The purpose of the SLC Instrumentation and Control (I&C) system will be to produce the appropriate monitoring and control functions to successfully direct the complex SLC operation described above in order to deliver two reliable low-emittance beams to the collision point. The system must also provide a quick and efficient means of switching between SLC operation and other LINAC operations, such as delivery of beams to the experimental yard and the filling of the SPEAR and PEP storage rings.

The first chore for the control system will be to provide an efficient and flexible means for setting up the thousands of devices which affect the beam parameters. Then the system must monitor the beam parameters and make appropriate corrections to the initial settings. Finally, the system must monitor the health of all components and automatically correct for inoperative devices, if possible, or at least notify the machine operators of a failure.

The SLC I&C task will be especially demanding because of the tight beam-tolerance requirements and the very large number of unique devices that will affect the beam. Further, the control system must not only work flawlessly, but it must simultaneously allow for the rapid development and testing of new or upgraded algorithms, in order to maximize the SLC performance.

The present LINAC computer control system[3] is based primarily on a "look-and-adjust" manual control system. The SLC requirements preclude this type of control philosophy. Rather, a control philosophy based on machine modeling such as successfully employed in the SPEAR[4] and PEP[5-9] storage rings will be required. Further, the existing system has its roots based on technology that is nearly twenty years old. Therefore, the LINAC I&C will be replaced by a new system that will assume the functions of the present system plus provide a greatly enhanced capability for the precision control and monitoring of devices as well as the implementation of a model driven control system.

The SLAC Main Control Center (MCC) building will be expanded to contain a new control console area, and

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the SLC system will be built up in that area. The controls for the LINAC will migrate to the new console area as the LINAC improvement program progresses.

2. The Computer System

Since the ratio of computer hardware to software costs has decreased by at least a factor of 15 over the past decade, it is prudent to insure that a sufficient hardware processing capability exists in a new control system to virtually eliminate any significant programming effort applied to optimize the speed of or memory use of existing programs. This effort can then be applied to the development of new programs to increase the overall accelerator performance. The SLC computer system supports this philosophy by providing a combination of two large, powerful central processors that will be networked to 70-100 powerful μ-processor clusters, as shown in the block diagram in Fig. 2. Each of these clusters will have the capability of supporting an arbitrary number of 16-bit single-board computers operating in parallel. It is anticipated that the initial total processing power placed into operation for the new LINAC control system alone will be 15-25 times greater than the processing power in the existing system. Further, the system will be easily expandible to include much more processing power if required in the future.

The μ-processor clusters will interface directly to the equipment to be monitored and controlled so they will be distributed near their related accelerator components. Clusters will be located in each of the 30 LINAC sectors and near the damping rings, electron gun, positron source, etc.

2.1. Hardware Architecture

2.1.1. Central Computers. The heart of the SLC computer system will be based on a dual DEC 11/780 VAX system with shared memory and shared disks. The computers will be used to provide on-line execution of large modeling programs and will serve to interface with the machine operators in order to direct the overall efforts of the control system. These computers will also serve as a base for both the VAX and μ-processor software development efforts.

The dual processor architecture will provide extensive processing power when both processors are operational. Either processor will be capable of assuming full operational responsibility for the system in the event of the failure of the other processor. This will be accomplished by simply moving the execution of software programs from the failed processor to the operational processor. No hardware switching will be required.

The VAXs have been chosen because their virtual-memory operating system can simultaneously support many physically large, CPU-bound operating programs and on-line users, as well as provide an environment for fast, efficient program development and maintenance. There may be other processors which can also provide these features, but the VAXs were chosen because of the extensive VAX hardware and software support already existing at SLAC.

2.1.2. μ-Processor Clusters. The SLC system will contain 70-100 distributed μ-processor clusters. The μ-processor clusters will be based on a μ-processor crate using the Intel Multibus[10] architecture. This crate architecture can support an arbitrary number of single-board computers (SBC) and interface modules.

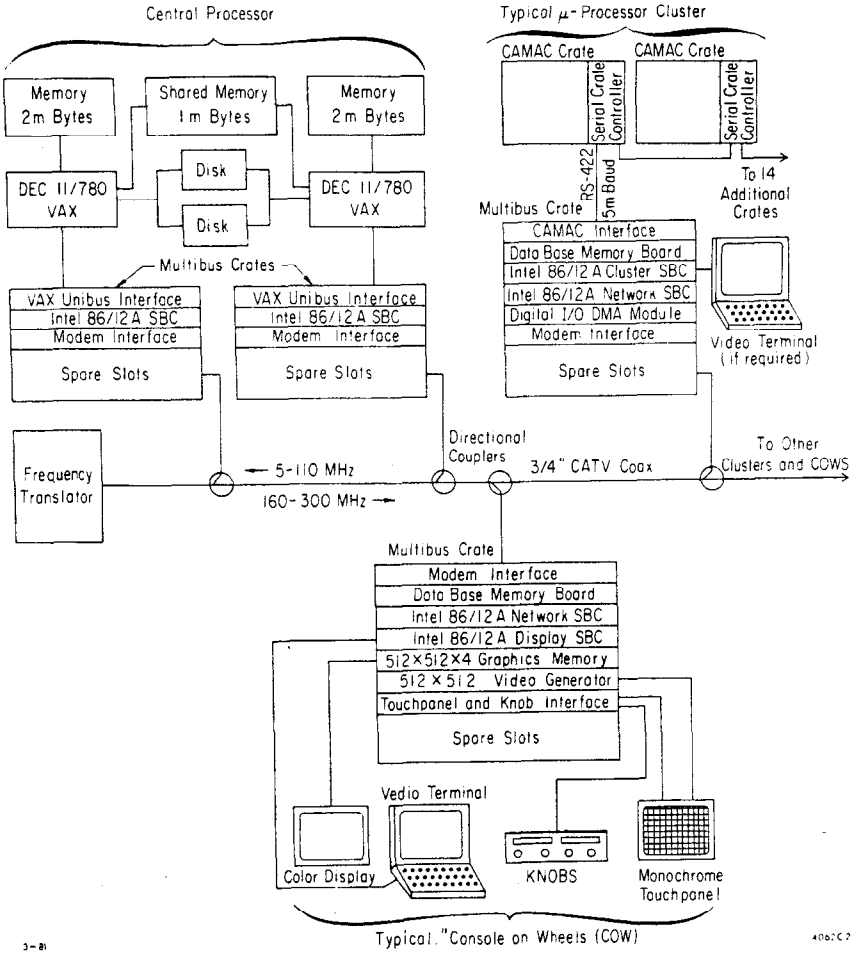

Fig. 2. SLC Computer System Block Diagram.

All of the boards within a crate can asynchronously communicate with one another through the use of shared memory and interrupts. We find that this capability provides a very powerful architecture for our needs because additional SBCs can be added to the crate to assume a portion of the processing load, if required.

The SBC chosen is the Intel 86/12A which will contain an Intel 16-bit 8086 CPU, 8087 floating-point processor, 64K Bytes of RAM, and 32K Bytes of EPROM. The relatively large amount of on-board memory for this SBC allows the processors to execute most of their programs through their own on-board memory which means that the Multibus backplane will not become a communications bottleneck. Various benchmarks show that this SBC has somewhere between 1/10 and 1/7 of the VAX processing power.

The actual interface to the SLC technical components will be made through the use of CAMAC. The CAMAC crates will be located very near to their related equipment. It is anticipated that the entire SLC system will contain 175-250 crates. The CAMAC crates will be interfaced to the Multibus crate through high-speed (10 μsec/cycle) low-cost serial crate controllers that are presently under development.

The Multibus CAMAC interface will be a high-speed Direct Memory Address (DMA) device that directly executes lists of CAMAC commands from the Multibus address space.

The choice of specific equipment for the μ-processor cluster was agonizing because of the development of the FASTBUS[11,12] architecture. The powerful and flexible FASTBUS architecture easily meets all of the cluster requirements and could potentially be used to replace both the Multibus and CAMAC crates. Unfortunately, the overall SLC schedule (see Sect. 4 below) will not allow adequate time to develop and support a FASTBUS implementation of the μ-processor clusters. In contrast, both Multibus and CAMAC are mature systems that are well supported by industry and within SLAC.

2.1.3. Communications Network. The μ-processor clusters and the VAXs will be connected through the use of a Carrier-Sense Multiple-Access Collision-Detect (CSMA/CD) local network similar to that specified by Eithernet.[13] The CMSA/CD networking architecture interconnects all of the nodes through a single cable and allows any node on the cable to asynchronously communicate with any other node. We expect that this very powerful networking architecture will be especially valuable when using dedicated μ-processors to implement time-sensitive control loops over long distances.

The SLC network will differ from the Eithernet specification in that modems and Cable Television (CATV) technology will be used to transmit several frequency-modulated signals over a broadband cable. In contrast, Eithernet uses single channel "baseband" modulation technique. Broadband CATV technology has been chosen for SLC use because it is relatively inexpensive and it readily supports high-speed communication over long distances. Further, the wide bandwidth of the cable (5-300 MHz) allows it to simultaneously support the transmission of several high-speed (2 Megabaud) digital, low-speed (9600 baud) digital, video, and voice channels.

2.1.4. Operator Consoles. The operator consoles for the system will be interfaced directly to the broadband CATV network. This will allow full flexibility in the geographical placement of the consoles, which will greatly enhance the support of development activities since a console can be located near the equipment that is under development.

An operator console will contain the following equipment: a full color 512 element × 512 line graphics display; a touch-panel similar to the ones used for PEP control;[14] general purpose slew knobs; and a CRT terminal.

2.2. Computer System Software Architecture

Essentially all of the SLC software development for the μ-processor clusters as well as the VAX will be performed through the use of the VAX. Wherever possible, FORTRAN 77 will be used for applications programming. FORTRAN 77 was chosen as the standard language because of its extensive support on the VAX, and because it is the most universally understood language. Although alternative languages could be used for the μ-processors, the consistency provided by standardizing on FORTRAN 77 has been deemed to be a great advantage for both the development and support of applications programs.

The μ-processor development software on the VAX will consist of a FORTRAN 77 cross-compiler, a linker, and a network downloader. A symbolic debugger will also be provided so that the execution of an μ-processor task can be directly monitored and controlled from any VAX terminal.

Applications tasks to be executed in the VAX will be written as structured subroutines which are attached to a VAX process that provides interface routines to the operator console, and to a structured database. This process will also provide a scheduling service for the subroutines.

An interpreter for the execution of touch-panel source code has been developed using the FORTH programming language as a base. This interpreter provides a convenient method for generating touch-panels that are capable of serving several application tasks. It also allows for the reorganization of the touch-panel buttons, without recompiling the relevant VAX code.

A "paranoia" process will also be provided for the system. This process will continuously monitor the operation of the accelerator and report any faults that are discovered. The definition of possible faults will be described in a computer file that can easily be modified by machine operators. Thus, troublesome situations can be defined as they are encountered so that a warning can be generated for all future occurrences of similar problems.

The μ-processor clusters will provide local control algorithms for the operation of the technical equipment. In general, the μ-processors will receive an operational configuration in engineering units for its equipment from the VAX. The μ-processors will then insure that the equipment is set to that configuration and will only report back to the VAX when it is unable to achieve or maintain the desired configuration. The μ-processor clusters will also provide monitoring information in engineering units to the VAX upon request. Dedicated μ-processor systems will also be used to implement time-sensitive digital control loops wherever required.

3. Instrumentation

This section will describe the functional operation of some of the major SLC instrumentation sub-systems. The examples cited here are primarily relevant to the operation of the LINAC since most of the engineering effort to date has been applied in this area. However, it is anticipated that many of the principles described here will be directly applied to support the needs of the other accelerator components.

3.1. Beam Monitoring

The primary beam monitoring system for the SLC will be position monitors. The LINAC will contain approximately 270 sets of stripline monitors located within the LINAC quadrupoles (see Fig. 3). Signals from these striplines will be sampled and digitized to provide a position measurement of any one of the three SLC bunches in a beam pulse. The monitors will be accurate to better than .1 mm. The collection of this position information, as well as information gathered from

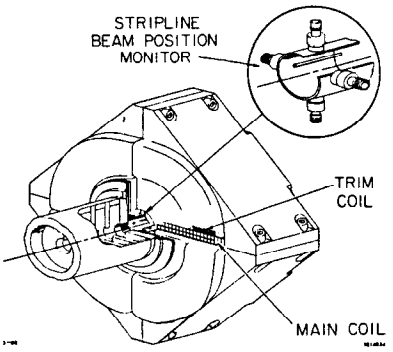

Fig. 3. Linac quadrupole and beam position monitor assembly.

approximately 600 additional monitors located in the transport lines, collider arcs, and final focus beam lines, will be synchronized so that a complete trajectory of individual beam pulse can be measured from the damping ring to the collision point.

Digitizing beam profile monitors will be provided at key points along the beam's trajectory to provide accurate quantitative measurements for the X-Y intensity distribution of the beam. These monitors will use a 32×32 charge-coupled device (CCD) array to record the scintillation produced by a single beam pulse striking a screen. The information in the CCD array will be read into the computer system to provide information for accurate emittance measurements of the beam.

Other forms of beam instrumentation will include energy defining foils and beam current toroids. The information from both of these devices will be digitized to record the parameters for any one of the three bunches in a beam pulse.

3.2. RF System

The state of the LINAC klystron-modulator system will be monitored on a pulse-to-pulse basis by the μ-processors to determine if a fault occurred in any one of the 240 stations on the last beam pulse. In the event of a fault, the relevant μ-processor must quickly notify all other μ-processors in the network so that they will not flood the VAXs with useless fault information. The μ-processor must then monitor the health of the questionable klystron over the next few cycles to determine whether or not to take the klystron off-line and to ask the VAX for a replacement station. The μ-processor system will also be responsible for the proper phasing and timing control of the RF system.

4. Power Supply Monitoring and Control

The computer system will be responsible for the control and monitoring of over 2000 power supplies in the SLC system.

The setpoint values for bending and focusing magnets will be determined by computer models.[15] The steering coil settings will be determined by orbit correction programs based on beam position monitor readings from the various accelerator components.

The LINAC modeling and orbit correction programs will be especially complex because they must consider the effect of the 240 klystrons on the lattice. This not only means that the computer system must have correct information on the energy contribution of each of the klystrons, but it must also change the magnetic lattice whenever the distribution of operating klystrons changes because of a klystron fault. Whenever a faulting klystron is replaced by a standby klystron, the computer system must correct the focusing elements between the two klystrons because of the beam's energy change in that region. Also, a local correction to the beam steering must be made in a small region downstream of each of the switched klystrons to compensate for any steering effect of the klystrons.

The klystron replacement function will be a time-critical process because it is possible that the klystron fault rate may approach one per minute. In order to maintain a high integrated luminosity under this condition, the lattice reconfiguration and orbit correction algorithms must be completed in less than 3 seconds. Although the details of this process have not yet been completely specified, it is believed that this timing requirement can easily be accomplished through the use of a combination of the VAX computers and μ-processor system.

Certain crucial points in the beam's trajectory, such as the injection point of the LINAC and the collision point, will require a very stable beam position. Local digital control loops will be implemented to stabilize the beam position by feeding back position monitor information to steering coils in order to compensate for low-frequency machine variations and variations caused by ground motion.

5. Schedule

The SLC I&C system will be constructed in several phases in synchronization with the construction of the overall SLC system.

The first phase calls for the development of prototype beam instrumentation for the testing of the first LINAC sector. In fact, prototypes of the beam position monitors, beam profile monitors, energy foils, and toroids described in Sect. 3.1 above are now operational. Also, a special test set-up has been implemented[16] to monitor the operation of the new SLED II klystron stations which are under development.

The second phase of the project specifies that the new I&C system for the first third (10 sectors) of the LINAC, the first damping ring, and the injector, must be operational by October, 1982. As part of this effort, hardware and software prototypes of the VAX equipment, μ-processor clusters, and computer networking will be operational by September, 1981.

The I&C system for the remainder of the LINAC and other accelerator components will be operational by October, 1985.

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