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A LOW NOISE PWC CATHODE READOUT SYSTEM*

E. Cisneros, D. Hutchinson, D. McShurley, R. Richter†, S. Shapiro
Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

Abstract

A system has been developed, primarily to detect the induced charge deposited on PWC cathodes, which is versatile, fast and has a good signal to noise ratio for signals of $\geq 10^{-14}$ Coulomb input. The amplifier system, which is completely separated from the detector by 95Ω coaxial cables, is followed by a new charge integrating, version of the SHAM/BADC system developed at SLAC. This SHAM IV system is CAMAC based, allowing for computer calibration of the entire system from amplifier through ADC.

Introduction

A system has been developed whose primary function is to detect and measure the induced charge deposited on PWC cathodes. The system has good bandwidth, low inherent noise and is capable of operating remotely from the proportional chambers at distances of over 10 meters with no significant degradation in performance. The system is partially CAMAC based and allows for computer calibration of each channel from amplifier through ADC. Approximately 3000 channels of this system are now in operation at the LASS Spectrometer at SLAC.

The system is comprised of five primary elements: (a) the input cable; (b) the low noise amplifier, (c) the output cable and its termination, (d) the SHAM IV integrator; and (e) the BADC. The input cable[1] and the BADC[2] have been used in other applications and have been described elsewhere. This paper will emphasize the characteristics and performance of the amplifier and integrator circuits, and the ultimate performance of the system as a whole.

The Input Cable

The input cable (Brand Rex T5563) is a 95Ω miniature air core ribbon coax whose small size and good frequency response make it ideal for use in our application. A separate ground sheath of aluminum mylar laminate is placed around each cable bundle to provide additional RF shielding. The properties of this cable are summarized in Table I.

TABLE I
Properties of Brand Rex T5563

Impedance	95Ω
Capacitance	13.5 pf/ft
Velocity of Propagation	0.80 c
Attenuation at 400 MHz	14 db/100 ft
Dielectric Material	Air
Number of Coaxial Cables/Ribbon	8
O.D. of One Cable Strand	0.112"
Drain and Signal Wire Size	29 AWG

The Amplifier

The proportional chamber amplifier has been designed to give low noise amplification with moderately fast response (less than 10 nsec rise and fall times). Additionally it has been designed to operate separable from the proportional chamber by cable lengths of up to 10 meters or more. These three requirements tend to be contradictory, viz. good bandwidth, tolerance of input cable capacitance and low noise. To solve these problems, our input stage employs a FET (for low noise)[3] in common gate configuration with the dynamic source resistance set equal to the cable characteristic resistance to terminate the cable with minimum reflection. As the input cable is now a terminated transmission line, the typical 50 nsec Iong chamber pulse into 95Ω reaches the amplifier input with minimal broadening due to the effect of this cable. The amplifier, therefore, retains all the time information inherent to proportional devices. Figure 1 is a simplified schematic of the amplifier circuit.

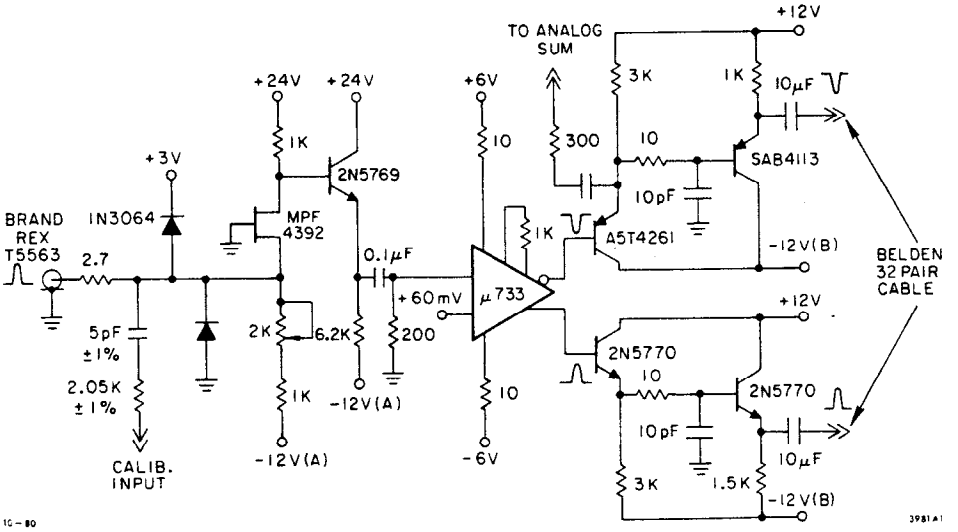

Fig. 1. A simplified schematic of the low noise amplifier.

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† Present address: CERN, Geneva, Switzerland.

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The FET drain resistance, 1 kΩ in ratio to the cable resistance (95Ω) gives the voltage gain of the first stage, approximately 10. The FET is followed by an emitter follower and a video amplifier (μA733) set to a voltage gain of ~50 (differential) for a total gain of 500 (differential). The emitter follower is used to allow the input resistance of the video amplifier to be small (viz. 200Ω) to reduce its output noise and to preserve a good rise time at the FET drain due to the small input capacitance of the emitter follower. The video amplifier input is biased to shift the ±2 volt output range to $-0.5 \rightarrow 3.5$V and $+0.5 \rightarrow -3.5$V on its two complimentary outputs, allowing a $0 \rightarrow 7$ volt (differential) output voltage range. Cascaded emitter follower drivers are employed on each output to drive the twisted pair line. The output is AC coupled with large (10 μfd) capacitors to avoid base line shifts due to multiple hits within one SLAC beam pulse (1.6 μsec).

This amplifier can be used to service either polarity input signals by the manipulation of 3 jumpers/channel provided on the PC board. The amplifiers are packaged 16 per PC board and 16 PC boards per crate. Each amplifier card has circuitry for generating the analog sum of eight adjacent channels (2 circuits per card) and circuitry to provide a digital output (TTL) if the analog sum pulse height is greater than an adjustable value. Table II summarizes the amplifier specifications.

On each card, the capability is provided to strobe a voltage step function onto a precision 5 pf capacitor at the input to each amplifier for computer calibration of the entire system. Alternate channels can be calibrated separately. Figure 2 is a combination block diagram and schematic representation of the calibrate circuitry.

TABLE II
Amplifier Specifications

Gain	:	100-4000 set by a single resistor
Bandwidth	:	$t_r \leq 10$ nsec t differentiation ≥ 20 μsec
Linearity	:	Gain variation ≤ 1% from 10 mV → 4 volt differential into 51Ω
Noise	:	Vn (rms) = 1.5 mV output ⇒ Equivalent input noise of 1.5×10^{-15} C for gain = 500 and R_{in} = 100Ω
S/N	:	at 10^{-14} C input = 3
Temperature Stability	:	Gain and S/N vary ≤ 1% for 5°C temperature change.
Crosstalk	:	Crosstalk induced charge output is 52 db (400x) less than the inducing (test) charge pulse on adjacent channels
Ringing	:	Output response to a step input voltage has no more than a 10% overshoot
R_{in}	:	95Ω ± 10% as used: R_{in} is variable/channel by changing a single bias potentiometer to vary the FET quiescent current
R_{out}	:	< 10Ω
Power/card	:	+24V 200 ma +12V 381 ma + 6V 394 ma - 6V 381 ma -12V 581 ma
Calibration	:	Provision is made to apply a voltage step function (-5V→+5V) to a precision 5 pf capacitor at the input to the circuit. Alternate channels can be calibrated separately

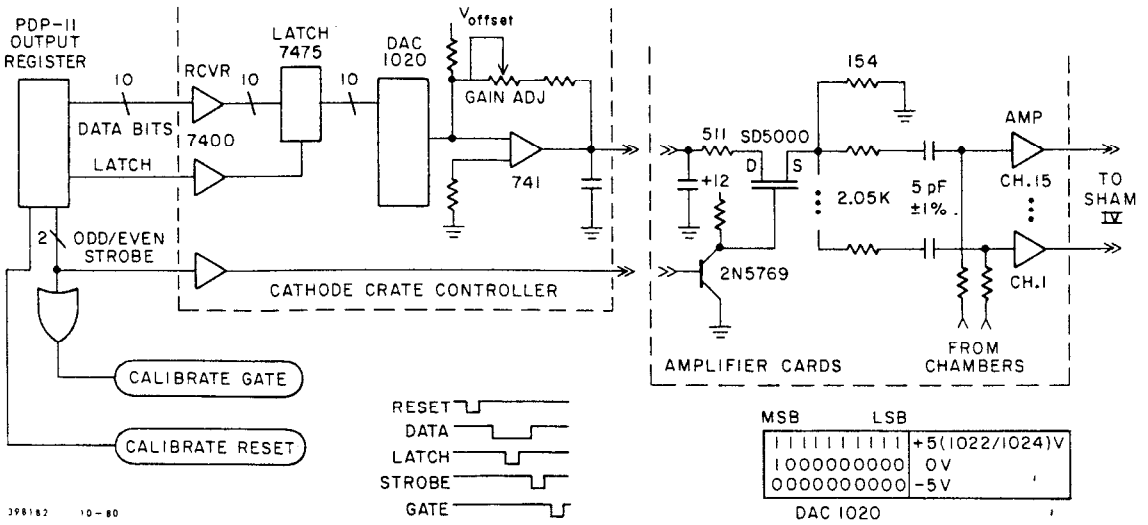

Fig. 2. A block diagram/schematic representation of the calibrate circuitry.

The PC card itself is a 4 layer card, approximately 12" x 14" in size. Ground and power planes on the interior layers provide good card to card shielding and power returns. Figure 3 is a photograph of the amplifier card.

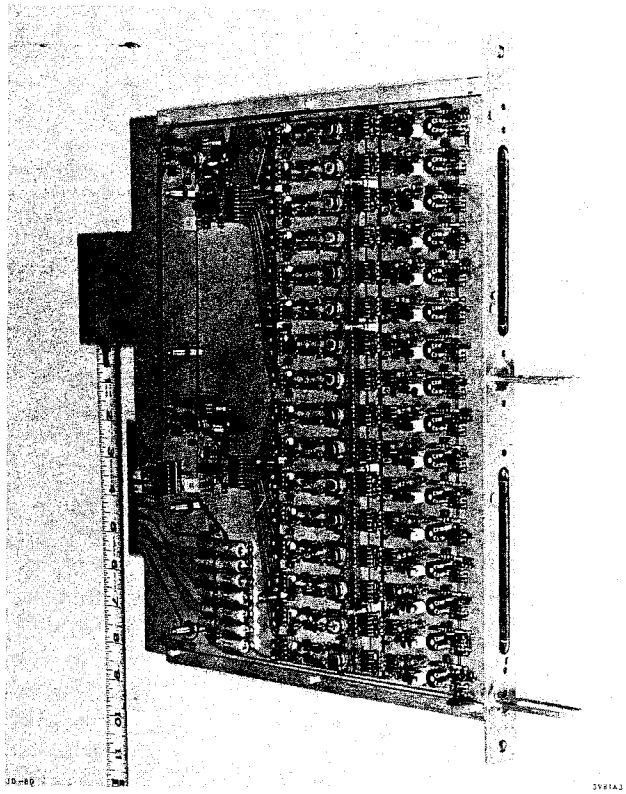

Fig. 3. A photograph of the amplifier card.

The Output Cable

The output cable is designed by Belden to our specifications. Each cable consists of 32 twisted pair of #24 AWG wire. Each pair is separately shielded with a polyester/foil type shield containing a drain wire. The entire ensemble is similarly shielded with a group shield and drain. One cable services 2 amplifier cards and one SHAM IV unit. The cable has a characteristic impedance of 51Ω and a velocity of propagation of 0.559 c. The cable provides the dual function of transmitting the signal to the SHAM IV and providing the electrical delay necessary to time these signals into coincidence with the event gate. A cable length of 70.5 meters is necessary to establish the coincidence. Passing a signal through a long cable has the unfortunate side effect of dispersing it. To counter this, a termination circuit shown in Fig. 4(a) is used on each channel. Figures 4(b)-4(d) show the effect on pulse height and width of this circuit. It can be seen that this circuit restores the width of our pulse but at the expense of pulse height. Not shown, however, is a signal to noise degradation of the system by about 50% due to the necessity of using this circuit.

The SHAM IV

The SHAM/BADC system has been in use at SLAC for many years.[4] The system as designed, receives 32 channels of analog information, stores it and presents it to an analog multiplexer. Each module is a single width CAMAC module. Twenty modules can be accommodated within one crate. The modules within each crate are

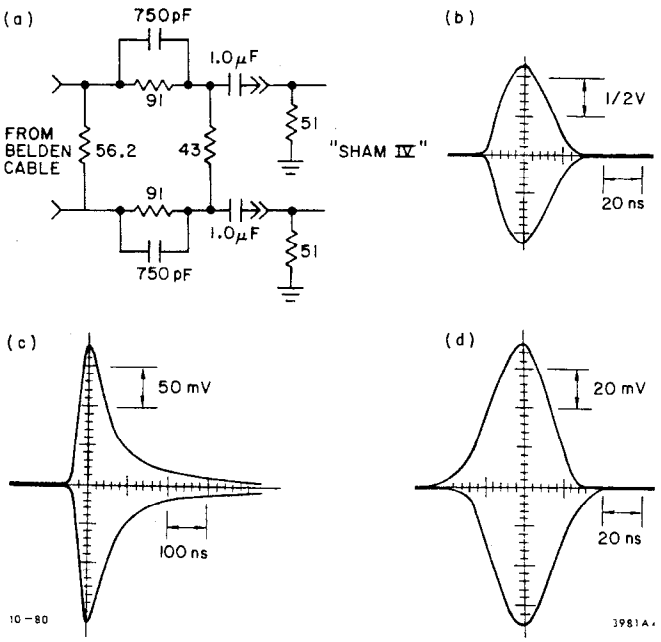

Fig. 4. (a) A single channel schematic of the termination network.
(b) The signal pulse at the amplifier driving 51Ω.
(c) The signal pulse after 70.5 meters of cable into 51Ω.
(d) The signal pulse after the cable and properly terminated.

scanned by an autonomous controller containing a single ADC, memory and arithmetic capability for offset, gain, and linearity corrections. The SHAM IV module designed for use in LASS is a fast charge integrator. Pulses in the range of 0-300 mV (differential) and approximately 50 nsec wide at the base line are received, amplified, and a charge proportional to the integrated area under the pulse stored on a FET-isolated, 100 pf storage capacitor, provided only that the pulse fall within the "event" gate, which can be as narrow as 100 nsec. The reset pulse, which precedes the event gate, shorts the storage capacitor to ground just prior to the integration process. This pulse can also be used to abort an event and rearm the SHAM to accept a second pulse within the SLAC beam spill.

Figure 5 presents a block diagram/schematic of the SHAM IV circuit. The SHAM IV is fabricated on a 4 layer PC card. The inner ground plane is extended to the edge of the input connector at the front panel for maximum crosstalk reduction. The input impedance of the circuit is set by resistors R1 and R7 and are user defined in the range $0 \leq R \leq 1K$. Transistors Q1A and Q1B are connected as a differential voltage amplifier with a differential gain of approximately 10. (Determined approximately by the ratio of R5 to the sum of R2+R3). This pulse then drives a bootstrapped current source Q2 and Q3A,B. The pulse current is determined by this amplified input pulse amplitude at the base of Q2 and by the emitter resistor R11. The bootstrap circuit Q3A,B provides positive feedback to the collector of Q2 thereby raising the effective impedance of R12 to $\geq$ 100 kΩ. AC coupling capacitors C2 and C3 are chosen to limit bandwidth and thereby reduce noise. Q4 is a shunt switch which grounds the pulsed current source whenever the integrator gate is in the non conducting (high Z) state. This reduces feedthrough to the storage capacitor of spurious input pulses which might occur just ahead of the integration gate time. Q5B is

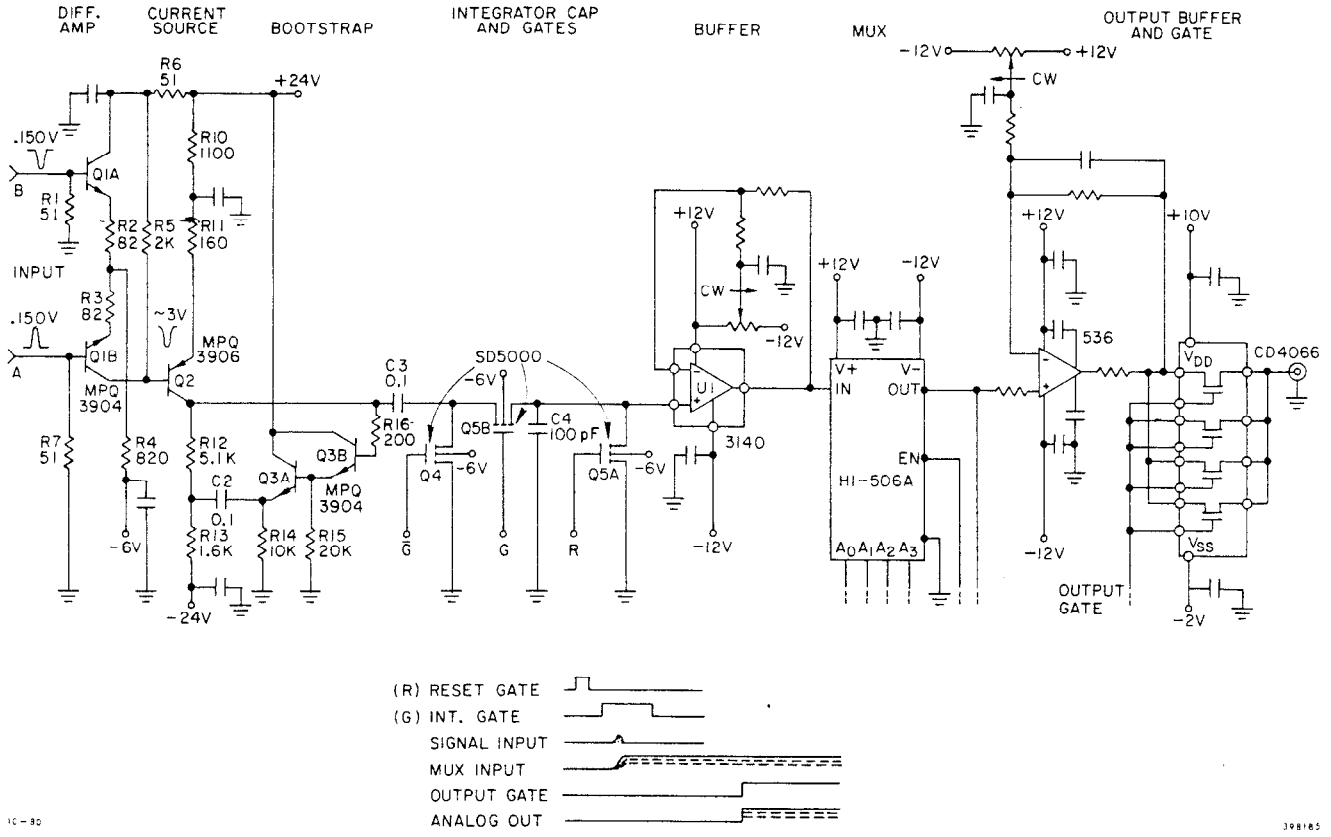

Fig. 5. A block diagram/schematic of the SHAM IV circuit.

the integrator gate. Q5A performs the reset function by discharging the storage capacitor C4 to ground just prior to opening the integrator gate. U1 is a FET input op amp with an input impedance of 1.5 TΩ and a voltage gain from the + input of +1. From this point onward the analog multiplexing, buffering and CAMAC control logic is identical to other modules in the SHAM family.

The SHAM IV input range is 0-150 pC resulting in an analog output range of 0-4 volt. Use of a 12 bit ADC yields a sensitivity of 0.0375 pC/channel. The SHAM IV specifications are summarized in Table III. A photograph of a SHAM IV is presented in Fig. 6.

TABLE III
Summary of SHAM IV Characteristics

Number of Channels	:	32
Analog Input	:	0-150 pC Diff. (Z_{in} = 50Ω)
Analog Z_{in}	:	Selectable (typical 50Ω)
Gain	:	37.5 pC/V Diff.
Output Noise	:	~1 mv RMS
Integral Linearity	:	~2% 0-4 V
Integrator Droop	:	8% / μsec; gate open
Gate Feedthrough	:	< 60 db
Integrator Slew Rate	:	50 V/μs
Analog Output	:	0 to +4 V
Analog Z_{out}	:	< 150Ω
Delay, Input to Integrator Capacitor	:	5 ns
Delay, Gate Input to Gate On	:	20 ns
Channel Offset Range	:	100 mV
Output Offset Range	:	250 mV
Int. Gate	:	1 T^2L Load - Logical 0 Enable
Reset Gate	:	1 T^2L Load - Logical 0 Enable
Reset Time	:	50 ns Min
CAMAC Requirement	:	Read CH 0-15 N·A·F(0)·S1
		Read CH 16-31 N·A·F(1)·S1
CAMAC Response	:	X output
Power Supply Requirements	:	+ 6V 125 ma
		- 6V 310 ma
		+24V 575 ma
		-24V 350 ma
Analog Input Connector	:	Edge card fingers to mate with Viking 3VH36/1JN5
Gate, Reset, and Analog Out Connector	:	LEMO

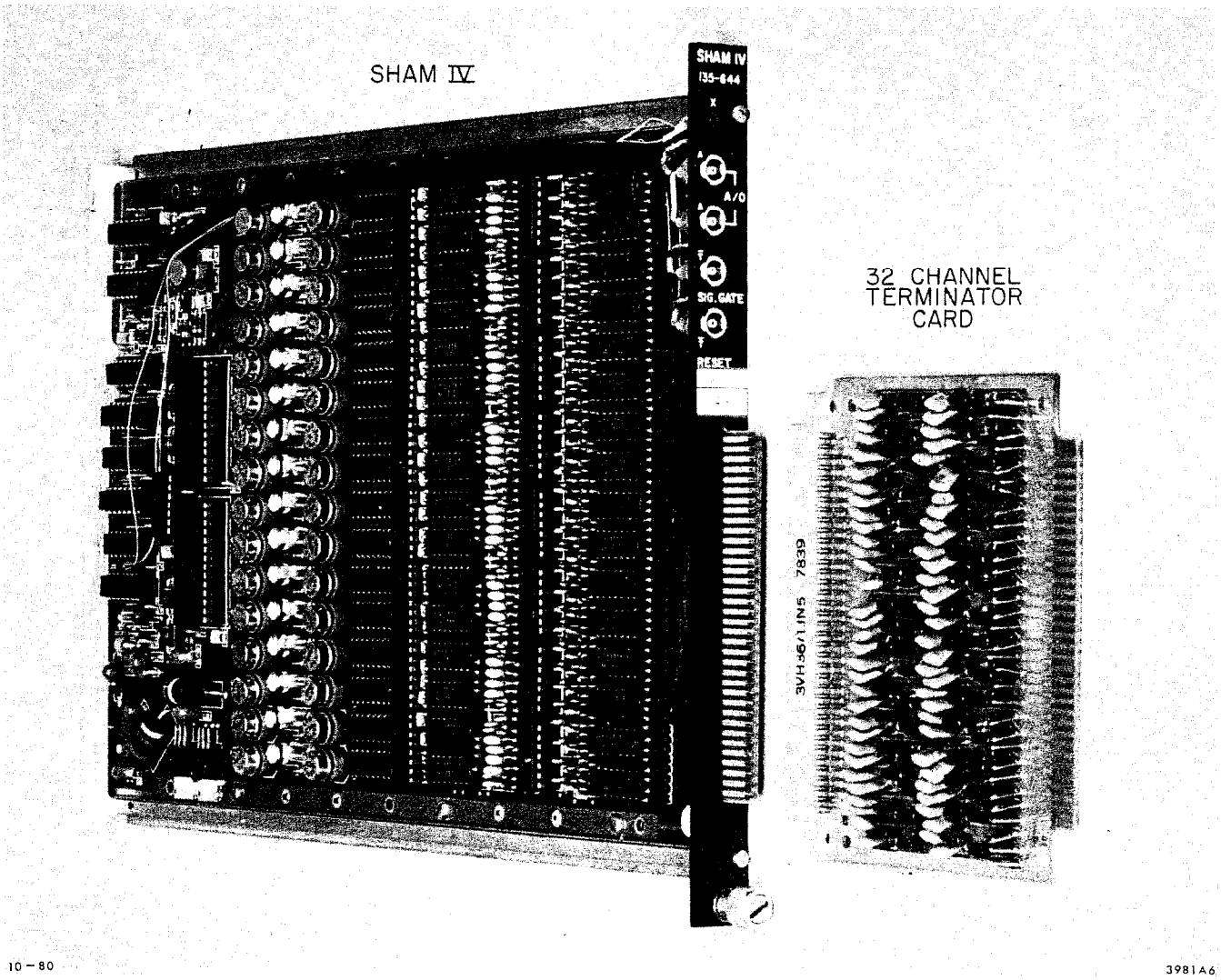

Fig. 6. A photograph of the SHAM IV PC board and termination card.

The BADC

The BADC controls the analog multiplexing of a CAMAC crate of up to 20 SHAM IV modules i.e., 640 channels, digitizes the analog data and executes the microprogrammed algorithms for the data handling and corrections. The BADC employs a 12 bit ADC which requires a conversion time of approximately 2 μsec. At LASS, a system employing 6 BADCs is in operation. Data transmission time is reduced to a minimum since the BADC's only transmit "good" data, i.e., data higher than a programmable threshold value. Each data word transmitted is accompanied by its functional label -- in our case, PWC cylinder number, cathode number and strip number, making further address decoding unnecessary. The BADC must be used in conjunction with the SLAC Type U CAMAC Crate Controller.[5]

The use of the SHAM/BADC concept resulted in a savings of both dollars and labor. The cost of the ADC, CAMAC crate, and type U controller are amortized over 640 channels. The microprogram developed to guide the BADC was more than adequate for our needs and was used unchanged.

Summary and Conclusion

A system has been developed which is capable of detecting the charge induced on PWC cathodes. The signal to noise ratio for deposited charges as low as 10^{-14} Coulombs is about 2:1. The time information characteristic of proportional devices is retained. No electronics need be attached to the proportional devices since their location precludes easy removal for electronic repair. Time and money were saved by developing a system compatible with the SHAM/BADC system already in existence at SLAC. A detailed description of the performance of our new proportional detectors which use this electronic system and which include a discussion of spatial resolution as well as the use of pulse height information to reduce multiple hit ambiguities is presented in a companion paper submitted to the 1980 Nuclear Science Symposium.[6]

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