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MSHAM - A MULTI-HIT SAMPLE AND HOLD MULTIPLEXER*

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Abstract

The MSHAM is a single-width CAMAC module intended to be used for dE/dx or Z-position measurements, with a density of 16 analog channels. It is designed to record up to four hits/event per channel but the design can be easily adapted to eight hits. The charge collection time interval allowed per hit is externally controlled in the range of 50-500 ns, according to the requirements of the experiment. Besides the electrical performance of the MSHAM, i.e., linearity, noise, cross-talk, etc., the goal was to design multi-function circuits and high density packaging in order to achieve low cost per channel.

Introduction

The wire chambers involved in high-energy physics experiments, particularly those with multi-hit capability, produce a tremendous number of signals which must be processed. It is the purpose of the multi-hit sample and hold analog multiplexer to accept the analog data from the chamber preamplifiers and provide multiplexed analog signals to the data acquisition processor. In this way, the MSHAM modules allow the use of a single processor for 640 chamber wires and up to 4 hits per wire, or 2,560 hits.[1]

The MSHAM is a 16-channel CAMAC module designed to record the total charge carried by each wire in four equal time intervals, or storage cells, whose length is dictated by the conditions of the experiment. For example, the MARK III detector which was designed to operate at Stanford Linear Accelerator Center's SPEAR machine, must respond to the $e^+ - e^-$ interactions occurring at a rate of 1.28 MHz (780 ns). As the primary trigger decision is made in 640 ns, the MSHAM is controlled to accept the signals during four time intervals of 160 ns each, the charge being stored in four cells. This read-in process takes place each 780 ns, until an event is accepted. If an event is accepted by the trigger logic, the recorded signals are multiplexed onto the analog bus to the BADC, a semi-autonomous controller for data acquisition.[2] The BADC digitizes the analog data and executes microprogrammed algorithms for data handling and corrections, before the result is transferred to the host computer.

If the trigger logic rejects the event, the stored charge during the four time intervals must be cleared before the next collision occurence. In the MARK III detector the MSHAM is cleared by a 90 ns RESET pulse which discharges the storage cells to .02%.

The MSHAM is conceptually different from the solution adopted elsewhere.[3]

Circuit Description

The MSHAM structure, as a module and as a system, is shown in Fig. 1. The analog output of each module is OR-ed to a common bus connected to the BADC input, through the analog multiplexer MUX-2. This multiplexer is controlled by the N-lines. The high number of modules connected to the analog bus constitute a capacitive load which must be discharged after each read-out. This is accomplished by Q_{10} and Q_{11} FET-switches operated by the S1 strobe pulse.

For a fast clear of the storage cells, Q_1 through Q_4 FET-switches are turned "ON" simultaneously; this configuration leads to a very low rail discharge time constant

$$\tau_d = 10.5 \text{ ns} \quad (R_{ON} = 12\Omega \ , \ C = 875 \text{ pF}) \ .$$

The analog circuits of each channel consist of an input stage which is a transconductance amplifier (G_m), shown in Fig. 2, and a gated integrator. The differential amplifier provided with a current source accounts for a CMRR better than 60 dB. The output impedance of this stage is increased by a bootstrapping stage; this improves the integral linearity and the droop of the recorded signal to less than 1% each.

The amplifier drives a rail to which four sample and hold circuits are connected. The configuration Q_1 and Q_2 makes the feedthrough to this rail negligible. The parallel switch Q_1 keeps the integrator clamped before an event is expected and during the read-out of a stored event; the series switch Q_2 isolates the rail from the oncoming signals during the read-out cycle.

The simplified scheme of the logic circuits is shown in Fig. 3; this scheme is self explanatory.

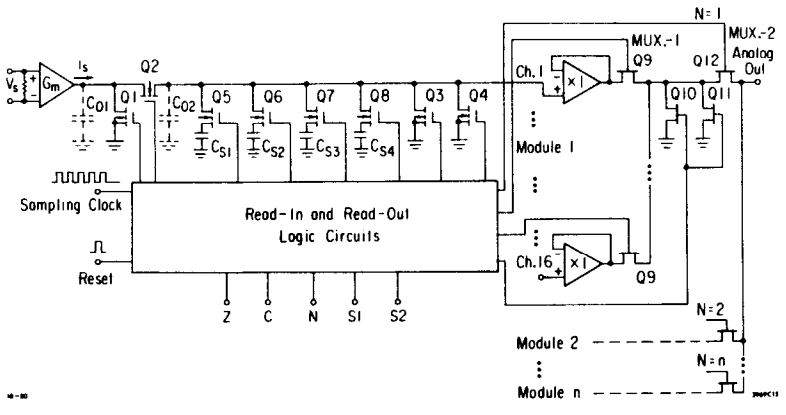

Fig. 1. MSHAM scheme.

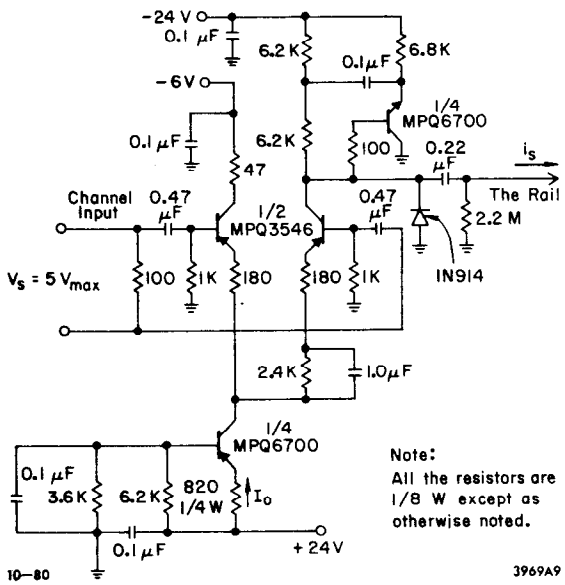

Fig. 2. The input stage circuit diagram.

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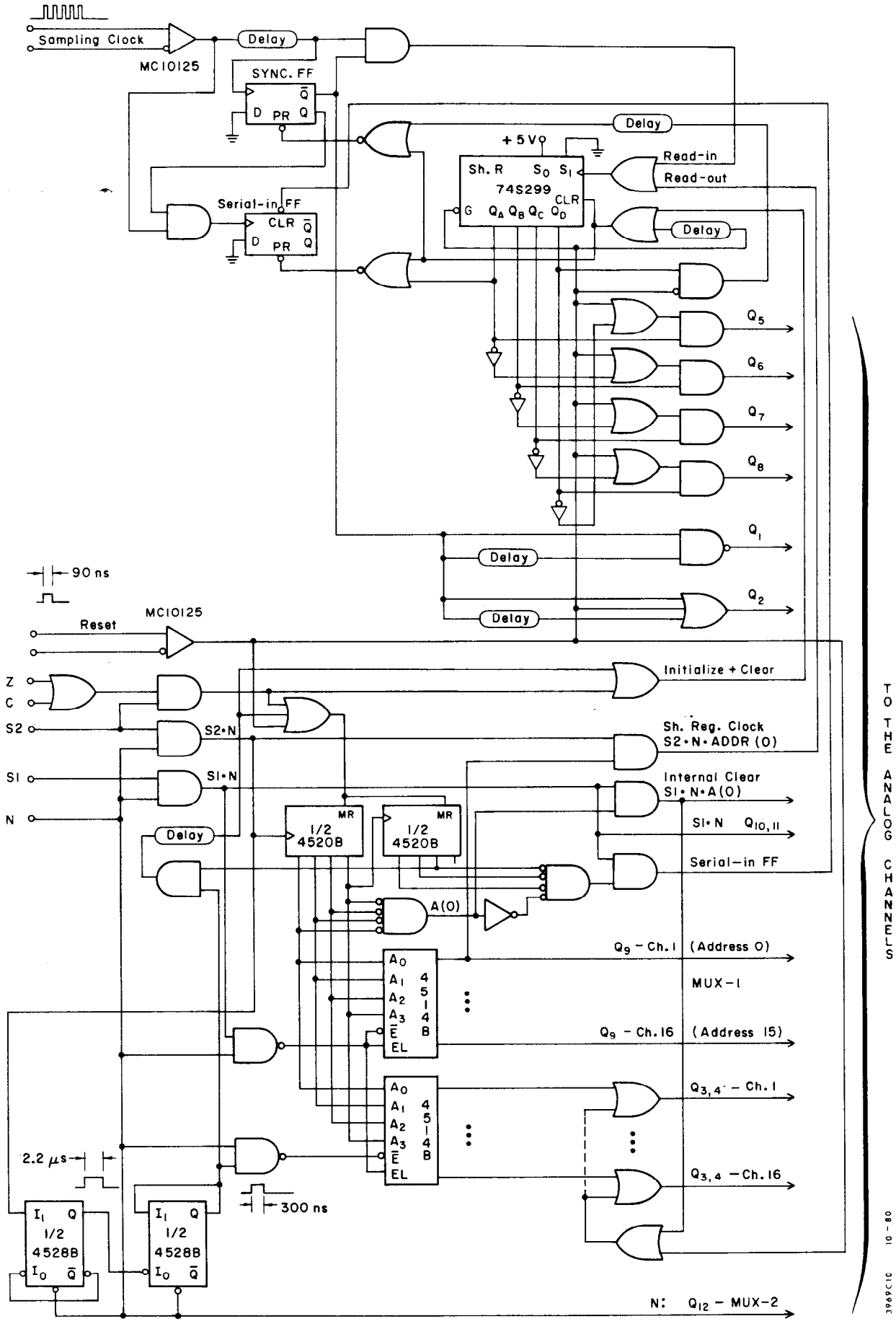

Fig. 3. The simplified logic diagram. Level shifters, buffers and drivers are not shown.

I would mention only that:

(a) An eight-bit shift register is used. Although only four bits are necessary for the MSHAM, the component was chosen with the assumption that the design might be extended to 8-hits. The shift register is clocked by the Sampling Clock in the read-in cycle and by the S2 strobe in the read-out cycle. It controls the four storage cell switches, Q_5 through Q_8.

(b) An eight-bit counter, clocked by the S2 strobe, controls the read-out of 64 analog signals (16 channels × 4 hits). This counter is internally reset after 64 counts and is also reset by the externally supplied RESET or $(Z+C)\cdot S2$ pulses.

(c) Two 1-of-16 decoder/demultiplexer with input latch are used. The first one addresses the channel multiplexer MUX-1 and the second one, enabled after each read-out of a storage capacitor, is used to address the discharge FET-switches, $Q_{3,4}$.

Module Operation

The MSHAM is operated in two steps: the READ-IN cycle and the READ-OUT cycle.

1. Read-in Cycle

Under the control of five externally supplied sampling clocks, the shift register controls the four storage cells, Q_5 through Q_8, successively. In this way the charge supplied by the input amplifier is stored in each of the four cells. The read-in timing diagram is shown in Fig. 4. The rail has an inherent stray capacitance C_0 split in two values, C_{01} and C_{02}, by the series switch Q_2. The buffer amplifier prevents the inherent capacitance of the MUX-1 and MUX-2 to increase C_{02}.

Although most of the charge signal is stored in the storage capacitors, the remainder is stored in the stray capacitance of the rail; part of this charge will be transferred to the following cell. Therefore the voltage signal developed across a storage capacitor is given by:

$$V_n = \frac{1}{C}\left[\int_{t_{n-1}}^{t_n} i_s\,dt + q_{n-1}\right] \qquad (1)$$

where

V_n = the voltage across the n^{th} cell capacitor

$C = C_{01} + C_{02} + C_s$

i_s = the current signal

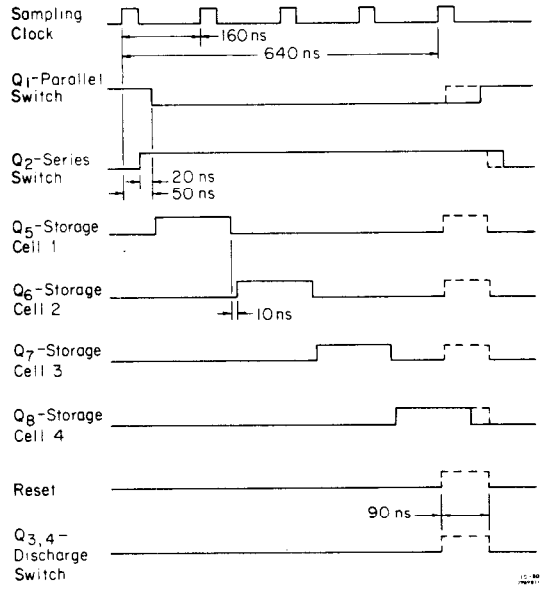

Fig. 4. The READ-IN timing diagram.

q_{n-1} = the charge stored into the rail stray capacitance during the previous time interval.

If the primary trigger decision is to abort the event, a reset pulse, externally supplied to the module, will discharge the storage capacitors and will also reset the whole logic circuitry to the initial state.

2. Read-out Cycle

Read-out is accomplished by a version of the BADC processor with a 12K memory. This unit assumes control of the CAMAC DATAWAY in order to address each of the storage cells. The read-out sequence of the array of 16 channels by 4 hits is: the 1st hit position is addressed (shift register bit 1), then the sub-addresses (which correspond to the channel number) are stepped from 1 through 16. Four such cycles are required to complete the read-out. The read-out timing diagram is shown in Fig. 5. Read-out is straight forward; as each cell is addressed the analog switch for that cell (Q_5 through Q_8) closes transferring the charge to the common rail. After the voltage on the analog busline is sampled by the BADC, a clear pulse, internally generated, discharges the capacitor to zero voltage. After the 64th read-out an internally generated pulse resets the logic circuits.

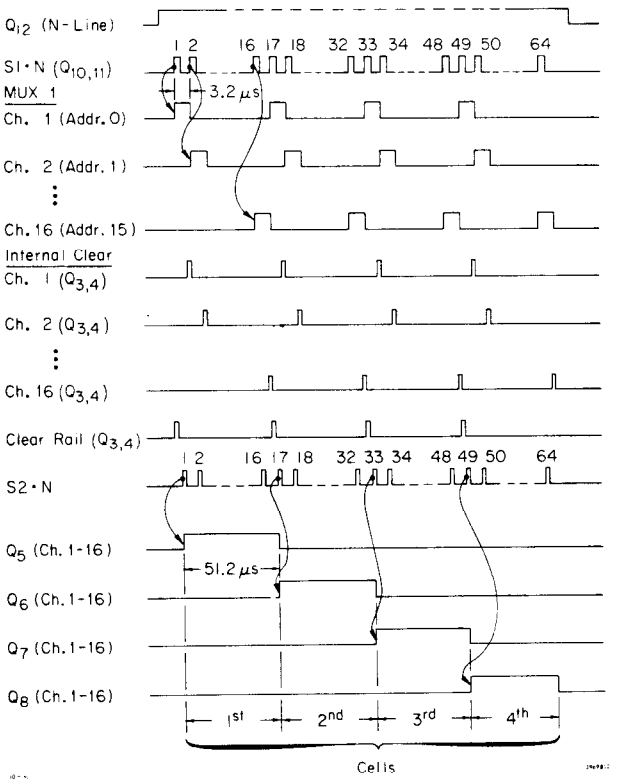

Fig. 5. The READ-OUT timing diagram.

To emphasize the effect of the rail stray capacitance, Fig. 6 shows the read-out of four hits when four identical signals are driving the channel. In this case the correlation between different signals is given by:

$$V_n = V_1\left[1 + \frac{1}{1+a} + \ldots + \frac{1}{(1+a)^{n-1}}\right] \qquad (2)$$

where

$$a = C_s/C_0 \quad , \quad n \geq 2 \quad .$$

Figure 7 shows the same read-out signals in more detail. Note that in the process of reading-out, the effect of the rail capacitance is to reduce the read voltage signal by the factor $C_s/(C_s + C_{02})$ with respect to the voltage V_n across the storage capacitor.

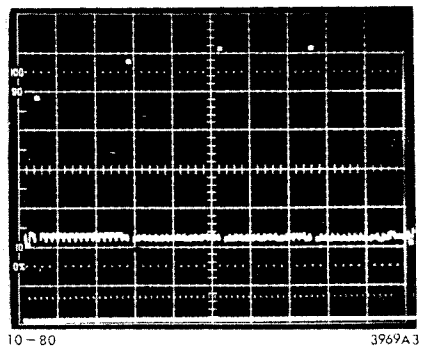

Fig. 6. Read-out cycle.
Upper trace: Analog output signals
Lower trace: S2
500 mV/div. - 20 μs/div.

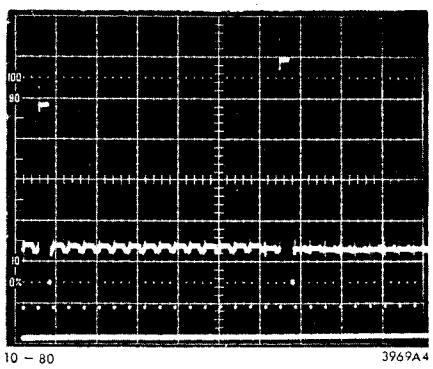

Fig. 7. Read-out : 1st and 2nd hit.
Upper trace: Analog output signals
Lower trace: S2
500 mV/div. - 10 μs/div.

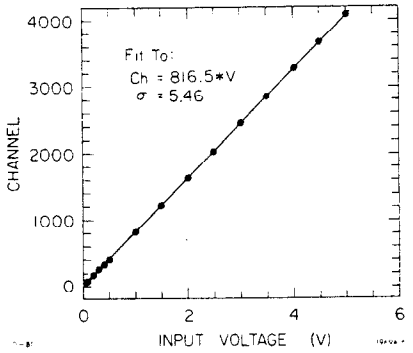

Fig. 8. MSHAM typical transfer characteristic.

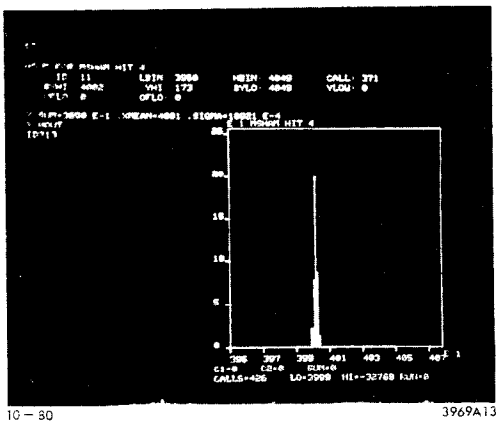

Fig. 9. MSHAM histogram (Channel 2 - Hit 4).

Module Measurements

GAIN : unity-gain was measured for a 100 ns pulse width.

LINEARITY : the transfer characteristic, measured with the BADC, is shown in Fig. 8. The nonlinearity, based on the gain standard deviation, is less than ±0.5%.

NOISE : the noise measured on the pedestals only (without any signal source connected at the input), is V_N = 0.5 mV_{RMS}. The noise measured with a 5V input signal is V_N = 1.45 mV_{RMS}; σ = 1.165 Ch. over 4,096 Ch. full scale. See Fig. 9.

PEDESTAL : the pedestals are no more than 60 mV, as shown in Fig. 10. Note that the pedestals are decreasing from one cell to the following one, because some charge is stored on the rail just before the 1st cell reading-in (due to the switching of Q_1 and Q_2). See Figs. 10 and 11.

CROSS-TALK : the cross-talk measured between two adjacent channels is less than 0.5%.

SETTLING TIME: less than 1 μs at 5V.

PACKAGING : a high density of 112 IC-chips was achieved on a 4-layers CAMAC P.C. board. An overall view of the MSHAM module is shown in Fig. 12.

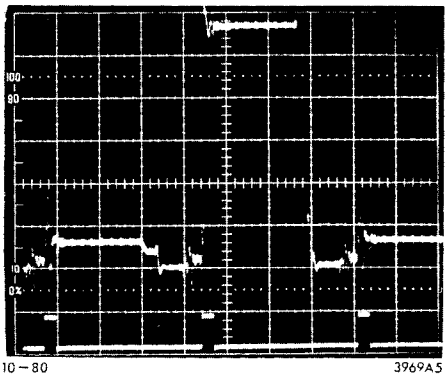

Fig. 10. 1st cell pedestals.
Upper trace: Analog output signals
Lower trace: S2
100 mV/div. - 1 μs/div.

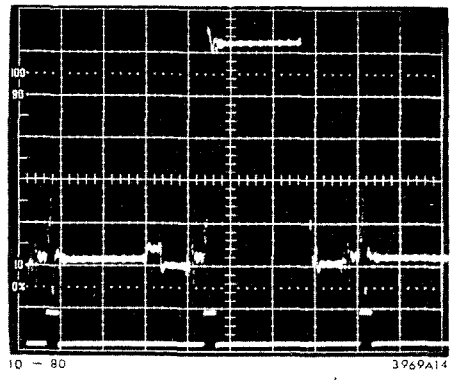

Fig. 11. 2nd cell pedestals.
Upper trace: Analog output signals
Lower trace: S2
100 mV/div. - 1 μs/div.

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References

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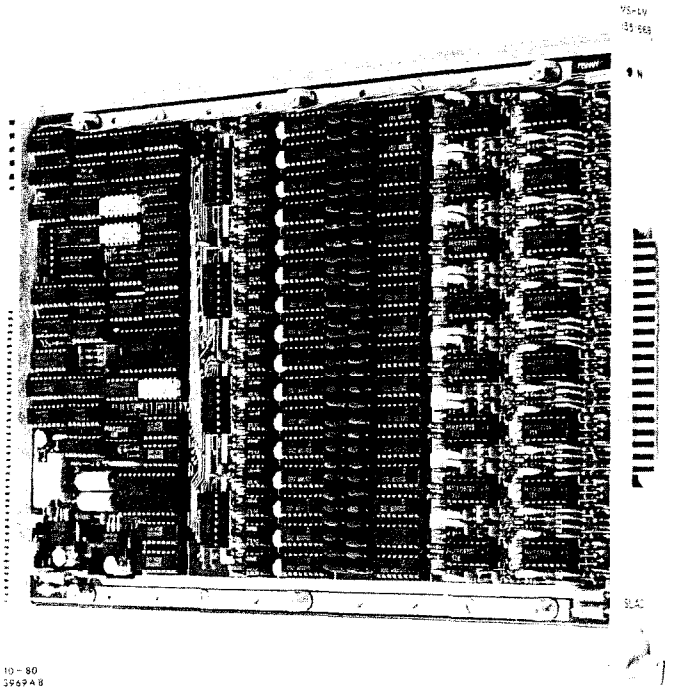

Fig. 12. View of the MSHAM module.