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A MODULAR SAFETY INTERLOCK SYSTEM FOR HIGH ENERGY PHYSICS EXPERIMENTS*

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Abstract

A frequent problem in electronics systems for high energy physics experiments is to provide protection for personnel and equipment. Interlock systems are typically designed as an afterthought and as a result, the working environment around complex experiments with many independent high voltages or hazardous gas subsystems, and many different kinds of people involved, can be particularly dangerous. A set of modular hardware has been designed which makes possible a standardized, integrated, hierarchical system's approach and which can be easily tailored to custom requirements.

Introduction

Many high energy physics experiments require multiple high-voltage sources and associated distribution. High-voltage safety standards require some form of personnel protection, usually including interlocks. In many experiments the detector itself needs to be protected by some form of interlock on the high-voltage system.

Interlock system designs are often left until late in the design of the system and then tend to be detector-specific and difficult to modify or reuse. This paper describes a modular, hierarchical, and reusable interlock system, which allows for the expansion or modification of an installation. Interlock functions may be pyramided to any required depth. Provision is included for two types of interlock: the PRIMARY, or hard, interlock which is always open if any component is open; and the SECONDARY, or soft, interlock which allows the safe bypassing of one portion of an interlock chain following suitable personnel warnings and time delays.

A block diagram of a typical system is shown in Fig. 1. The main components are a master channel and systems power supply unit, slave units, the actual interlock loops, one or more annunciator panels, and the (optional) monitor and control connections to a computer. The following paragraphs provide some construction and operational details.

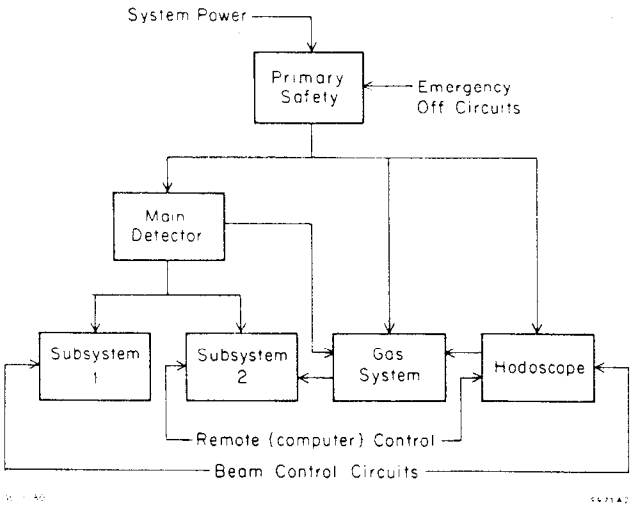

Fig. 1. Block drawing of an example interlock system. Each box represents a channel of interlock logic. System interlock details are not shown.

Basic Function

The units were initially designed as the safety components for high-voltage systems. However, they are of general use wherever the protection of personnel and equipment is required. This system is especially useful in experimental situations because it allows multiple levels of interlocks, and fast or delayed enabled conditions.

The system is packaged using identical channels, either one channel and a master power supply on a panel, or two channels per panel. When all interlock chains are complete, channel turn-on is immediate and may be controlled by one operator. Should the secondary chain be open by the removal of barriers to allow necessary test or equipment repair, the system may be enabled after suitable warnings and delays. This delayed enable requires two operators, one of whom must be physically present at the exposed hazard area.

Provisions are included which allow remote control and computer monitoring (Ref. 1). Interconnections are made by using a low-cost commercial connector system. The system-specific wiring can be discarded as experiments change, and the interlock system can be easily reconfigured for a new experimental installation. Displays show the condition of the interlock chains.

Additional assemblies provided are large 8-channel display panels. These panels may be connected in parallel for ganged displays where required by the physical layout of the experimental area.

Chassis Description

There are three major components of the system. The first is a master chassis (always required) containing the system power supply and one channel of interlock.

The second is the slave chassis, which contains two channels of interlock (Figs. 2 and 3). Power is obtained from the master chassis, either directly, or through one or more levels of interlock, as is sometimes required in cascaded interlocks (Fig. 1). Additional slave chassis may be added as required by the interlock system design.

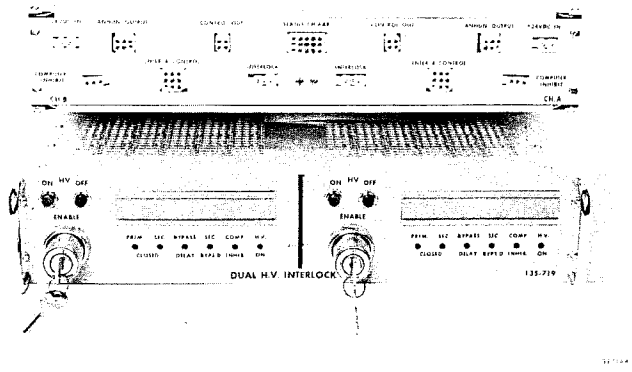

Fig. 2. Slave Chassis, rear and front views.

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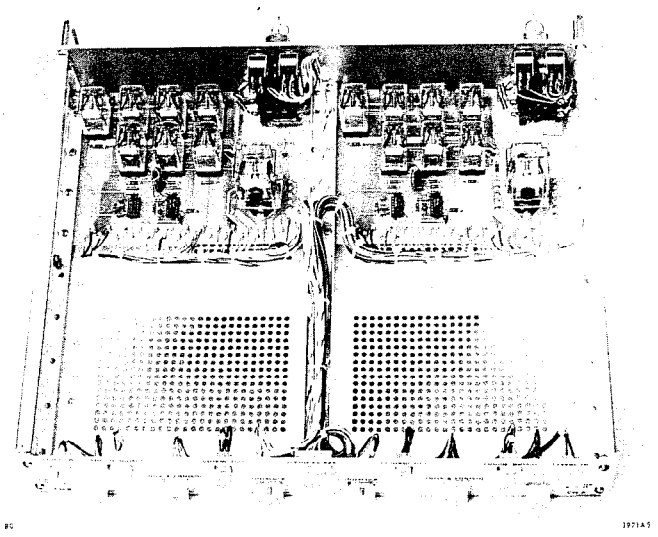


Fig. 3. Slave Chassis, top interior view.

The third component is the annunciator panel, a remote display and alarm panel which is intended for installation in the area where the high voltage systems are actually installed (Fig. 4). A single panel allows the display of up to eight system legends. The display panel face is a plastic sheet containing brief channel function legends, and may be altered as the experiments change. Each legend space is 18.5" × 2.5" on the face of the 24" × 20" × 6" panel. Each legend may be displayed as 'off' (dark), 'to be enabled' (flashing), or 'on' (lighted). Also, each panel includes a rotating red beacon which is in operation whenever any one system is enabled, and a loud bell which alerts personnel when a system goes from 'off' to the 'to be enabled' condition. A provision is included to allow the ganged operation of multiple panels. Panels should be installed so that one is always visible from any location in the hazard area.

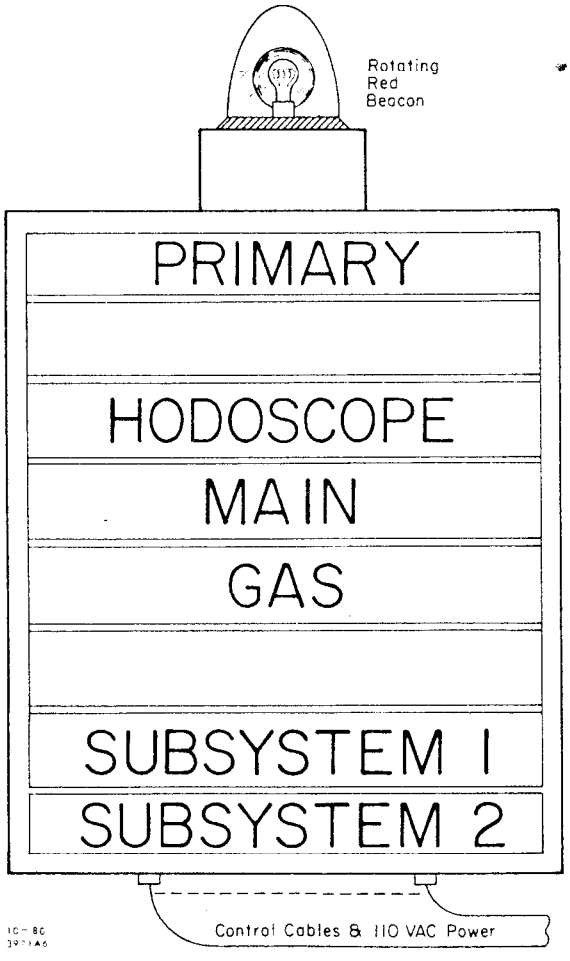


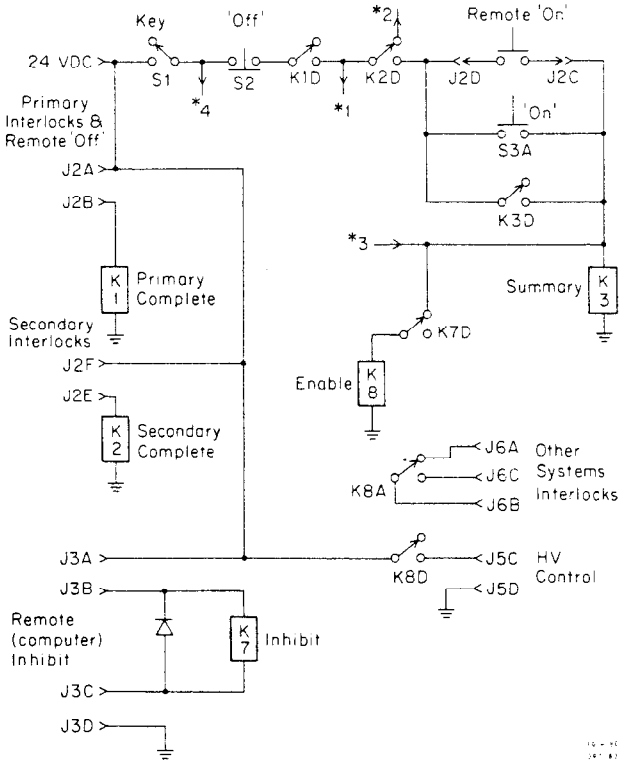
Fig. 4. Annunciator panel for a typical system.

Interlock Circuit Description

An operational description of a single channel is given below. Refer to the block drawings, Figs. 5 and 6, and to the schematic drawing of the master panel (Fig. 7). The schematic shows the system power supply and one interlock channel circuit. J7 may be used to remotely monitor the status of the primary and secondary circuits. The J7 connector on the slave chassis connects the information from both channels of the slave unit. References 2, 3 and 4 list the drawing packages for the three assemblies.

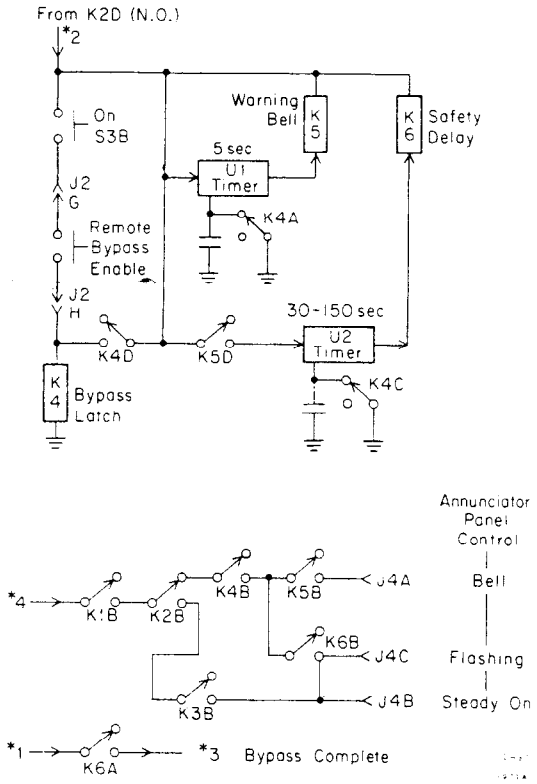
1. Normal Primary and Secondary Interlock Operational Mode (Fig. 5)

When power is connected to a chassis, status power is applied directly to terminal 16 of the printed circuit board so that the status information of the interlock circuits is available before the control circuits are enabled. To operate the control circuits the key switch (S1) is closed and the "HV ON" switch (S3) is actuated. If the interlock chains are complete the summary latch relay (K3) will energize. The holding circuit for K3 is completed via the primary and secondary interlock repeater relay contacts K1D and K2D, and the normally closed contacts of the "OFF" switch (S2A). This applies control power to the enable relay (K8) via the normally closed contacts of the computer inhibit relay (K7D). When K3 is energized the local "HV ON"



* Refers to connections to Fig. 6.

Fig. 5. BLOCK - Normal interlock mode.



* Refers to connections to Fig. 5.

Fig. 6. BLOCK - Secondary bypass mode.

light will come on and power will appear at J4B where it may be used to control a remote status light.

A break in the primary or secondary interlocks, turning S1 off, or pushing the "OFF" switch (S2) will de-energize K3 and thus K8, and power must be restored manually by restoring the open circuit and actuating the "ON" switch (S3), or an optional remote momentary "ON" switch connected between J2C and J2D.

Note: The interlocked high voltage power supplies are always considered "ON" when all the interlocks are complete, regardless of the state of the computer inhibit relay (K7). The computer inhibit circuit is configured to be compatible with open collector drivers and opto-isolators. The computer inhibit relay is controlled via J3.

2. Secondary Interlock Bypass Operational Mode (Fig. 6)

When the secondary interlocks are open the secondary interlock repeater relay (K2) is de-energized and the status and control functions are transferred to the bypass circuit by K2B and K2D. In the bypass mode the status and control circuits are routed through the bypass latch relay (K4), and timer relays K5 and K6.

To activate the bypass circuit two operators are required. One operator must actuate the local "ON" switch (S3) and the second operator must momentarily actuate a remote "Bypass Enable" switch connected between J2G and J2H. K4 latches when both switches are simulataneously actuated. When K4 is energized it starts timer U1, and switches power for local and remote status to contacts of K5 and K6. This timer energizes K5 for approximately 5 seconds allowing K5B to apply power through J4A to sound a remote warning bell. K5D

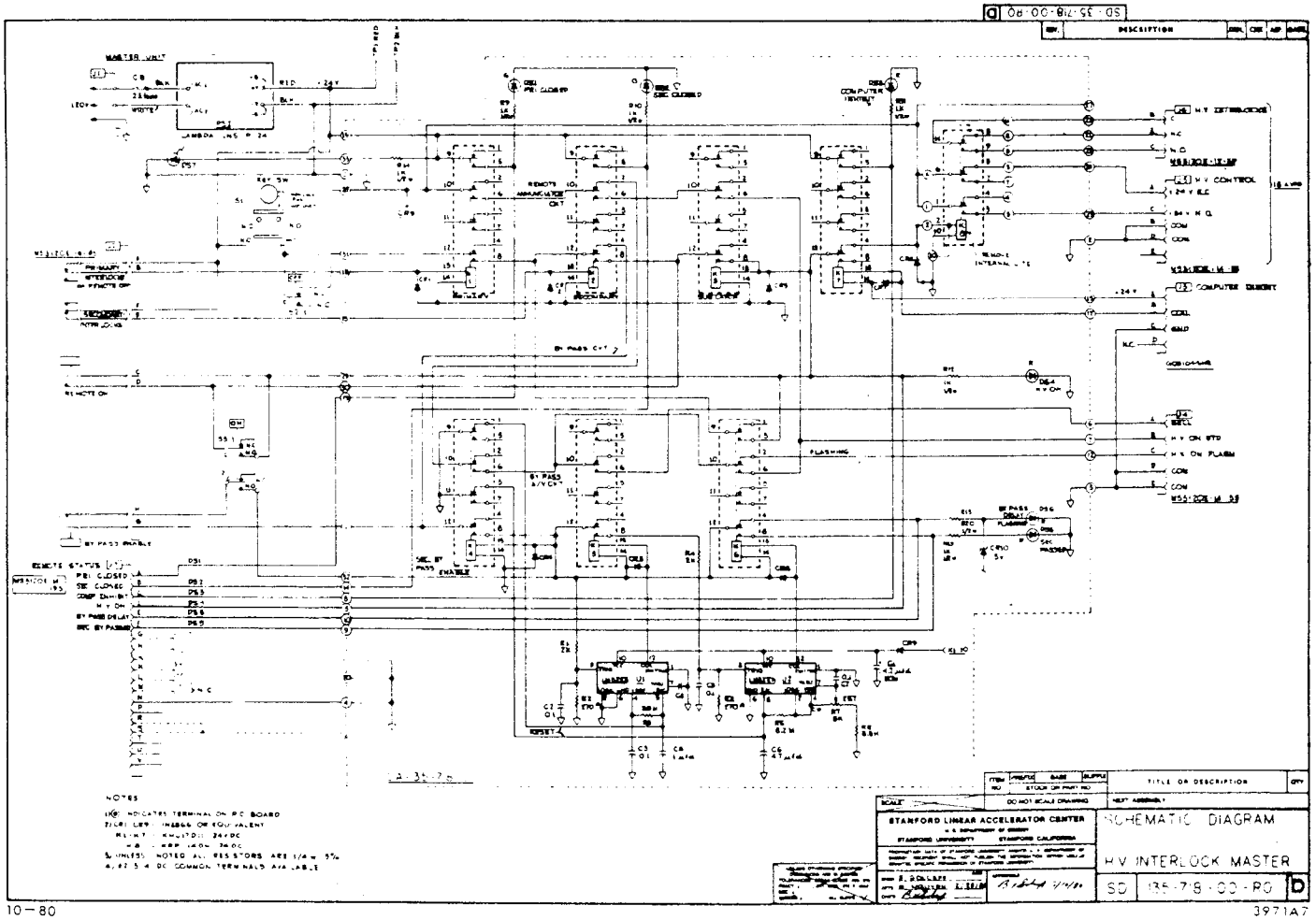


Fig. 7. Schematic Diagram, Master Chassis.

triggers timer U2. U2 is configured in a delayed turn-on mode, and the delay is adjustable from 30 to 150 seconds. During the delay period, K6 is off and K6B and K6D are closed, providing power for a local flashing light, and a remote flashing light via J4C. When U2 times out, K6 energizes, shunting the secondary interlock control contacts (K2D and K3D) via K6A, and the secondary is now bypassed. K3 is now latched, energizing K8, and the local and remote "HV ON" lights are now lit. The secondary bypass mode may be cancelled at any time by opening the primary interlocks, or actuating the "OFF" switch (S2). K4A and K4C are used to reset both timers by shorting timing capacitors to ground.

Summary and Conclusion

We have described a modular interlock system which has been implemented in Experiment PEP-6 (MAC) and has met all basic design goals. The modularity and flexibility of the system components should enable relatively simple configuration of interlocks in future experiments.

Acknowledgements

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