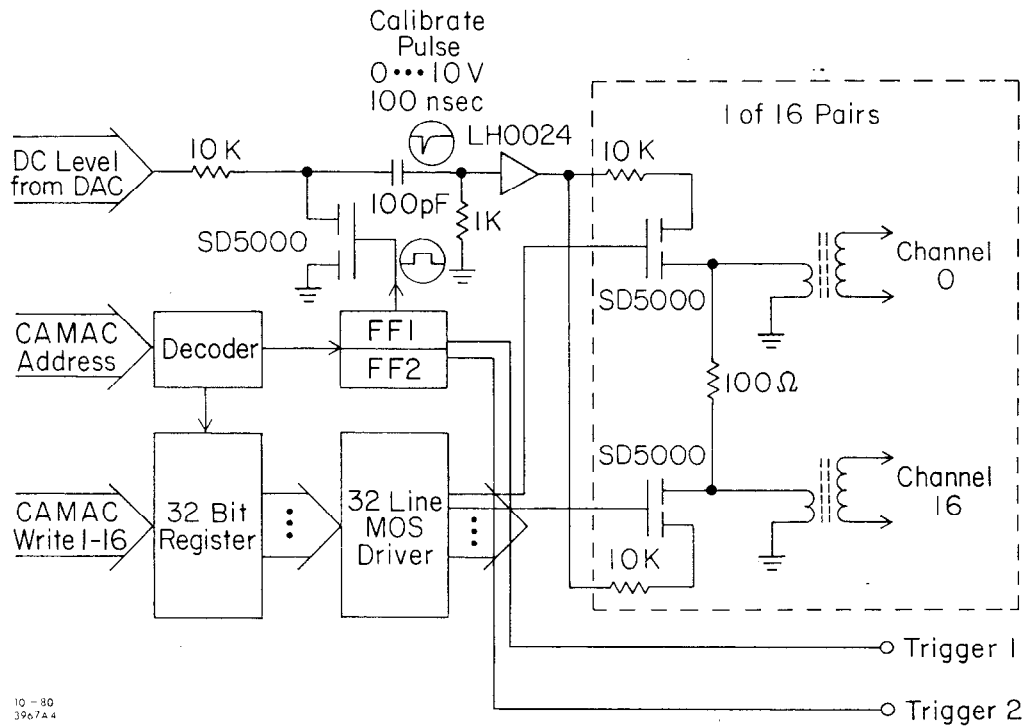


LOW NOISE CHARGE SENSITIVE AMPLIFIER WITH LOW INPUT IMPEDANCE*

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On page 2, "TEST PROCEDURE" section, line 11: for "output" changed to "input".

On page 3, Figure 4: "100 K" changed to "100 Ω ".



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ABSTRACT

This amplifier was designed for use in a large array of proportional wire chambers with charge division readout and for cathode readout of proportional chambers. The single stage high gain (10^4) amplifier with FET input has low component count, low cost, and a high packing density of 32 channels per double-sided P.C. board. Edge connectors are used for input, output, power and calibration signals. The on-board calibration system drives two independent groups of amplifiers through a range which is proportional to a distributed DC level over 3 orders of magnitude. The input and output signals are differentially driven for optimum noise rejection and interchannel isolation.

INTRODUCTION

The amplifier which I am going to describe was designed for use in a large detector containing 50,000 proportional wires. The number of analog channels, however, is much smaller due to the fact that the sense wires are connected in groups of up to 40. The amplifier can be adapted to a range of specifications, but I am going to concentrate on the configuration as used in the MAC detector at SLAC.

The applications in the detector were for:

- 1) Single-ended charge readout from a group of 40 proportional wires connected in parallel.
- 2) Double-ended readout from both ends of a group of proportional wires for determination of the source point of the ionization by the charge division method.
- 3) Collection and amplification of charge induced in large area cathode strips.

This resulted in the following approximate specifications:

Full scale sensitivity	100 pCoul
Input Impedance	5Ω
Noise	<(full scale)/400
Good differential and integral linearity.	

A convenient calibration system and a flexible system of generating sum signals of many analog channels were to be incorporated into the design.

BASIC CIRCUIT DESCRIPTION AND ANALYSIS
 OF THE CHARGE AMPLIFIER

For maximum simplicity and optimum linearity a single high gain amplification stage with negative feedback from the output terminals to the input was implemented (Fig. 1). The input stage is a FET in grounded source configuration. Note that for charge division readout at the low impedance used the FET does not reduce noise compared to a bipolar transistor since the thermal noise from the wire is large. But in other applications the FET reduces noise and the practical advantages to using one amplifier design throughout are considerable. Some work went into determining a good pulse shape. For accurate amplitude measurement a long flat top of the signal is desirable. For that reason an attempt was made in the early design studies to generate a very long pulse with a possibility of reset. However, it proved very difficult to achieve the required dynamic range of 1:1000 and the cost appeared to be high. A very simple pulse shape with ≈ 50 nsec rise, a 2 μ sec decay through zero with a shallow undershoot was finally adopted. Sampling of the amplitude is done at the peak of the pulse. The integration time is not long compared to the fluctua-

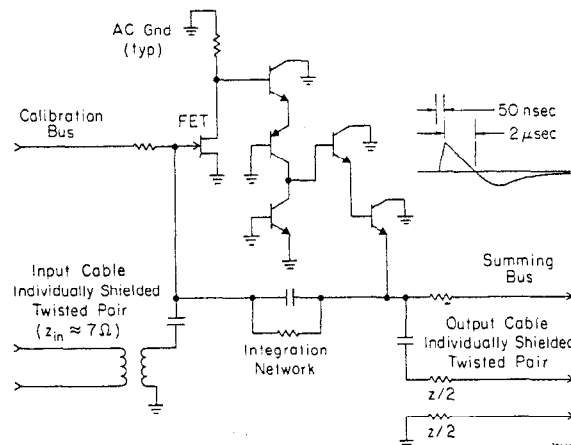


Fig. 1.

tions of drift times in a single proportional cell but such fluctuations should average out over 40 cells.

The individually shielded twisted pair output cable is driven by a Darlington emitter follower through back terminating resistors. This balancing is cheaper than transformer coupling and is good for a 1:1000 crosstalk limit between channels for a 40 m cable run.

The coupling to the input had to be done with some care. At the low impedances used the inductive pickup of stray signals, e.g., a strong radio station, can be severe. Also, there are some subtle problems with the ground return for charge division readout. All these problems could be minimized by using individually shielded twisted pair cable and transformer coupling at the input. A transformer at the sending end would reduce pickup even more but could not be used because of the magnetic fields near the detector. Transformers wound with Teflon wire are also used for high voltage insulation.

CALIBRATION CIRCUITRY

For convenient checkout, calibration circuitry is provided as an integral part of a 32 channel amplifier board. The method used is the discharge of a precision capacitor which has been charged to an externally supplied DC level through a network of precision resistors simultaneously into a group of 16 amplifiers. Two groups of amplifiers can be pulsed separately: Either alternate channels (odd-even) or, with modified jumpering, the right or left 16 channels. The discharge of the capacitor is performed through two DMOS switches on the board which are activated by TTL signals. The calibration circuitry (Fig. 2) is linear over more than three orders of magnitude.

The distribution bus does not introduce measurable crosstalk at the 1:1000 level.

SUMMING AMPLIFIERS

For purposes of performing operations on output signals from groups of amplifiers, four summing amplifiers are provided per board of 32 charge amplifiers. There are patch facilities for connecting any number of subgroups of four amplifiers to any combination of the four summing amplifiers. The summing amplifier pro-

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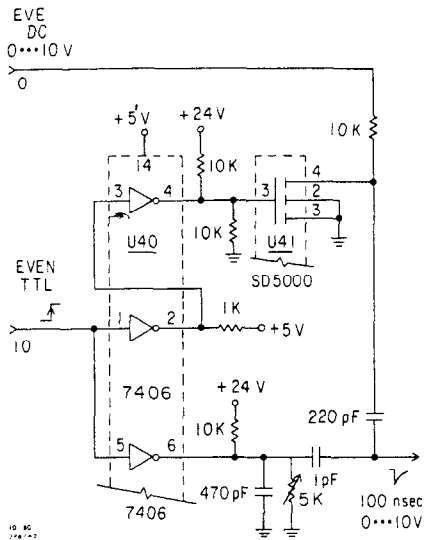


Fig. 2.

vides an input impedance of $<2\Omega$. The measured crosstalk from one channel into any other due to the summing bus is less than 1:1000.

GENERAL LAYOUT

The physical construction of the amplifier is shown in Fig. 3.

Thirty-two charge amplifiers, four summing amplifiers, two calibration channels and voltage regulators are housed on a double-sided P.C. board of 17" by 10"

area, 3/4" high. No crosstalk at the 1:1000 level was observed between channels even though no shielding walls are installed between the closely spaced amplifiers. All transistors and the gain determining elements are on sockets. This arrangement facilitates servicing and repair.

Six boards are mounted in a flat cage which at the rear holds two connectors per board for distribution of power and calibration signals and for the amplifier output and sum out signals. Input cables come in at the front.

The calibration circuitry near the input, summing amplifiers near the output and the on board regulator providing a low noise supply voltage can be seen on the photo as separate groups.

The amplifiers are run off a single-ended 24V supply voltage at 10 mA per channel or about 60W per cage of 192 channels. This is low enough to make special provisions for cooling unnecessary.

TEST PROCEDURE

Testing of the ≈ 4000 amplifier channels proceeded in two stages. The first step was the usual debugging run using an oscilloscope and a manually controlled test setup.

A number of the more subtle errors, e.g., faults which reduced the open loop gain or leaky components adding to the noise, could not be caught at this stage. For that reason an automatic test procedure was set up which measured all the relevant properties of the amplifiers and produced a printed summary. The open loop gain was determined through a measurement of the output impedance, the quantity of interest for the user (Fig. 4). For that purpose the amplifiers are connected in pairs through 100Ω resistors approximating the config-

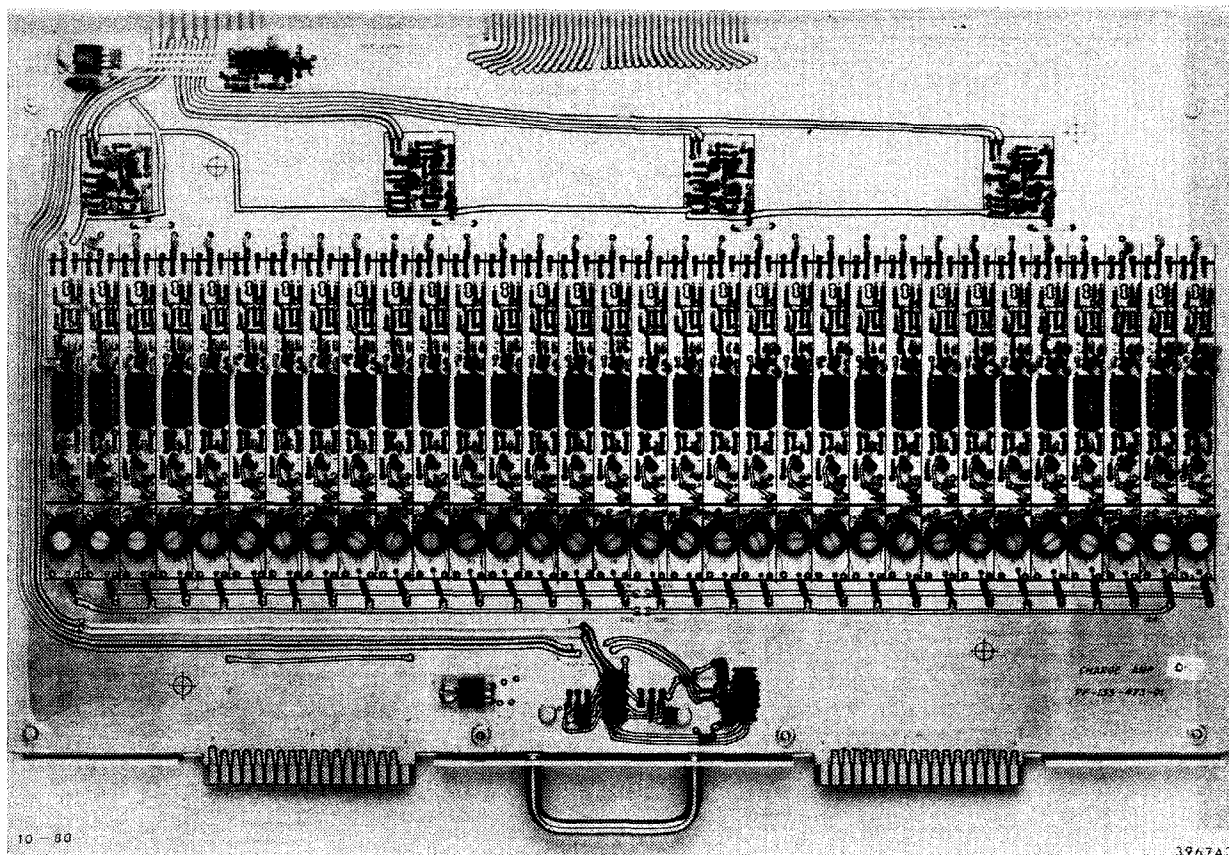


Fig. 3.

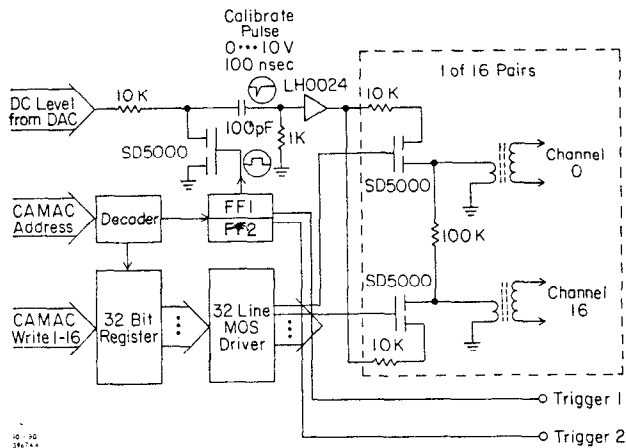


Fig. 4.

uration of the experimental setup. Under control of a computer, pulses are fed through electronic switches into either of the connecting nodes of a pair of amplifiers and the amplitudes in the two channels digitized. This yields four numbers for each pair of amplifiers from which the two gains and the two input impedances can be determined separately. The calibration circuitry is tested in the separate program loop which also tests linearity. Each type of programmed pulse is sent out 10 times and the variance of the result is calculated to measure the noise in the channel. Figure 5 shows the distribution of input impedance determined with this system. An example of the summary printout is shown in Fig. 6.

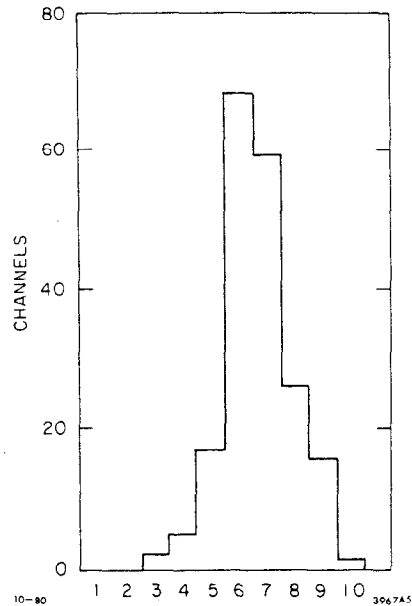


Fig. 5.

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SER. NO.= 44
0 CAL= 3367 9 (OBS-PRED)= -35
1 CAL= 3264 9 (OBS-PRED)= -29
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.
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30 CAL= 3401 15 (OBS-PRED)= -27
31 CAL= 3646 16 (OBS-PRED)= -24
RMIN= 4 RMAX= 9
AMIN= 3218 AMAX= 3646
NSMIN= 0 NSMX= 10

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R= 5 REL.GAIN= 102 NOISE= 0
R= 7 REL.GAIN= 103 NOISE= 10
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R= 5 REL.GAIN= 105 NOISE= 0
R= 6 REL.GAIN= 105 NOISE= 9

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10-80
3967A6

Fig. 6.

ACKNOWLEDGEMENTS

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