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HIGH RESOLUTION TIME-OF-FLIGHT ELECTRONICS SYSTEM*

J. Evan Grund

Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

ABSTRACT

A new electronics system for time-of-flight measurements has been developed to meet the performance requirements of the Mark II Detector for operation at the PEP Storage Ring of the Stanford Linear Accelerator Center. This system incorporates high resolution time measurements with the capability to correct systemic errors from the scintillator and photomultiplier tubes. The correction technique involves making three measurements on each photomultiplier signal every storage ring beam interaction. Two timing measurements are made relative to the beam interaction time with different discriminator threshold level settings. The charge integral of each photomultiplier pulse is also recorded. These multiple measurements allow computer correction of errors due to discriminator walk with pulse amplitude, timing errors due to scintillator light attenuation and spread, and finite rise-time limitations of the photomultiplier and cabling. The system can be quickly reset after each beam interaction if there is no trigger, thus eliminating any need for delay cables in photomultiplier signal cabling. The electronics designed for the new time-of-flight system is the subject of this paper.

SYSTEM REQUIREMENTS

This electronics system is to provide improved processing of signals from the existing Mark II time-of-flight scintillation counters. Figure 1 shows the location of the 48 counters which have photomultiplier tubes installed on both ends. The time period to be measured is from when the storage ring beams collide in the vacuum chamber, to when particles are detected by the scintillators.

The system goals include:

1. High time resolution circuitry so that electronic noise is negligible compared to the scintillator time resolution,

2. Provide means to correct for "time walk" which is normally observed when input pulse shape or amplitude varies,

3. Simple system calibration, in which calibration coefficients (and channel-to-channel variations) are automatically measured and applied to the data,

4. Formatting and linearization of data to minimize the required CAMAC transmission time (with its accompanying system dead-time) and host computer processing overhead, and

5. High density CAMAC system packaging with a minimum of required cables.

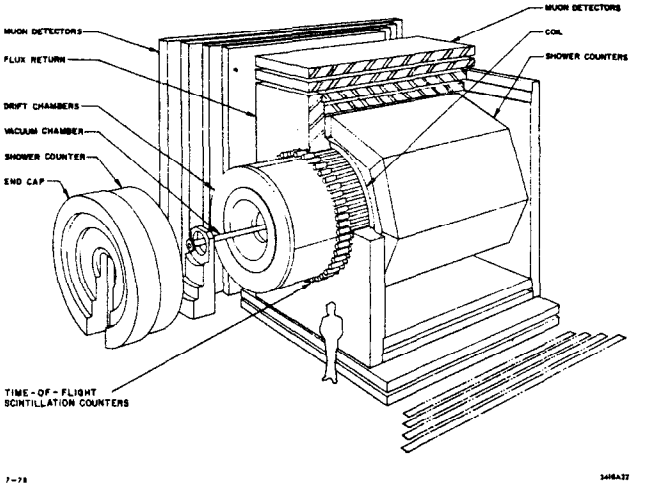

Figure 1: Isometric view of the Mark II Detector

SYSTEM HARDWARE

This CAMAC based time-of-flight (TOF) system, diagrammed in Figure 2, consists of a "TOF Strobe Generator" or STROBER (one single width CAMAC module per crate), a "TOF Threshold Controller" or THRESHER (one single width module per crate), "TOF Discriminator Modules" or DISCO's (single width modules which accommodate four photomultiplier signals each), and a "Brilliant Analog-to-Digital Converter"(1) or BADC autonomous controller, designed with digitizing and processing capabilities (one triple width module per crate).

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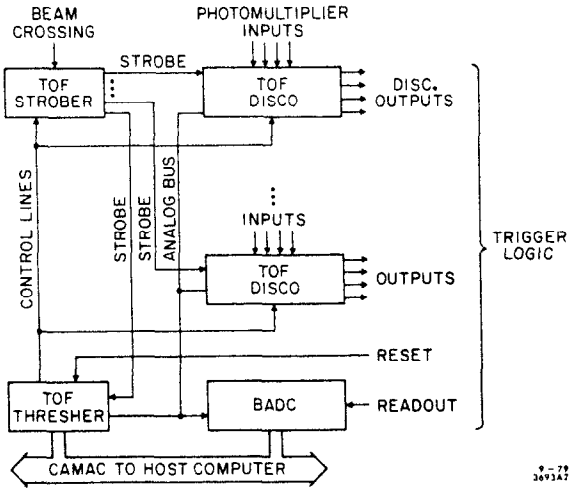

Figure 2: System Block Diagram

STROBER - Strobe Generator

The system operation is synchronized to the storage ring beam crossing by a "XING" NIM logic signal which is generated from a beam pickoff sensor. The STROBER generates a pulse of precise width, called "STROBE," from the XING signal. STROBE is furnished to all the TOF Modules from 16 NIM logic outputs. This is the reference signal for the timing measurements; the leading edge of STROBE enables DISCO's to begin timing measurements, while the trailing edge terminates their timing periods.

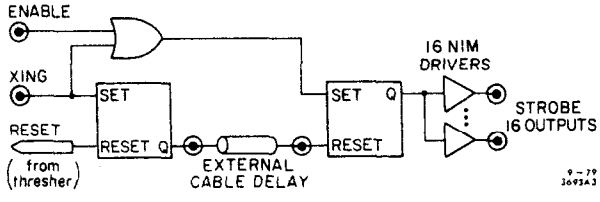

Figure 3: STROBER Block Diagram

The DISCO's are enabled only after beam crossing so that they ignore the cosmic ray background counts that occur prior to beam crossing. This enabling after XING arrives can possibly cause a timing problem. The velocity of the XING signal through its cabling is only two-thirds that of the beam particles velocities, and XING may actually arrive at the electronics after valid scintillator signals. Instead of adding delay cable in the scintillator paths, the chosen solution is an "ENABLE" signal, generated from the PEP RF system, which can be used to begin the STROBE period. STROBE's back edge is the critical timing edge, therefore it is always timed from the high precision XING signal. The STROBE timing period is controlled by an external cable delay, so that it is adjustable and very stable.

Since we want measurements only during system live-time, we require the TOF system "RESET" signal (which originates at the trigger logic) to proceed an ENABLE or XING signal before a STROBE can be generated. Since RESET's occur only during system live-time, STROBE's are not produced during readout time, even though ENABLE and XING signals continue. This allows gating circuitry to be avoided in the critical XING signal path, and the single RESET signal from the trigger logic can control both the measurement and readout modes.

THRESHER - Threshold Controller

The THRESHER's purpose is to take directions from the detector's trigger logic, the BADC and/or host computer, and generate the necessary signals to control all the DISCO's in a CAMAC crate. Figure 4 shows the signal paths through the THRESHER.

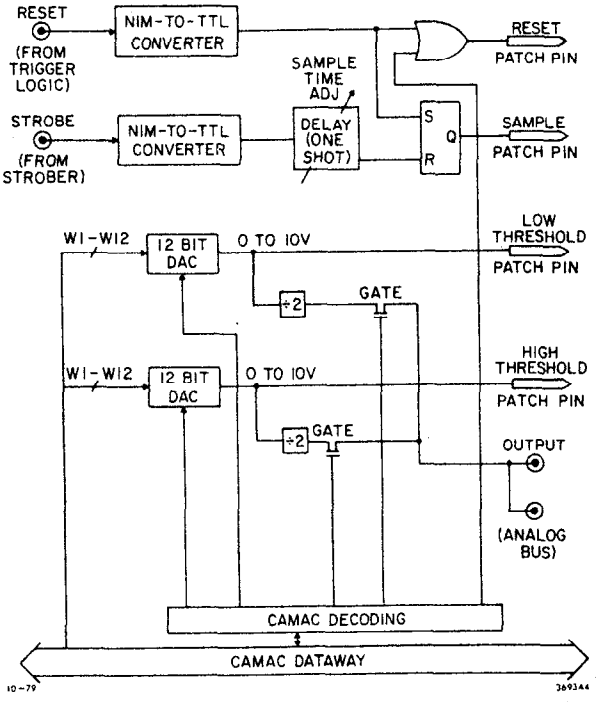

Figure 4: THRESHER Block Diagram

Control from the trigger logic requires only one signal, RESET. This NIM logic signal which is 250 to 1000 nanoseconds in width, must proceed every measurement. The THRESHER translates this signal to TTL levels and sends it down a CAMAC DATAWAY patch pin to the STROBER and all DISCO's in the crate. The STROBER responds by setting a flip-flop to enable a STROBE signal generation at the next beam crossing, while the DISCO's reset their measurement circuits.

A signal called "SAMPLE" is also generated by the THRESHER. SAMPLE controls the track-and-hold section of the DISCO's charge integrator.

Two analog signals are produced which control the DISCO's "LOW and HIGH THRESHOLDs." They are 0 to 10 volt signals from CAMAC controlled digital-to-analog converters. Patch pins on the DATAWAY bus these voltages to the DISCO's where these voltages are inverted and divided by 10 to set the actual discriminator levels to a 0 to -1 volt range. The voltages that are on the patch pins can be gated to the TOF analog bus (divided by 2 to fit the BADC's input range) by CAMAC commands, so the BADC can monitor the threshold voltages. Using the CAMAC patch pins reduces the amount of cabling required to control the DISCO's.

DISCO - Discriminator Module

The actual time measurement is done by the DISCO modules. Each DISCO has four photomultiplier (PMT) inputs, and makes one analog and two timing measurements on each. Time resolution measurements made by this module on photomultiplier signals have a time jitter of less than 10 picoseconds RMS, and when using clean (NIM level) inputs, 2 picosecond RMS noise can be obtained.

Figure 5 shows the main DISCO functional blocks. The timing reference, STROBE, is converted from NIM to ECL levels by the same discriminator circuit used for the PMT signals. Discriminator time walk due to temperature changes (about 12 ps/°C) is therefore largely cancelled by compensating the time reference to match the signal delay change. An electronic analog thermometer is also provided and can be monitored through the BADC for further thermal corrections by computer. STROBE and buffered THRESHER control signals are bussed to all measurement sections, which are labled "input circuits" in Figure 5.

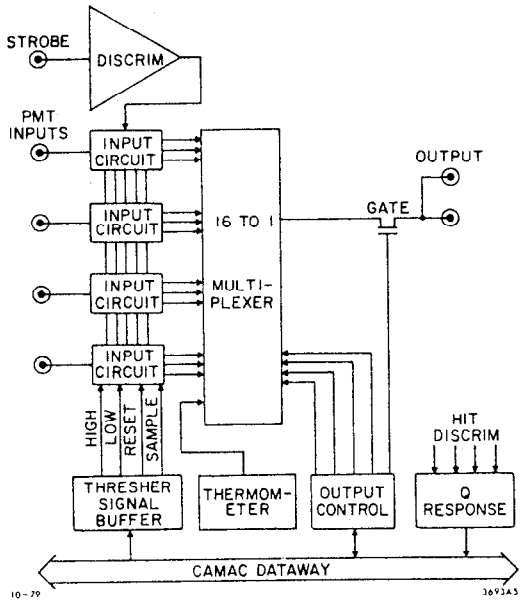

Figure 5: DISCO Block Diagram

All measurements can be gated to the analog bus called "OUTPUT" under CAMAC control. The OUTPUT's of all DISCO's and the THRESHER are daisy-chained together, and they form the BADC's input. To eliminate the reading of DISCO's that did not receive any PMT signals, a CAMAC Q Scan, or 'ACA - Address Scan Mode,'(2) can be used. The Q response is generated only when one of the low threshold discriminators has seen a 'hit'.

DISCO's Input Stage. The PMT signals are inputs to discriminators whose thresholds are set from the THRESHER. When a photomultiplier signal voltage exceeds the set threshold level a "START" signal is produced which begins a timing period. A NIM "DISC" output signal is available on the front panel for each photomultiplier channel for possible use in other logic. The discriminator circuits are self-latching so that once they are triggered, the time measurement will continue until STROBE terminates the timing period regardless of input pulse widths. The conversion of a time interval to a voltage is the time-to-amplitude converter's function.

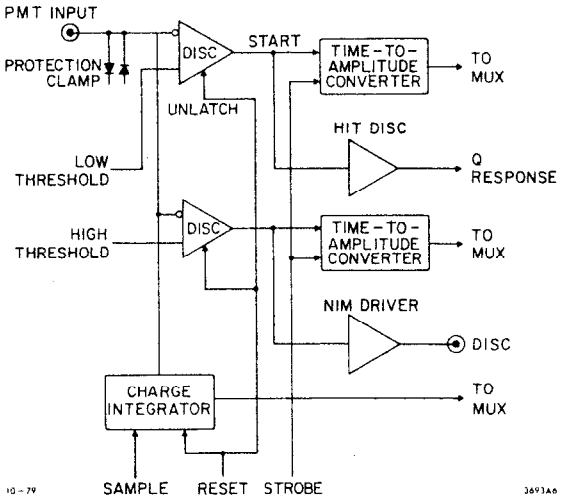

Figure 6: DISCO Input Circuit Diagram

Time-to-Amplitude Converter. The time interval is defined as beginning with a START from a discriminator and ending with STROBE's back edge, which functions as a common stop. A capacitor discharge circuit, Figure 7, using a switched current source generates a voltage representative of the time interval.

The capacitor discharge or rundown circuit operates as follows. C1 in Figure 7 is precharged to "5V REF" by Q2 during the RESET period. During the time period to be measured, a 10 milliampere current source linearily discharges the capacitor. The resultant capacitor voltage represents the time interval. The capacitor is buffered by a FET amplifier so it performs as a sample-and-hold circuit that holds while the voltages are read and digitized. The current source is switched 'on' and 'off' by a transistor array that forms a current-switch tree. This series gating technique logically AND's the START and STROBE

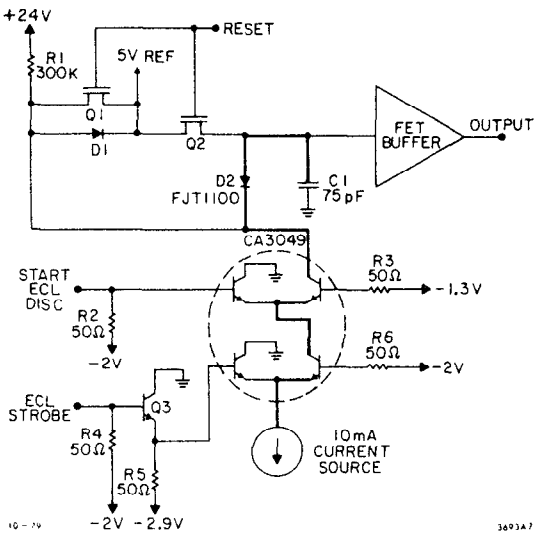

Figure 7: Time-to-Amplitude Converter Schematic

signals together. D2 allows C1 to be discharged, while isolating C1 from leakage currents during the long readout period. The leakage current from the transistor array flows through R1. This resistor has a large value, therefore it approximates a small constant current source during rundown, and does not add nonlinearity. At the end of a rundown, R1's current causes the transistor array's collector voltage to rise to where D1 clamps it. D1's clamp to a fixed voltage is important because when the voltage at D2's cathode slews, D2's capacitance pumps charge into C1. In this case, the amount of pumped charge is approximately proportional to the final rundown voltage, so linearity is preserved. Q1 is needed to quickly discharge the parasitic capacitance at D2's cathode, but it causes one operational requirement. At the end of RESET, D2's cathode voltage is at 5 volts and will be ramped to 5.6 volts, where D1 clamps it. Unless the time between RESET and STROBE (i.e. the start of timing) is long, it must be fixed to a few nanoseconds. Holding this interval constant means that the small amount of charge pumped into C1 will be a constant plus an amount proportional to the measurement period, hence the error is calibrated away.

A major circuit problem in this type of rundown circuit is the memory effect that is caused by the dielectric absorption of the rundown capacitor, C1 of Figure 7, and all stray capacitances that are in parallel with C1. This effect can cause a time measurement to vary by over 100 picoseconds, depending on the values of previous measurements. Component selection and layout can reduce this effect (C1 is a polystyrene capacitor in this design), but the effect can not be eliminated as it is not due to C1 alone. A small total capacitance of 100 picofarads is needed to obtain the desired time resolution from the 10 milliampere switched current source. Stray capacitances on the printed circuit board, and the capacitances of the various silicon devices account for one-quarter of the total capacitance. Since one has little control over the active device dielectrics, and their effects can not be made negligible by a large passive capacitor, operational techniques must complement the circuitry's limitations.

Three techniques are used to reduce the memory problem: common stop operation, fixed readout rate, and after readout reset. These operational techniques apply the argument that if the undesired memory can not be removed, we must control what is remembered, determine what the subsequent error is, and then this predictable error can be treated as a calibration factor and removed.

First, a simple description of the memory effect is in order. After setting at a fixed voltage for a long period, a capacitor's dielectric comes to a stressed equilibrium which is a function of the applied electric field. Changing the applied voltage will change the E field and a new equilibrium will be established with a time constant of roughly a few milliseconds. Therefore, if we suddenly change the voltage on a capacitor from 5 volts to 1 volt (like a rundown does) and then isolate the capacitor (as during a readout period), the voltage will slowly drift upward a small amount (e. g. a 50 millivolt drift that settles in one-quarter second).

The common stop operation was chosen so that the capacitor would remember its beginning voltage, 5V REF shown in Figure 7. The typical duty factor for a discriminator channel is 1%, and with the common stop operation, only a channel that is hit will have a capacitor voltage change. Therefore, the capacitor's memory "soaks" up the 5V REF level 99% of the time. Because the dielectric time constants are long, a quick rundown and reset does not change the memory significantly. Measurements made with and without a hit (and rundown) on the previous beam crossing differ by only a few picoseconds.

With a common start system there would be a rundown every beam crossing, so an average (time integral) voltage is remembered. Also with common start, during each readout period a constant voltage is held and that voltage becomes remembered. When rundowns again commence, the memory begins to forget that constant value and starts remembering the new average. This memory change takes several milliseconds, so a trigger and a new readout will probably start before the memory effects have settled, causing an unpredictable drift.

The common stop operation makes the memory drift reproducible. During the readout period one would expect most channels to be at 5V REF (not hit) and a few to have a voltage about 1 volt (a hit shortly after crossing) and be slowly drifting upward. The amount of drift (to a first approximation) is proportional to the initial voltage change. The BADC is programmed to read, digitize and store all the channels in the same order and at the same rate each readout period. This means the drift in a particular channel will always be the same for the same initial voltage after rundown. Hence, when it is read (between 10

microseconds and a few milliseconds later), it will have moved a repeatable drift amount which is automatically removed when the calibration coefficients are applied.

During the readout period we still have the condition where a few channels are soaking up a new memory value. This error is reduced by dividing the readout period into two subperiods: DISCO to BADC transfer and BADC to host computer transfer. During the first subperiod, the capacitor voltages must be held, but during the second subperiod, which is usually longer than the first, the capacitors are reset to 5V REF and held there until the system begins taking data again. This is accomplished by the BADC sending a CAMAC command to the THRESHER after all channels have been read, causing a long RESET before new measurements.

Charge Integrator. The charge integrator is a one transistor circuit approximating a voltage controlled current source driving a critically damped RLC circuit. Figure 8 shows the integrating and buffering circuits. R1 terminates the PMT cable in its characteristic impedance and the current from the photomultiplier is converted to a negative voltage pulse. The negative input pulse to Q1's base causes its emitter voltage to drop a like amount. The voltage across R2 drops so the emitter and collector current flows of Q1 are reduced by an amount proportional to the input voltage. Q1's collector load is L1, C1 and R4. L1 approximates a constant current source that equals the quiescent current through Q1. When Q1's current drops, some of L1's current then flows into C1, causing Q1's collector voltage to rise. This voltage rise is a time integral of the input charge. RLC critical damping is used as this is the best trade off between fast recovery and minimum droop during the measurement period. This circuit produces a reasonably linear charge time integral for input pulse widths of under 25 nanoseconds while recovering to the quiescent operating point before the next beam crossing (2.4 microseconds later).

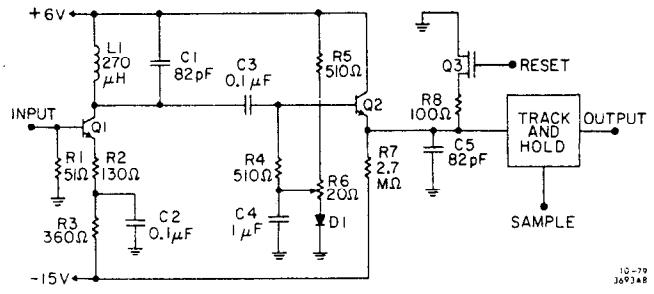

Figure 8: Charge Integrator Schematic

C3 couples this signal to the base of Q2, an emitter follower. The quiescent emitter voltage of Q2 is slightly positive, adjusted by R6. D1 helps cancel the thermal drifts of Q2's base-emitter junction. The emitter load of Q2 is mainly capacitive, so Q2 functions as a peak stretcher. This allows a moderate speed track-and-hold to be used at the expense of an additional reset switch (Q3), and a slight nonlinearity at low values of charge due to variations in Q2's base-emitter voltage drop from changing emitter currents.

The peak stretcher is followed by a track-and-hold circuit which captures the integral voltage for later readout. The track and hold enters the hold mode at the end of the SAMPLE period which is controlled by the THRESHER.

DISCO Construction. The component layout of the printed circuit board is one of the most critical design steps. The large amount of circuitry makes the layout dense, while the diversity of component types (TTL, CMOS and ECL digital IC's as well as high speed IC and discrete amplifiers) requires many different supply voltages. The high speed circuitry used needs 50 ohm transmission lines to produce clean, quite signals.

The circuit board has four layers. The layers are numbered from the component side, and their functions are:

1. Low speed or non-critical signals and power bussing,

2. A -2 volt plane used for ECL termination, CMOS supply voltages, a few long runs and critical high impedance nodes,

3. The ground plane, and

4. High speed signals (50 ohm microstrip lines) and critical low speed signals and power bussing.

The four channels are shielded from each other by bus bars that also distribute four power supplies.

The single width CAMAC module packaging was necessary to house all the electronics that is needed for processing the PMT signals coming from the Mark II in two crates. Figure 9 shows the prototype DISCO.

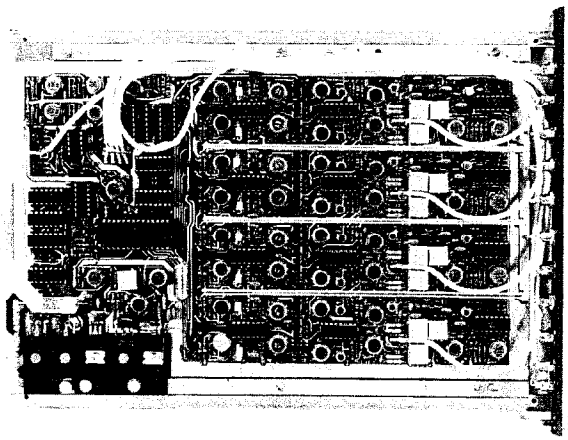

Figure 9: DISCO Prototype

BADC - Brilliant Analog-to-Digital Converter

All twelve measurements from each DISCO module can be multiplexed onto an analog bus which is common to all the TOF modules in the crate. The advantages of this analog bus structure is described in reference 3. The voltages, which are representative of the times and integrated charges, are multiplexed onto the analog bus, digitized, corrections applied and results formatted automatically by the BADC. The host computer can then read the data in corrected, condensed form.

The BADC functions as an autonomous crate controller for system calibration and data readout. Under its control, reference signals can be sent to the PMT inputs of the DISCO's. Resultant measurements are then fitted to a second degree polynomial model. The polynomial coefficients are internally stored and applied to the raw data each readout period by the BADC.

After the data is transfered to the host computer, or after a beam crossing that did not produce a trigger to initiate a data readout cycle, the trigger system issues a RESET and data will be taken at the next beam crossing.

CONCLUSION

This instrumentation package will be installed at PEP Interaction Region 12 as part of experiment PEP 5, in November of 1979. The resulting increase in electronic resolution is expected to have an important impact on particle speed measurement and hence particle identification. The multiple measurements will extract more information from the scintillator signals. This additional information will enable a computer correction technique to significantly improve the time-of-flight system resolution. These correction algorithms will be the subject of a future report.

ACKNOWLEDGEMENTS

M. Breidenbach was instrumential in the conceptual design of this system. D. Nelson was responsible for the circuit design of the THRESHER.

REFERENCES

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(2) IEEE Std 683-1976, IEEE Recommended Practice for Block Transfers in CAMAC Systems.

(3) E. L. Cisneros, H. K. Kang, J. N. Hall and R. S. Larsen, IEEE Trans. on Nucl. Sci. NS-24, No. 1, 413 (1977).