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MICROPROCESSOR STANDARDS

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ABSTRACT

The current status of standardization efforts proceeding under the IEEE Computer Standards Committee of the IEEE Computer Society is summarized as of October 1979. Names and addresses are listed as sources for further information.

INTRODUCTION

The Computer Standards Committee of the IEEE Computer Society, chaired by Robert G. Stewart, is involved in several standardization efforts which may be of interest to people working in data acquisition and control. Most of these projects are being carried out by subcommittees of the Microprocessor Standards subcommittee, which was organized in 1977 by Dr. Stewart, and is currently chaired by Gordon Force.

These projects arose out of the frustrations of engineers working in microcomputer applications, initially due to the inadequate specification of the common microcomputer buses, and later expanding to include software aspects. The committee work is mostly carried out by volunteers on their own time, with interested companies contributing peripheral support, such as use of duplicating facilities from time to time.

A project called Futurebus has served as a focus for identifying additional bus standards which will be needed in the near future, and has resulted in the formation of the Future Backplane project and the Local Networks project. Standardization work is nearly complete on the S-100 bus and on Intel's Multibus.

Software related projects include a standard for choosing assembler language mnemonics, a high level language project which is attempting to make existing languages more suitable for use with microprocessors, a joint project with ANSI for the standardization of PASCAL and its extensions, and a project seeking a common standard for relocatable object code.

A project which has both software and hardware implications is the Floating Point Standard project, which is intended to facilitate communication at the hardware level among devices which use floating point, specify computational algorithms for arithmetic operations so that various processors will get the same results for the same calculation, and specify behavior under exceptional conditions in a way which maximizes the useful information returned to the programmer.

Because of the desire to get useful standards defined as soon as possible, most of these efforts have relied on small core groups to quickly create a draft document, which is then published as widely as possible for comment, and revised on the basis of the feedback received. Some topics have proved of such wide interest that the committees have grown to larger size and progress has slowed, but this is necessary in the case of controversial subjects.

To contact the Computer Society's Standards Committee chairman, write Robert G. Stewart, Chairman, IEEE Computer Society Standards Committee, Stewart Research Enterprises, 1658 Belvoir Drive, Los Altos, CA 94022; (415) 941-6699. To contact the Microprocessor Standards Subcommittee chairman, write Gordon Force, Kylex Corporation, Chairman, Microprocessor Standards Committee, 1128 Amur Creek Court, San Jose, CA 95120; (408) 268-3692.

THE S-100 PROJECT
(IEEE Task No. P696)

The S-100 bus was one of the first targets of standardization efforts. Originally the 8080 microcomputer bus used in the MITS Altair 8800, the first digital computer widely sold to hobbyists, the bus was largely defined by a list of signal names and the 8080 timing characteristics. When a large number of manufacturers began supplying boards to plug in to the bus, the name S-100 was generally adopted, meaning the Standard bus with 100 pins.

Because the bus was not well specified, and because of some unfortunate design decisions in the original, compatibility problems soon arose so that some combinations of boards did not work reliably. The arrival of the Z80 and other microprocessors with different timings than the 8080, as well as higher speed versions, made the situation worse. Inadequate grounding caused noise problems, and some control lines which were active high in the TTL bus caused problems during transfers of bus mastership to direct memory access (DMA) controllers. In addition, a new wave of microprocessors with 16-bit words and larger address spaces is about to arrive, calling for standardized extensions to the bus.

These problems have all been addressed in the draft standard. A protocol for DMA has been defined which works reliably, a priority arbitration method for selecting the next master without resorting to off-bus daisy chains has been devised, additional ground lines have been specified, processor independent timings have been specified, and mechanical and electrical specifications have been developed.

In addition, optional expansion of the bus for 16-bit data words, 16-bit I/O port addresses, and 24-bit memory addresses has been accomplished. The original bus had separate 8-bit data-out and data-in buses, which have been converted to a single 16-bit bidirectional bus for 16-bit transfers. This has been done in a way which allows compatibility with old boards and allows intermixing of 8- and 16-bit devices in one system.

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The byte addressing within a word (the most significant byte has the lowest or even address) is matched to the new Zilog Z8000 and Motorola 68000 microprocessors, opposite to the convention used by the Intel 8086 or the familiar DEC PDP-11. The address bus was expanded by assigning formerly undefined lines. A few lines of the original bus which were of marginal utility have been reassigned, but most old boards will continue to work in the new system. A few boards may require minor patching, some will continue to be unreliable in the new system, and some will not work at all. However, for the most part the boards which will not work in the new system are those which have been having compatibility problems in the old.

An early draft of the new standard was published in the IEEE Computer Society magazine, Computer, in May 1978. A great deal of feedback from the industry was received and considered, and a new draft was published in the July 1979 issue of Computer magazine. The new draft differs in many respects from the previous one, but should be quite close to the final standard. Feedback received to date has emphasized the byte ordering problems and compatibility problems with pin assignments, especially the grounding of pin 53. A few pin assignments will probably change in order to move that ground to pin 55 before the final version is submitted to the IEEE Standards Board late this year.

The expanded bus with new DMA mechanism and greater reliability should provide a good base for the next generations of microprocessors, and strengthen the position of the S-100 bus as one of the most widely used in the hobby, small business, and industrial application areas. Many manufacturers are working with the draft standard already, so that several products have already benefited from the clarified definition of the bus. The next wave of new products should work much better than in the past.

For further information, contact George Morrow, Chairman, S-100 Committee, Thinker Toys, 5221 Central, Richmond, CA 94804; (415) 524-2101, or Howard Fullmer, Co-chairman, S-100 Committee, Parasitic Engineering, 5208 Miles Ave., Oakland, CA 94618; (415) 527-6133.

THE "MULTIBUS" PROJECT
(IEEE Task No. P796)

The Multibus is Intel's development system bus, with compatible boards available from many other manufacturers as well. The standard is basically a clearer public specification of that bus, with support from Intel and other manufacturers and feedback from the user community.

The original Multibus has been expanded from 16 to 20 address lines, from 8 to 16 data lines (with a mechanism for allowing mixtures of 8- and 16-bit devices to coexist on the bus), and from 8 to 12 I/O address lines. The number of vectored interrupts has been expanded, and timings and usages have been clarified. The number of address lines and the addressing of bytes within words (the most significant byte has the higher or odd address) are matched to the 8086 microprocessor.

The name "Multibus" is to be replaced by the IEEE number in the eventual standard. A synopsis of the proposed standard will soon be published in Computer magazine. Submission of the standard for Standards Board approval is expected late this year.

For further information, contact Rich Boberg, Chairman, "Multibus" Committee, Microbar Systems Inc., 1120 San Antonio Rd., Palo Alto, CA 94303; (415) 964-2862.

THE FUTUREBUS PROJECT
(IEEE Task No. P696.4)

This project has identified several areas in which new standards will be needed in the near future. Two new projects, the Backplane Bus project and the Local Network project have been established as a result of this work.

Current work is directed toward the needs of the home of the future: a home control and communications bus for unifying intercom, telephone, burglar detection, lighting and heating control, audio and possibly video systems; power-line signalling for control and status purposes; remote appliance control.

Other organizations are also beginning to address these problems. For example, a Home Bus Standards Association has been formed in Washington, D. C. This project will seek to cooperate with and help coordinate other efforts as it becomes aware of them.

For further information, write S. Cash Olsen, Chairman, Futurebus Committee, Signetics Corporation MS 026, 811 E. Arques Avenue, Sunnyvale, CA 94086; (408) 746-1557.

THE BACKPLANE BUS PROJECT
(IEEE Task No. P896)

This project is working on parallel backplane buses. A tentative goal is to design a fast 32-bit bus which has 16-bit and 8-bit subsets. In addition, the subset buses should be able to use smaller circuit boards, which are perhaps half the size needed for the full 32-bit system. The hope is that simple boards can be small and inexpensive and still be usable within a larger system which has more complex and larger boards.

The new 16- and 32-bit development system buses are being examined, as is the Department of Energy's multiple-segment FASTBUS.

For further information, contact Andrew Allison, Chairman, Backplane Bus Committee, Mini/Microcomputer Technology and Marketing Consultant, 27360 Natoma Road, Los Altos Hills, CA 94022; (415) 941-6065.

THE LOCAL NETWORKS PROJECT
(IEEE Task No. to be assigned)

This project is working toward a standard for local networks which are likely to be found in the office, laboratory, computer center and factory of the future. A likely candidate for standardization is the Xerox Ethernet. Work on this new project is just beginning.

For further information, contact Maris Graube, Chairman, Local Networks Committee, Tektronix, P. O. Box 500 MS 50-454, Beaverton, OR 97077; (503) 644-0161 x6234.

THE FLOATING POINT PROJECT
(IEEE Task No. P754)

The Floating Point project arose from the recognition that floating point processor chips were going to become available from a variety of sources, and that agreement on a standard floating point format could facilitate the combination of such chips into systems. Even peripheral devices, such as digital voltmeters, can be envisioned using a floating point format if a standard exists.

However, it soon became apparent that the choice of format is not unrelated to the mathematical properties of the floating point arithmetic, and so experts in that field joined in. At that point, even though this is nominally a committee addressing microcomputer problems, minicomputer and even large mainframe manufacturers became involved because they realized that the existence of a really good standard could impact their products' futures.

A draft standard has been written which defines floating point formats for single (32-bit) and double (64-bit) precision. The draft uses a biased exponent, signed magnitude arithmetic, and a hidden bit. (The redundant leading bit in a normalized significand is suppressed. The significand lies between 1 and 2 in the chosen format, so the remaining bits display the fraction.) It also uses gradual underflow, so that a number which becomes too small for the exponent range available continues to be represented (as a special unnormalized number), and has special numbers such as infinity which propagate correctly in subsequent calculations. The double precision format includes a larger exponent range than the single as well as a longer fraction. Other proposals for the handling of infinities and near-zeroes are still being considered. While gradual underflow does not eliminate underflow error, it reduces it to the same magnitude as roundoff error. An important consideration in the design has been the inclusion of features which support interval arithmetic, which provides the ultimate in protection by giving the user guaranteed upper and lower bounds on the true answer.

The committee has not yet addressed the problem of standardizing the order of transmission of fragments of floating point numbers within or between systems which cannot perform the transfer as a single full-width parallel operation. Since no existing or imminent microprocessors are capable of such wide transfers, this problem will have to be dealt with soon, if the full potential of standard hardware is to be realized. Comments on this problem are solicited.

The guiding principle has been the provision of mechanisms to protect the user from hidden erroneous results, and the generation of useful answers where at all possible. For some time, the debates have continued largely on technical grounds. Now that a fairly complete draft exists, however, the realities of the marketplace must be considered. If the standard is supported by some major manufacturers, it is much more likely to become widely used. The single precision format is very similar to the format used in DEC's PDP-11 family. DEC would be more likely to implement the arithmetic changes needed for the rest of the standard if the format were made exactly like theirs. Meanwhile, Intel and several other manufacturers are believed to be developing chips for the microcomputer industry (to which the standard was originally addressed) which implement the draft standard as is.

It is too soon to tell what compromises will be required for eventual acceptance of the standard, but an important vote on the question of gradual underflow appeared to show block voting, with the mini manufacturer employees solidly opposed (no mini now has gradual underflow arithmetic), chip manufacturers divided, and representatives of the numerical analysis user community solidly in favor. The resulting vote of 20 for vs. 12 against fell short of the 2/3 majority required for the adoption of gradual underflow.

One possible outcome would be that no standard will result from the committee's work officially, mini manufacturers will go on as they are, and chip manufacturers will produce floating point processors to the draft standard as is. Eventually this would probably result in a de facto standard. Another possibility is that the draft may be compromised in ways which do not seriously degrade its performance, and be supported as a standard by mini and micro manufacturers. It is unlikely that the committee would approve any changes which would significantly degrade the mathematical performance of the standard, as the battles between speed and rigor have always been won by rigor in this committee in the past, a phenomenon which could never have occurred before the advent of large scale integration.

The draft supported by the majority of the committee is to be published soon in Computer magazine, along with a summary of the objections of the minority. Integrated circuit manufacturers have already announced and delivered devices which implement the new format of the draft standard, but not all the other features.

For further information, contact Richard Delp, Chairman, Floating Point Standard Committee, Four-Phase Systems, MS 22-1D2, 10700 N. De Anza Blvd., Cupertino, CA 95014; (408) 255-0900 x4036.

THE ASSEMBLY LANGUAGE MNEMONICS PROJECT
(IEEE Task No. P694)

This is a project which arose from the annoying petty difficulties faced by a system implementer when he must switch often from one microcomputer system to another. Petty differences in the assembly language instruction mnemonics, such as LOD versus MOV, cause wasted time and effort correcting mistakes which never should have happened. More subtle are problems such as reversed sequence of operands from one machine to another. This project has resulted in a draft standard specification for assembler language mnemonics and operand conventions which can be used as a guide by the assembler implementer when he is faced with arbitrary design decisions.

Though manufacturers will probably continue to demonstrate their creativity in mnemonic generation (at least one manufacturer actually copyrighted individual mnemonics!), most assemblers are written by software support houses, which may be more willing to produce tools which make the user's job easier and less concerned with locking him into a particular product line.

This draft standard will be published this fall in Computer magazine, with several microprocessor instruction sets included as examples in appendices.

For further information, contact Wayne P. Fischer, Chairman, Assembler Language Mnemonics Committee, Kylex Corporation, 82 Shereen Place, Campbell, CA 95008; (415)-969-5200 or (408) 374-5405.

THE HIGH LEVEL LANGUAGES PROJECT
(IEEE Task No. P755)

This committee has been working on extending high level languages for use in the microcomputer environment. The goal is to provide the features needed for applications where programs must be able to refer to explicit address locations and hardware features, and yet retain the simplicity and clarity achieved by programming in a high-level language. Support for interrupts, concurrent processes, and multiple processors is also needed. In addition, the execution location of generated code must be under user control.

The minimum level of support needed is the ability to pass information and control between the high-level language and assembler language subroutines. Some committee members wish to go beyond this to add new statements to the high-level language, but others wish to make the minimum required changes to existing languages. There is also a wide range of opinion about the suitability of various high-level languages for these applications, with some of the least suitable ones being the most widely used. One obvious candidate is PASCAL, which spawned the project described below. However, in view of the widespread use of FORTRAN and BASIC, extensions to them will be considered as well. Considerable work has been done by other groups on real-time and other related extensions to these languages, and the work of this committee will have to be integrated with existing standards.

For further information, contact Richard Karpinski, Chairman, High-level Languages Committee, 6521 Raymond Street, Oakland, CA 94609; (415) 666-4529.

THE PASCAL PROJECT
(IEEE Task No. P770)

A high priority project has been the standardization of PASCAL. Though PASCAL is relatively uncorrupted by variants compared to other languages, due to a fairly complete specification by Jensen and Wirth in the PASCAL User Manual and Report published by Springer Verlag, certain ambiguities in the specification have been discovered which need resolution. The current effort is to cooperate with the International Standards Organization and ANSI's X3J9 in evaluation of a draft standard prepared by a British Standards Institution committee. This should be completed in a few months, allowing further efforts to be applied to the subject of extensions to PASCAL.

Most industrial users of PASCAL agree that certain extensions to the language are needed to allow independent compilation of modules, linking with assembler language modules, control of memory usage, mechanisms which allow handling of I/O through ports or memory mapping, and variable dimensioning of arrays.

However, there is little agreement as to how many and which of these features are really needed, and each implementer chooses his own as he sees fit. Making these changes to the language in a way which preserves the ability of the compiler to detect errors whenever possible and in a way which does not disturb the philosophy of the base language is not easy. The committee will have a difficult job choosing a suitable set of extensions for standardization. Several other efforts are already under way, and this committee will cooperate with them.

For further information, contact Bruce Ravenel, Chairman, PASCAL Committee, Language Resources, 1307 South Mary Avenue, Sunnyvale, CA 94087; (408) 737-2525 or (415) 928-8086.

THE RELOCATABLE OBJECT FORMAT PROJECT
(IEEE Task No. P695)

This project again arose out of the frustrating problems which the typical user of multiple software and hardware systems faces. If one uses one system configuration from one vendor, the problems are minimal. But the typical designer today jumps from one system to another with different memory or I/O configurations and often finds that the software tools he wants to use are not easily applied to the system he is currently working on. Part of this problem is due to the lack of a standard format for relocatable object modules. In fact, many systems in common use today have no relocatable object mechanism at all! A primitive relocation mechanism is essential in systems which support libraries of object modules or which allow combining of modules written in different languages, such as FORTRAN and Assembler language.

Unfortunately, manufacturers derive some benefit from the current situation, which makes it difficult for their captive customers to start using products from another manufacturer. Therefore, cooperation from industry has been very minimal, with the better relocatable object formats being regarded as proprietary or secret. In the face of this opposition to standardization, the committee has been largely stymied and there has been little useful progress to date, though recently some software suppliers have expressed a willingness to cooperate in the formation of a new standard.

Volunteers are needed to help in this work, which is a much bigger task than it might at first appear. Furthermore, a great deal of supporting software is needed before such a standard would be useful.

A recent development is the committee's discovery of a machine independent relocatable object format, CUFOM, devised at CERN, the European Nuclear Research Center in Geneva. This format is used by a large family of cross assemblers for various hosts and microcomputers connected in a large network. Most of the software is written in a manner which makes it easy to transport from one machine to another, so it might make a suitable base for standardization. The object code is mostly stored in hexadecimal character form, which is convenient for human inspection and data transfer, but is rather inefficient in its use of file storage. Further study will be needed.

For further information, contact Tom Pittman, Chairman, Relocatable Object Format Committee, Itty Bitty Computers, P. O. Box 23189, San Jose, CA 95153; (408) 578-4944.

SUMMARY

The IEEE Computer Society Computer Standards Committee and the Microprocessor Standards Committee and their subcommittees have made significant progress on several fronts, with the likelihood of more to follow. Some of the standards which will result from this work are likely to have a significant and lasting beneficial effect on the computer industry.