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FAST SYNCHRONOUS GRAY COUNTER*

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Gray counters are used when the unit-distance property of the Gray code is required. For example, if a binary quantity has to be latched "on the fly," i.e., while a counter is changing states, it would be hazardous to use a natural binary coded counter. Consider the hazards in changing from natural binary $15_{10} = 01111_2$ to $16_{10} = 10000_2$. If, for example, the most significant bit (msb) should arrive at the latch somewhat earlier than the lesser significant bits, the latched quantity could become $11111_2 = 31_{10}$. Thus, a large error may be introduced using the natural binary code. The Gray code however, being a unit-distance, non-weighted code, does not exhibit the above hazards: in a unit-distance code adjacent coded numbers differ in <u>one</u> bit only; thus, in Gray code 15_{10} = 01000 while 16_{10} = 11000. Latching "on the fly" either code results in an error not greater than 1 lsb. When the highest frequencies of operation are required there is more incentive for using Gray code synchronous counters, since latching "on the fly" becomes more difficult at these higher frequencies.

Surprisingly, a literature search did not reveal a synchronous Gray counter that could be operated at the highest possible frequencies. A classical design procedure, using T FFs and their excitation tables yielded the following (for a 4-bit Gray counter):

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$$T_0 = \overline{Q_3 \oplus Q_2 \oplus Q_1 \oplus Q_0}$$

$$T_1 = Q_0 \, (Q_3 \oplus Q_2 \oplus Q_1)$$

$$T_2 = Q_1\overline{Q}_0 \, \overline{(Q_3 \oplus Q_2)}$$

$$T_3 = \overline{Q}_1\overline{Q}_0 \, (Q_3 \oplus Q_2)$$

The above expressions show the high frequency limitations of this approach due to (a) the extensive gating required and the resultant propagation delays at the T-inputs, and (b) the extensive loading at the Q_i terminals which becomes more pronounced as the number of bits in the Gray counter increases.

A simple solution for the problem was found by deriving the Gray code from a synchronous natural binary counter. The truth tables of the natural binary code and the Gray code are given in Table 1. Note that for each logic transition from 0 to 1 in the i-th bit of the binary code there is a change of state in the corresponding i-th bit of the Gray code. The same information is contained in the waveforms shown in Fig. 1 in which the binary code appears dashed and the Gray code in full lines. Observe that the i-th bit of the Gray code is half the frequency of the corresponding i-th bith of the natural binary code.

The implementation of an 8-bit Gray counter is shown in Fig. 2. The natural binary counter consists of two ECL ICs type 10016 with a typical count frequency of 200 MHz. The delay, $\tau d < 1/2f$ (f = operating frequency) is required for the 180° phase shift between B_0 and B_1 as shown in Fig. 1. The Gray code is obtained at the outputs of the FFs type 10231 having a typical toggle frequency of 225 MHz.

Table 1

THE NATURAL BINARY AND GRAY CODES

Decimal	Gray G_4	G_3	G_2	G_1	G_0	Natural Binary B_4	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	1
2	0	0	0	1	1	0	0	0	1	0
3	0	0	0	1	0	0	0	0	1	1
4	0	0	1	1	0	0	0	1	0	0
5	0	0	1	1	1	0	0	1	0	1
6	0	0	1	0	1	0	0	1	1	0
7	0	0	1	0	0	0	0	1	1	1
8	0	1	1	0	0	0	1	0	0	0
9	0	1	1	0	1	0	1	0	0	1
10	0	1	1	1	1	0	1	0	1	0
11	0	1	1	1	0	0	1	0	1	1
12	0	1	0	1	0	0	1	1	0	0
13	0	1	0	1	1	0	1	1	0	1
14	0	1	0	0	1	0	1	1	1	0
15	0	1	0	0	0	0	1	1	1	1
16	1	1	0	0	0	1	0	0	0	0

A 125 MHz Gray code counter was constructed and operated satisfactorily. Using the Fairchild 100K series natural binary counter type F100136 and FFs type F100131 it should be possible to implement Gray counters operating up to 450 MHz.

Thanks are due to Anthony Tilghman for constructing and testing the curcuit.

Figure Captions

Fig.1 Waveforms

---- Natural binary code

—— Gray code

Fig.2 Synchronous Gray Counter.

Logic diagram

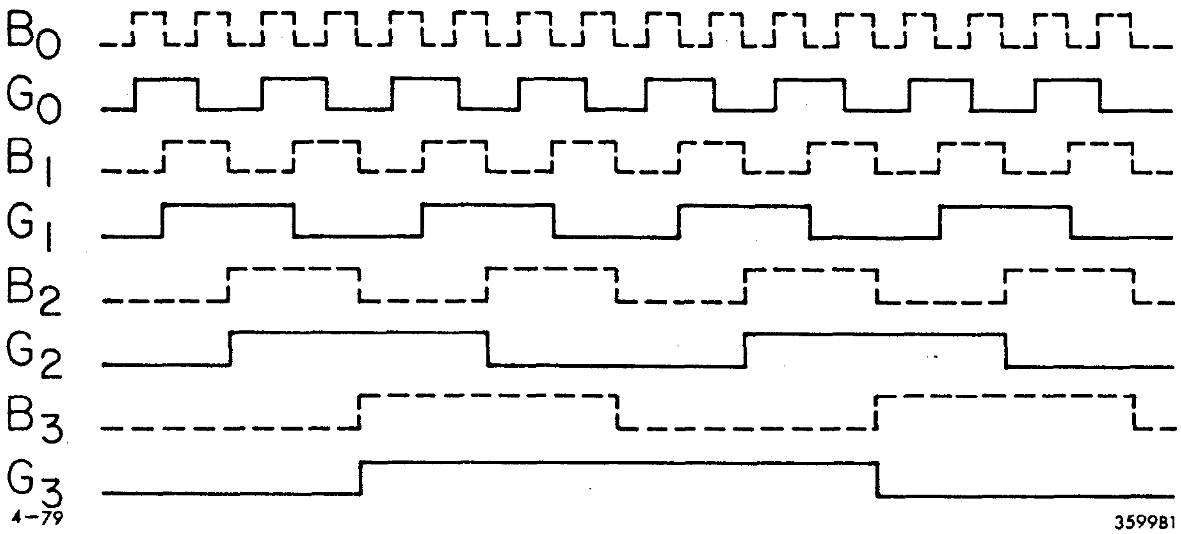
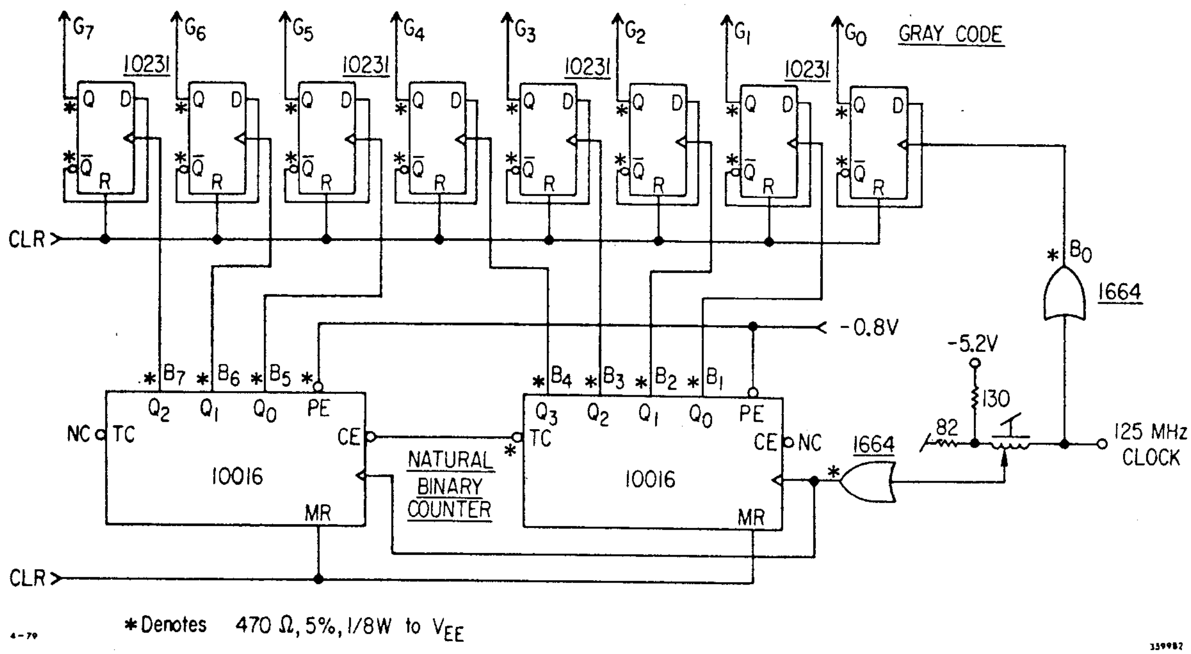


Fig. 1



G7
G6
G5
G4
G3
G2
G1
G0
GRAY CODE
10231
10231
10231
10231
Q
D
Q
R
CLR
B7
B6
B5
B4
B3
B2
B1
B0
1664
-0.8V
-5.2V
130
82
Q2
Q1
Q0
PE
Q3
NC
TC
CE
10016
10016
MR
NATURAL
BINARY
COUNTER
1664
125 MHz
CLOCK
CLR
4-79
*Denotes 470 Ω, 5%, 1/8W to VEE
359982

Fig. 2