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(I)

TRACK CORRELATOR AS A FAST TRIGGER IN THE DETECTION OF π-μ COULOMB BOUND STATES*

Dan I. Porat and Dale A. Ouimette†

Summary

The circuit generates a fast ($\approx$200 ns) trigger in response to two particles (one π and one μ) passing through two scintillation hodoscopes and satisfying criteria of direction and spatial separation. The selection of 4-fold coincidences identifying the relevant tracks is effected by simultaneous RAMs[1] in coincidence with SSI logic.

Introduction

In an experiment for the detection of π-μ Coulomb bound states[2], it is required to select rare events of π-μ atoms in the presence of a high background of γ-rays and highly energetic pions and muons. A thin aluminum foil in the path of the π-μ atoms (see Fig. 1) dissociates the π and μ making their detection possible. The uncoupled pion and muon emerge from the foil with the same velocity, an almost perfect spatial coincidence, and an angle of a few milliradians. These properties greatly facilitate the design of a relatively simple pattern-recognition circuit.

The coincident particles are passed through two equal and opposite magnets to first separate them spatially and then deflect them to almost parallel paths. After traversing a 5-plane MWPC the particles pass through two scintiallation hodoscopes of 24-counters each (see Fig. 1). The specification for spatially coincident tracks that give a signature of the dissociated π-μ atoms are as follows (see Fig. 2):

1. Tracks of the type I_A must be in coincidence with tracks II_A (skewed) or II_B (parallel), but not with II_C.
2. Tracks of the type I_B may be in coincidence with tracks II_A (skewed in one direction), tracks II_B (parallel), or tracks II_C (skewed in the opposite direction from II_A).

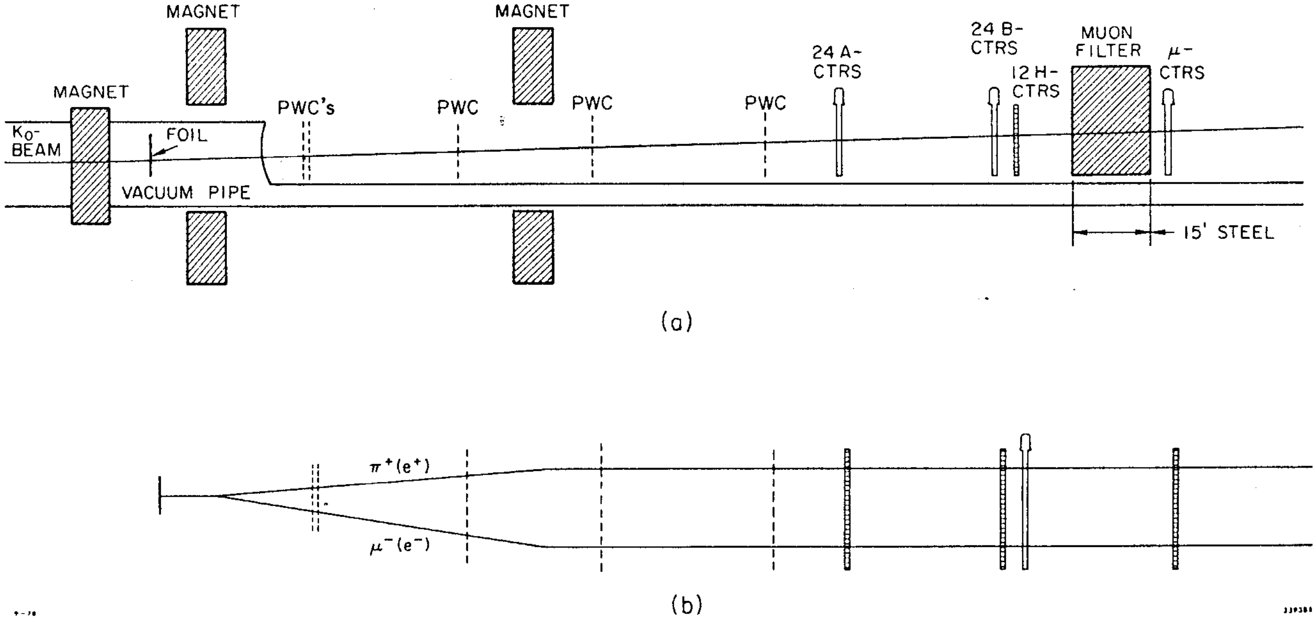

Fig. 1. (a) Experimental arrangement, elevation; (b) π-μ path, plan view.

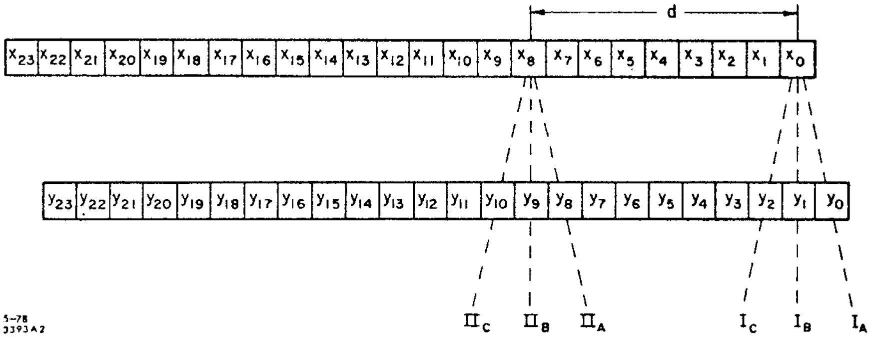

Fig. 2. Definition of combinable track types.

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[†] Stanford Linear Accelerator Center, Stanford University, Stanford, California 94305

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3. Tracks of the type I_C must be in coincidence with tracks II_B (skewed) or II_C (parallel), but not with II_A.

4. In addition to conditions 1 through 3, the separation, d, between tracks of type I and type II, must satisfy $2 \leq d \leq 15$, where d refers to the individual scintillation counters.

In short, the two tracks contributing to the fast trigger must meet certain critera of spatial separation and near parallelism. The Boolean equations for the 4-fold coincidences involving a track passing, for example, through x_0 and y_0 are:

$$I_A(II_A+II_B) = x_0y_0(x_2y_2+x_2y_3+x_3y_3+x_3y_4+\dots + x_{15}y_{15} + x_{15}y_{16}) \qquad (1)$$

where the parentheses contain 28 double coincidence terms. For a track passing, for example, through x_0 and y_1 the expression is:

$$I_B(II_A+II_B+II_C) = x_0y_1(x_2y_2+x_2y_3+x_2y_4+\dots + x_{15}y_{15} + x_{15}y_{16} + x_{15}y_{17}) \qquad (2)$$

where the parentheses contain 42 double coincidence terms. Finally for a track passing, for example, through x_0 and y_2 the expression is:

$$I_C(II_B+II_C) = x_0y_2(x_2y_3+x_2y_4+x_3y_4+x_3y_5+\dots + x_{15}y_{16} + x_{15}y_{17}) \qquad (3)$$

where the parentheses again contain 28 double coincidence terms.

Of course, as the index of each track of type I increases by one, so do the indices for the corresponding tracks of type II. It is evident that the terms in parentheses of equation (2) are the Boolean sum of the terms in parentheses of equations (1) and (3).

$$I_B(II_A+II_B+II_C) = I_B(II_A+II_B) + I_B(II_B+II_C) \qquad (4)$$

This recognition saves a considerable amount of hardware. Moreover, the terms in parentheses can be implemented by programmable logic arrays (PLAs), or better yet by simulataneous RAMs (s-RAMs) of the kind described in reference 1. In short, the s-RAM performs the function of a PLA since the address of the s-RAM is not decoded. It accepts 16 x-variables and 16 y-variables and can generate a maximum of 256 double-coincidence terms. These are combined in a common OR circuit to yield just one output. It differs from the PLA mainly in that it has a bistable element at each x_iy_j intersection that can be set or cleared via appropriate control circuitry, or from a computer.

Thus far we have dealt with tracks x_0y_0, x_0y_1, and x_0y_2 and their corresponding tracks of type II. Similar expressions apply to tracks x_1y_1, x_1y_2, $x_1y_2 \dots x_{21}y_{22}$. In fact, by careful ordering of the signals from counters x_iy_j we can program all s-RAMs identically, saving a considerable amount of hardware and software.

System Implementation

Implementation of the system that recognizes close to 1400 valid track pairs is shown in the block diagram of Fig. 3. Central to the system are 20 printed circuit boards, each containing an s-RAM, 2-line to 1-line multiplexers and some SSI gates (see Fig. 4). Each board processes a set of type I (I_A, I_B, I_C) tracks and their associated type II tracks. All boards containing the s-RAMs are programmed simultaneously via a direct access to a PDP-11/40 UNIBUS. A LOAD program incorporating a look-up table facilitates the programming.

The circuit, after programming, is ready to accept signals from the scintillation hodoscopes. The inputs to the x-terminals of s-RAM numbered 0 are derived from x-counters x_2 through x_{15} in accordance with equations (1) through (3). Similarly the inputs to the y-terminals of the s-RAM numbered 0 are derived from y-counters

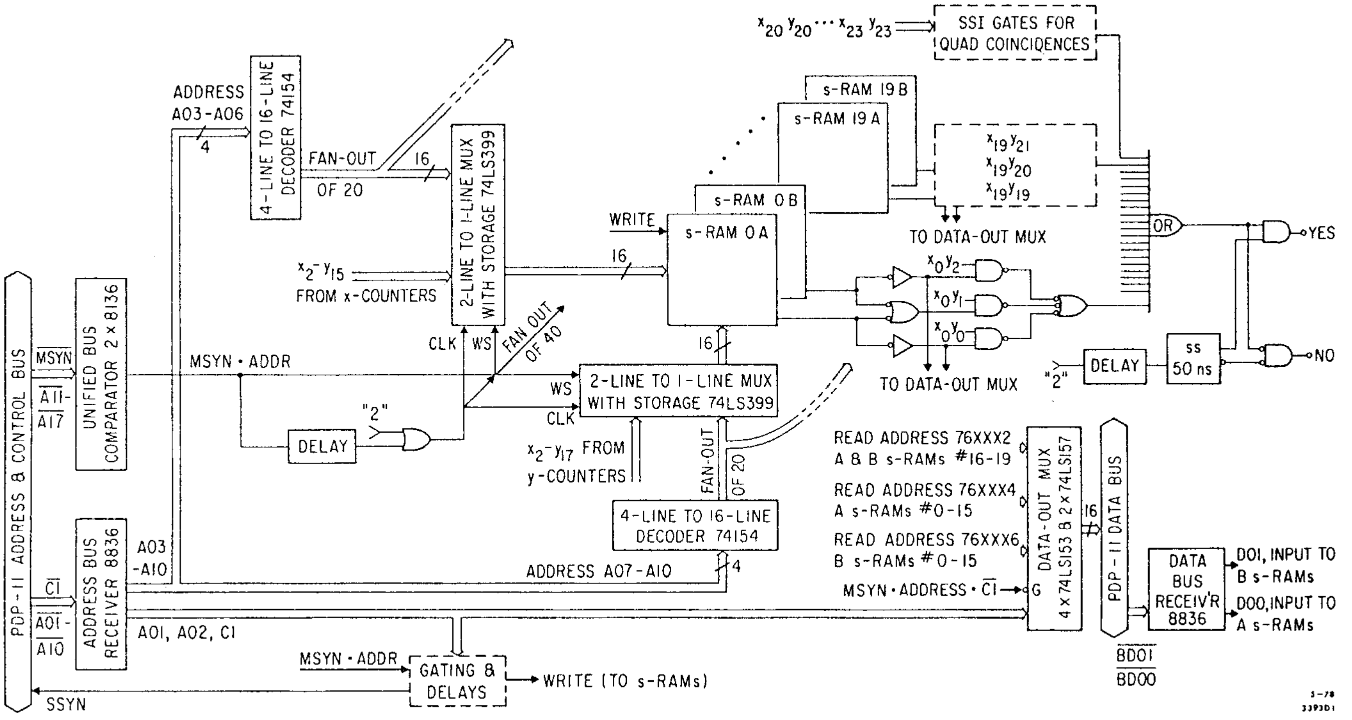

Fig. 3. Block diagram of track correlator

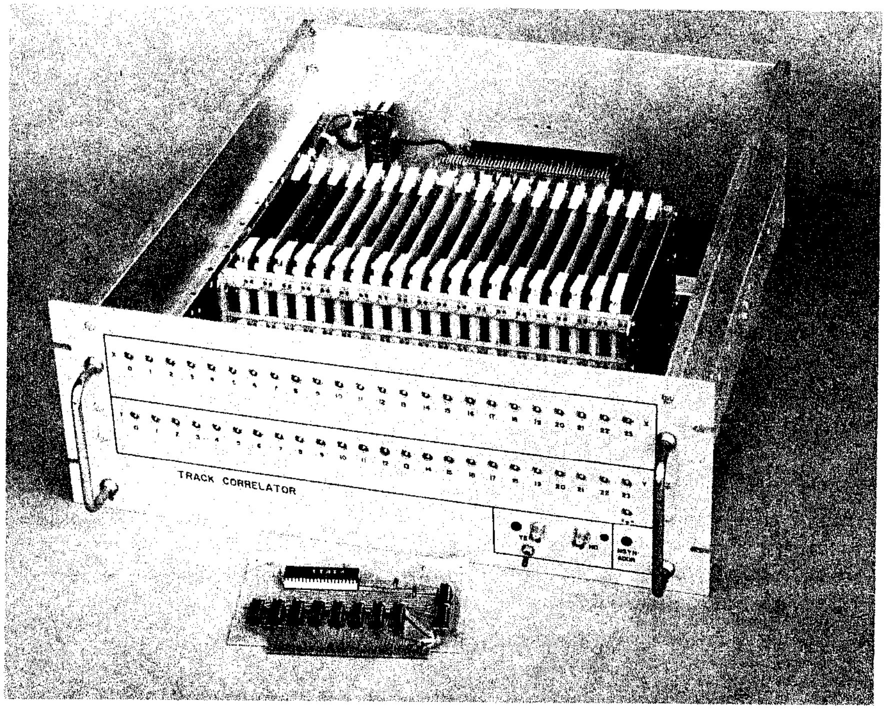

Fig. 4. Top view of track correlator

y_2 through y_{17}. The subscripts of x and y increase by one for each further s-RAM. In this way all possible combinations of specified tracks are covered. Some type I tracks (see Fig. 2) at the high end of the counter hodoscopes (tracks $x_{20}y_{20}$ etc.) have an insufficient number of combinations with type II tracks to warrant the use of s-RAMs and multiplexers. Thus nine 4-fold coincidences are implemented with SSI gates. Each of the two outputs of an s-RAM representing the terms in parentheses of equations (1) and (3) is gated with an external double-coincidence term. The terms in parentheses of equation (2) are realized by ORing the two outputs of an s-RAM. Finally, all such gated outputs together with the SSI terms described previously are ORed and gated out to two outputs. A valid combination of tracks results in a YES output. Otherwise a NO output is generated which aborts the event. The fast trigger is determined by the coincidence

$$\text{Fast Trigger} = 2A\cdot 2B\cdot 1H\cdot(\text{Track Correlator "YES"})$$

where A, B, and H are the scintillation counters shown in Fig. 1. The inclusion of the track correlator in the fast trigger reduced the rate of unwanted triggers in the experiment by 90 percent.

Software for System Checkout

Because of the difficulty in locating system faults by statistical analysis of the events taken, the following software was considered essential for system reliability: after the LOAD program loads the desired track recognition pattern it initiates a read cycle and compares the outputs of the s-RAMs with the original look-up table. Most system faults are thus easily located.

However, because the diagnostic portion of this program is limited to only checking the pattern in the s-RAMs, a more complete TEST program was developed that dynamically checks the complete system. By connecting the 48 inputs of the track correlator to output registers which are directly addressed via the UNIBUS, the TEST program simulates all the possible track pair inputs. As each track pair is generated the YES or NO outputs are monitored via an external TEST circuit (also on the UNIBUS). These outputs are checked against the algorithm for valid track pairs described previously. Hence the entire system is quickly tested in a simulated event fashion.

Acknowledgments

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References

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