

**"FASTBUS" - STATUS OF DEVELOPMENT OF A STANDARD
HIGH SPEED DATA ACQUISITION BUS
FOR HIGH ENERGY PHYSICS*†**

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ABSTRACT

In late 1975 the US NIM Committee initiated a study group, known as the Advanced System Study Group, to review the future data acquisition modular interface requirements for high energy physics. The final report¹ of this group recommended the development of a new standard system, now known as "FAST-BUS," which would have as principal features improved speed by a factor of 10 over CAMAC; more generalized architecture to accommodate distributed parallel processing and fast pre-processing; special scan modes of particular use in high energy particle detection systems; and standardized bus structures and mechanics.

This paper is a brief summary of current activity.

Introduction

In response to a request from members of the High Energy Physics community, the US NIM Committee, in late 1975, organized a special study group known as the Advanced System Study Group (ASSG), to review the future needs of the community in the area of data acquisition standards. The final report¹ of the ASSG concluded that the existing standard in wide use in the community, CAMAC, would not meet the future needs in physics, and recommended that a new standard be developed. The new standard has recently been dubbed "FASTBUS."

Subsequently, the ASSG was dissolved and a new inter-laboratory group established to undertake the development program. The new organization for this program is shown in Fig. 1; the current list of participants, representing hardware, software and physics specialists, is shown in Appendix A. At the same time, a formal joint funding proposal by five of the major laboratories² was made to ERDA requesting special funding to enable completion of the program within two years. The program envisages simultaneous development work at these laboratories as well as other centers, and completion implies the development of vendor-supported production hardware.

General Goals

The organization shown in Fig. 1 has been structured to ensure an adequately broad representation of hardware engineers, software specialists and users, in order to define goals and produce results which are optimized for the physics user community. At the same time it is recognized that if, at little or no additional cost, greater generality can be achieved in order to better serve a broader community (especially the broader ERDA community), then somewhat expanded goals may be desirable.

The general technical goal is to develop a standard with greatly improved features which will successfully meet the needs of users as well as gain the support of the manufacturing community. The latter implies that standard hardware must be developed, which of course does not preclude the compatibility of the system with other systems, including custom designs.

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‡ Chairman, Fast System Design Group, US NIM Committee.

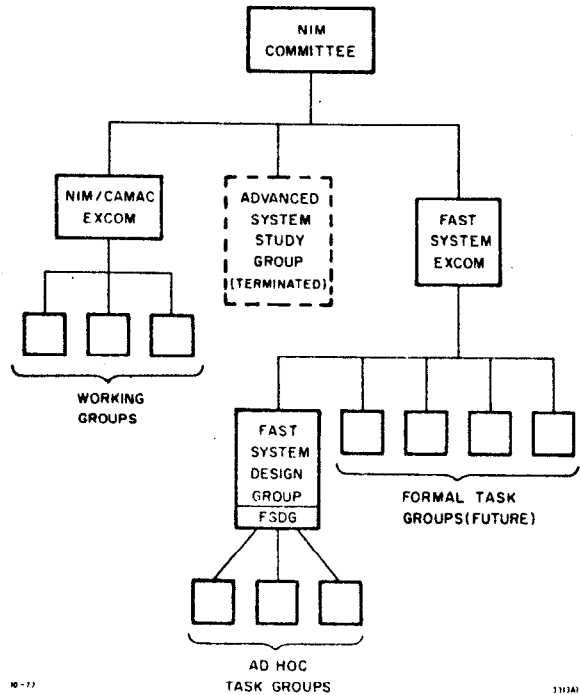


Fig. 1 Organization Fast System Development

Specific Goals

Reference 1 contains much background information including examples of types of systems which require improved capabilities. The major technical features required are as follows:

Modularity

The modularity at the sub-system level, as exemplified by CAMAC, needs to be retained. This implies the design of a standard module, enclosure or enclosures, etc. Modularity is also needed at the system level--that is, it should be easy to connect sub-systems together via more or less transparent interfaces.

Data Transfer Speed

A major goal is to design a system which can support data transfer speeds at the sub-system level of ≤ 100 nsec, i. e., ten times faster than present CAMAC. This means physical structures which will support high speed devices such as ECL, and transfer modes designed for the optimum in speed wherever possible.

Wide Address/Data Fields

With the trend toward more bandwidth and wider data fields in minicomputers, as well as in peripheral storage devices and modules, a 32 bit maximum data field and a 28 bit address field is desired. Subsets of both should be possible where warranted by the application, but the basic hardware bus or backplane should be able to support the maximum implementation.

Multiple and Parallel Processors

One of the chief shortcomings of CAMAC for future needs is its basic architecture: module positions in the crate are privileged, and the crate and branch structures are quite different. This makes the connection of multiple processors which must communicate with one another, or with other parts of the system, extremely difficult. This argues strongly for an architecture which removes these constraints, and promotes transparency between system and sub-system level buses or structures.

Sparse Data Scan Mode

A special problem in physics data acquisition is to collect data from a relatively small number of channels within a much larger array. Since the hardware dead-time is potentially a limiting factor in large systems, it is imperative to support data collection modes which will minimize the time taken to scan all channels. It is desired to design one or more such modes into the basic structure of the bus.

High Speed Block Transfer

It is important to be able to transmit blocks of data, either short or long, at high speed between nodes of the system. This is especially important in data pre-processing where it is desired to examine the raw data in some fashion to determine whether it contains significant information. Thus, there is a need for transfers which can be made at the maximum speed of the bus, and minimum amount of control information exchanged for each transfer. The highest speed would be a nonhandshaked transfer, once the communication path is established via a master gaining control of the bus and addressing the receiving device.

Message-Oriented Communication Protocol

In a distributed processing system, it is important to have a powerful communications protocol to, in principle, allow any intelligent device in the system to communicate with any other device. In practical experimental physics systems, this degree of complete generality will rarely, if ever, be required; however, the basic system message structure should allow this in order to facilitate flexible (and somewhat unforeseeable) system topologies.

Minimum Number of Physical Lines

To minimize the hardware at the bus level, two basic changes from CAMAC are possible: multiplex the address and data lines, and multiplex the read and write lines at the subsystem level. Modern integrated circuit devices make this quite attractive from a device standpoint; in addition, the system bandwidth suffers very little in practice, because most high speed DMA transfers will involve blocks of words, which can be transferred at maximum rate once the extra cycle overhead is paid to initiate the transaction.

Error Detection

Error detection needs to be made at some level; correction is basically not a problem, because the loss of a small percentage of data due to transmission errors is totally insignificant. Checking algorithms should be implementable, primarily at the expense of speed and the additional local hardware and system software necessary to support them.

Flexible Power System and Mechanics

There is a concern that power requirements for future IC families could change, and it has been suggested that on-board power systems should be possible at the module level to minimize disruption that might be caused by such changes. This matter is under study. In any event, it must be possible to support a wide range of power requirements, hopefully in

a modular fashion.

Similarly, suggestions have been made that the mechanics of busses and connectors should be flexible enough to allow different sized clusters of modules, rather than a standard crate-full, if the system configuration would benefit. This matter is also under study.

Vendor Support

It is absolutely essential that logic, electrical and hardware standards be developed which are economically supportable by the manufacturing community. This primarily requires efficient and economical design, broad acceptance and support by the user community, and close liaison during specification and design with manufacturers.

A summary of the required technical goals is given in Table I.

Table I
Fast System Technical Goals

1. Modular system for flexibility.
2. Data transfer speed ≤ 100 nsec.
3. Nonprivileged module position.
4. System and subsystem transparent.
5. Wide address and data fields (28 and 32 bits max).
6. Support multiple masters (priority arbitration).
7. Support sparse data scan mode(s).
8. Support high speed block transfers (DMA).
9. Message-oriented communication protocol.
10. Minimum number physical lines (mux data/address).
11. Error detection capability.
12. Flexible power/mechanics.
13. Ability to accommodate technology improvements.
14. Vendor supportable.

Progress and Present Status

The newly constituted Fast System Design Group met for the first time in Edmonton, Alberta, Canada, in June 1977, and later in Boulder, Colorado (August 1977) and San Francisco (October 1977). Between general meetings, a number of task groups has been meeting to work on specific technical issues. In parallel with this activity, a specific funding request has been submitted to ERDA for support of the program; this request is still pending. Some of the technical points which have been adopted as working models are as follows:

Topology

The concept of bus building blocks as shown in Fig. 2 has been adopted as a working model. This depicts a segment which can be controlled by one or more local autonomous processors. The segment can be connected to other segments via a transparent segment interconnect (SI), or to a remote link via a link processor (LP).

An example of a multisegment system with interconnects is shown on Fig. 3. Note that topologically, the segment which collects all SI's can be identical to all other segments, i.e., transparent.

Fig. 4 shows an example where a single master can access a number of segments via a simplified segment buffer.

Special control or access paths can be created via

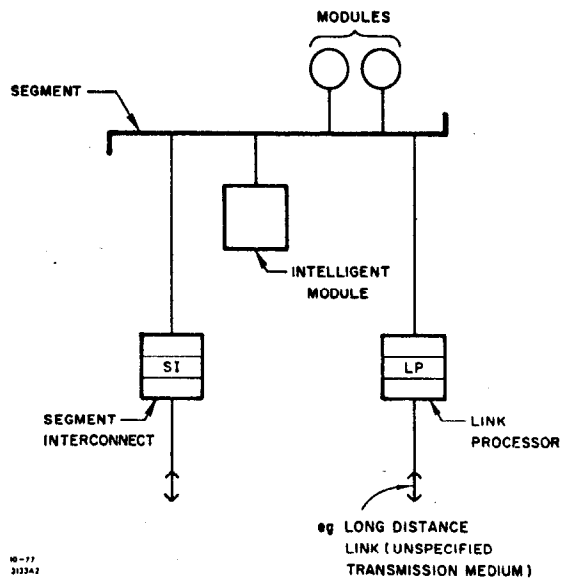


Fig. 2 Symbols

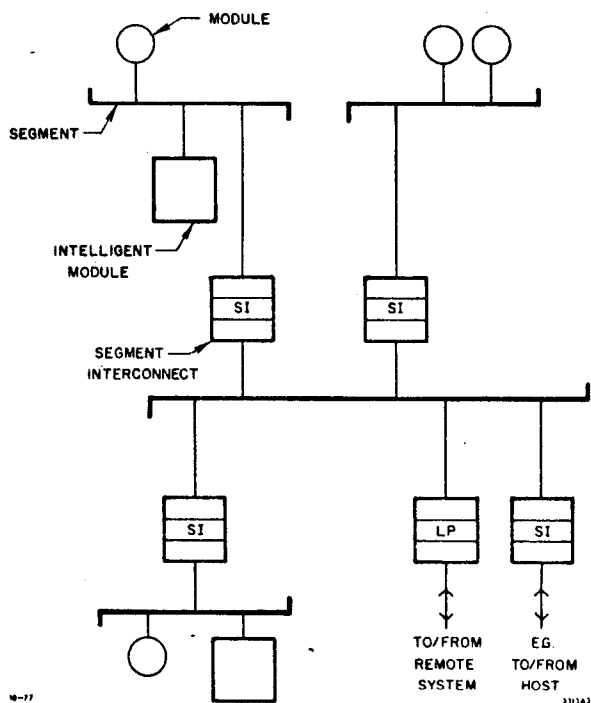


Fig. 3 Topology (Example)

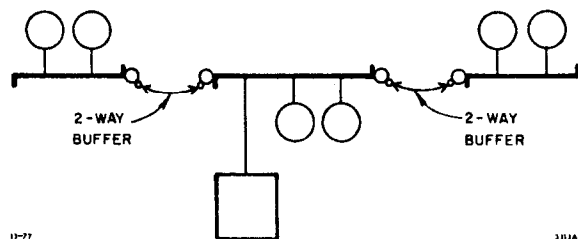
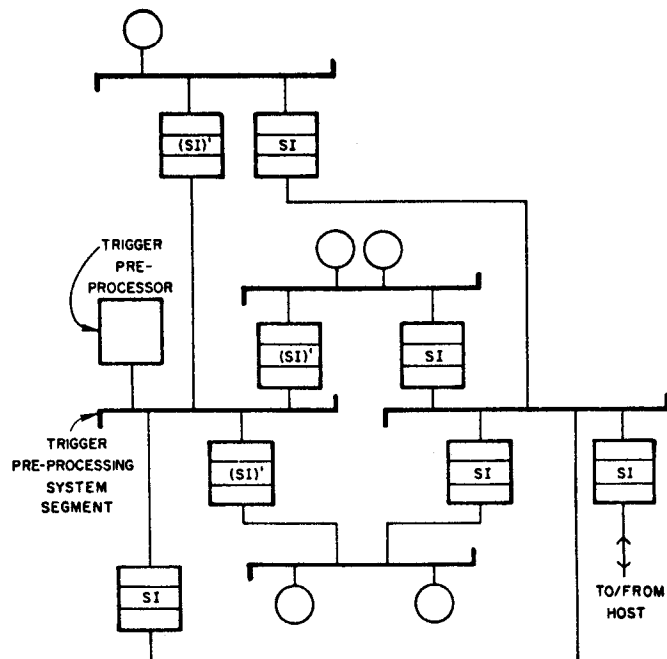


Fig. 4 Segment Buffer

more specialized SI's as shown in Fig. 5. This example incorporates a special segment for fast trigger processing, with special SI's to access the subset of data needed for the trigger decision.



SI = "REGULAR" SEGMENT INTERCONNECT
 (SI)' = SPECIAL FAST DEDICATED SI
 (FOR TRIGGER PRE-PROCESSING ONLY)

Fig. 5 Special Segment Example

Multiplexed Lines

The concept of multiplexed address and data lines has been adopted. The maximum number of data lines is 32 and of address lines, 28. To transmit a complete message, the address and function code are first transmitted, and then the data or command word. Thus, for single transactions, a double transmission cycle is required. However, for block transfers of data, once the data link between devices is established, data words can be transmitted in succession at maximum bus speed.

One possible bus implementation is given in Table II, where the line assignments are listed. A possible assignment of function codes is shown in Table III. Note that the number of special function lines has been minimized, both by multiplexing, and by the assumption that a "broadcast" command is available, which will allow up to 32 special control bits to simultaneously access all modules in the system.

Sparse Data Scan

The two basic methods under discussion involve either token passing, in which successive modules containing data intercept a control bit until their data are passed; or priority encoding, in which the addresses of the valid data words are raised in succession to the controller which is receiving the data. Both schemes essentially satisfy the requirements, and the pros and cons of the hardware implementation are being debated.

Multiple Masters

Various bus arbitration schemes are under discussion. One scheme involves a number of bus request lines by which mastership of the bus is granted on the basis of assignable priorities. Another scheme involves the concept of a (programmable) vector address for each master. In any case, it must be possible to request mastership of a second segment via one or more segment interconnects; in this case, the local master must have knowledge of and access to a global (system) address field, and the segment interconnect must contain the

Table II

Fastbus Signal Lines

<u>Name</u>	<u>Number</u>	<u>Function</u>
ADAL	32	SHARED ADDR. -FUNCT. /DATA LINES 1. (28) ADDRESS AND (4) FUNCT. LINES 2. (32) DATA LINES
BUS BUSY	1	INDICATES BUS MASTERSHIP AND OPERATION IN PROGRESS ON BUS
ADSYNC	1	ADDRESS SYNC: LEADING EDGE USED TO STROBE ADDR. /FUNCT. ASSERTED LEVEL USED FOR ADDRESS DECODING.
ADACK	1	ADDRESS ACKNOWLEDGE: INDICATES ADDRESS RECOGNIZED BY MODULE.
DASYNC	1	DATA SYNC: USED TO INDICATE ADAL CONTAINS DATA.
ACK	1	ACKNOWLEDGE: INDICATES DATA PRESENT ON OR HAS BEEN LOADED FROM ADAL.
NACK	1	NO ACKNOWLEDGE: INDICATES THAT OPERATION CAN NOT BE PERFORMED OR SUSPEND CURRENT ACTIVITY.
EOB	1	END OF BLOCK: INDICATES LAST WORD OF DMA TRANSFER.
PARITY	1	USED FOR PARITY OF BOTH THE ADDR. -FUNCT. AND THE DATA/EOB WORDS.
BUSREQ	8	USED FOR BUS ARBITRATION.
CLOCK	1	USED FOR BUS ARBITRATION.
GRN	1	GROUND
TOTAL	50	

Table III

Fastbus Function Codes

<u>Value</u>	<u>Function</u>
0000	SINGLE WORD READ
0001	DMA READ (WITH HANDSHAKE)
0010	DMA READ (WITHOUT HANDSHAKE)
0011	DMA READ TOKEN PASSING
0100	SINGLE WORD WRITE
0101	DMA WRITE (WITH HANDSHAKE)
0110	DMA WRITE (WITHOUT HANDSHAKE)
0111	DMA WRITE TOKEN PASSING
1000	BROADCAST
1001	NOT ASSIGNED
1010	NOT ASSIGNED
1011	RESUME DMA TRANSFER
1100	NOT ASSIGNED
1101	NOT ASSIGNED
1110	NOT ASSIGNED
1111	INTERRUPT

necessary logic to transmit the bus request to the next segment.

Timing

An example of a typical single-word transfer timing cycle is shown in Fig. 6. This example assumes ECL devices and typical propagation delays, and pulse widths which are consistent with the requirements of short printed circuit strip-line buses. Fig. 7 shows a timing cycle for a handshaked

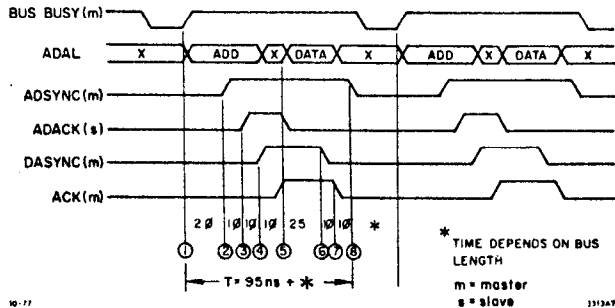


Fig. 6 Timing - Single Read Data Transfer

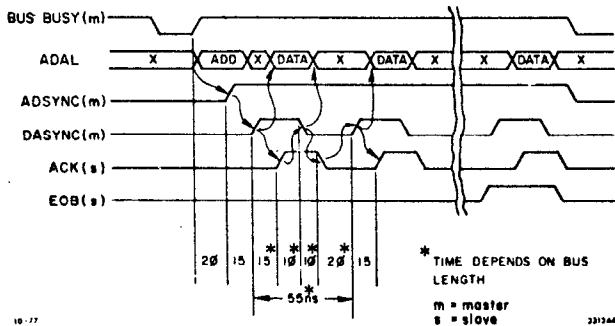


Fig. 7 Timing - DMA Read Transfer With Handshake

DMA transfer. It is clear that for performance in excess of 10 MHz transfer rates, ECL is probably mandatory. The characteristics of lines and associated problems of transmitting and receiving between many devices on a single segment are still being studied.

General

Much additional discussion has centered around the details of interrupts, error detection, power supplies, and mechanics, including connectors and ventilation. In general, ad hoc groups have been assigned to work on specific problem areas, in an attempt to arrive at the early specification of a number of key elements in the system. It is hoped to have a fairly completely specified model within the next 6 months. Following this, prototype construction will be undertaken, and hopefully a demonstration system will be operating within two years.

Summary

The FASTBUS concept has been firmly accepted by a large group of high energy physics laboratories as a worthwhile development to meet the future need for a laboratory standard. Task groups are making solid progress in specific conceptual designs, and specifications for certain key elements in the system should be available within the next 6 months. If ERDA funding requests are granted, the present rate of work can be accelerated, which is essential to meet the proposed two year basic development period. In the absence of special funding, the work will still proceed, but at a considerably slower rate.

Acknowledgment

A large contingent of interested and dedicated people has contributed to the FASTBUS development. Most of these are recognized in Appendix A.

Appendix A

List of Participants

Advanced System Study Group (terminated Feb. 1977)

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F. Kirsten	LBL		
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References

1. "Future Data Bus Requirements for Laboratory High Speed Data Acquisition Systems," US NIM Committee USERDA TID 26621, June 1977.
2. SLAC, FERMILAB, LASL, NBS, BNL.