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SIMPLE CAMAC TEST SYSTEM BASED ON THE S-100 BUS*

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Summary

A simple CAMAC test system based upon the use of the S-100 (Hobbyist) bus has been implemented at SLAC. The IMSAI 8080 computer is used, containing 16K bytes of RAM and 1K bytes of EPROM. All programming and operator interaction takes place via a thermal printer-keyboard, and all test programs are written in IMSAI BASIC. The system has been used to test components, CAMAC modules, and complex CAMAC systems.

Introduction

The initial goal of this project was to develop a simple computerized test system to test CAMAC modules in HEEP (High Energy Equipment Pool). It soon became obvious that such a system would have an even broader application in the testing and exercising of complex modules and CAMAC systems then in the development stage. In other words, it appeared to have considerable potential as a general laboratory tool. One of the important side benefits of computerized testing of modules and systems is a significant reduction in the amount of specially designed test equipment. In addition, thorough laboratory testing obviously reduces the difficulty of in-place testing after installation in a larger system. The CAMAC concept, as it turns out, is an excellent medium for testing, exercising, and measuring of complex electronic equipment.

The ground rules and basic considerations for this system are summarized as follows: (1) low cost, so it can be economically duplicated; (2) simple, to minimize training time, reduce maintenance, and maximize its use to all levels of personnel; (3) self-contained, independent of the SLAC Computer Center, for ease of use; (4) speed of secondary importance, since no real-time applications were expected; (5) programming to be done in BASIC for maximum accessibility, and minimum operator training; (6) microprocessor based, for possible educational value, reliability, ease of maintenance, and low cost; (7) system development time to be minimized to meet actual testing schedules.

The Basic System Description

What evolved as a solution satisfying these goals is the S-100 bus system shown in Fig. 1. The computer is an IMSAI 8080, purchased assembled and tested, consisting of the full control panel, 8080A microprocessor card, four 4K RAM cards (based on 2102), a 4K PROM card (based on 8702) containing about 1K bytes of EPROM, a serial interface (based on a UART) for the CDI Model 1203 thermal printer-keyboard (30 CHAR/sec), a tape cassette interface (Tarbell) for an audio cassette recorder, and a CAMAC interface for the SLAC CAMAC Branch which can control up to seven CAMAC crates. The crates contain modules under test and special stimuli-response modules as required. The total purchase price of the assembled system was about $3000, not including the terminal or the CAMAC equipment.

Basing the system on the S-100 (Hobbyist) bus gives access to many low cost peripherals. The cassette interface (Tarbell), for example, costs $170, and runs at 187 bytes/second, permitting an 8K load in 43 seconds. A manually operated audio cassette recorder running at 1-7/8 inches/second is used. This is used to load the IMSAI 8K BASIC interpreter into RAM as well as to store and load BASIC test programs in the 8K program space. Software (including checksum) for the

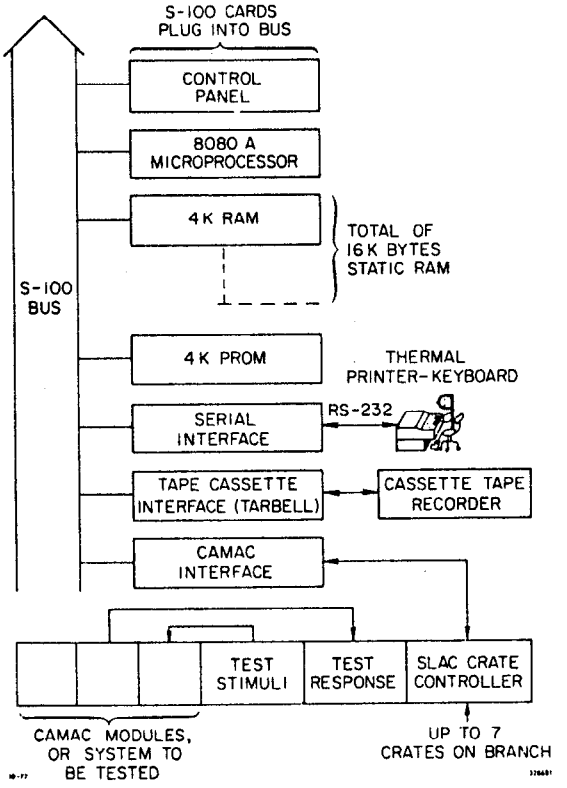

Fig. 1 System Block Diagram

Tarbell interface was supplied with the interface card, and resides in EPROM. SAVE and LOAD instructions permit the operator to handle the necessary tape operations in BASIC. The Tarbell interface records a phase encoded track on standard audio cassette tape.

The speed of an 8080A is summarized as follows. There is a 2 MHz clock, corresponding to a 500 nsec "state." Each instruction takes 4 to 18 states, or 2 usec to 9 usec. For example, to read 8 bits from memory to a register in the processor takes 2.5 usec. An 8 bit input or output to a port takes 5 usec. Actual operating times of the system when using BASIC are of course much longer.

The S-100 Bus and the CAMAC Interface

The S-100 bus is now a defacto standard in hobbyist computers and is used by companies such as Altair, IMSAI, Cromemco, Polymorphic Systems, among others, that are based on 8080 products. Many RAMs, peripherals such as floppy disks, etc., are available from a proliferation of companies. The bus consists of 100 pins and is functionally depicted in Fig. 2. All signals are TTL levels.

Bus operation is based on a byte parallel transfer with a 16 bit memory address (permitting 64K bytes of memory). Signals from the processor indicate whether it is a memory read or write operation (MEMORY READ, MEMORY WRITE). The processor can be "held" by the Ready line for slow memories. For input/output operations to 8 bit registers, 8 address bits are used (allowing 256 8-bit ports) along with the necessary control signals indicating an output (OUT and WRITE) or input (INPUT and READ) operation.

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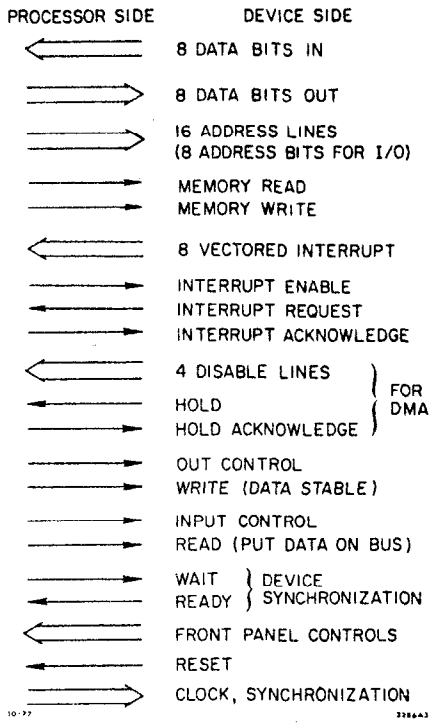


Fig. 2. S-100 Bus

Other signals on the bus include 8 vectored interrupt lines, interrupt handling lines, disable lines to disable drivers for DMA operations, various lines for front panel controls, clocking and synchronizing lines, and +8V and -16V power. The +8V is regulated to +5V on each card independently.

Both the connector and the card dimensions are "standard" so that cards can be interchanged among various manufacturers.

An S-100 CAMAC interface for the SLAC branch,[1] designed previously by D. Gustavson, was used without modification for this project. It is generalized and permits all CAMAC operations in up to 7 CAMAC crates. The interface consists of 41 chips on a single S-100 board.

A simplified block diagram of the interface card is shown in Fig. 3. Basically the CAMAC Command register and the

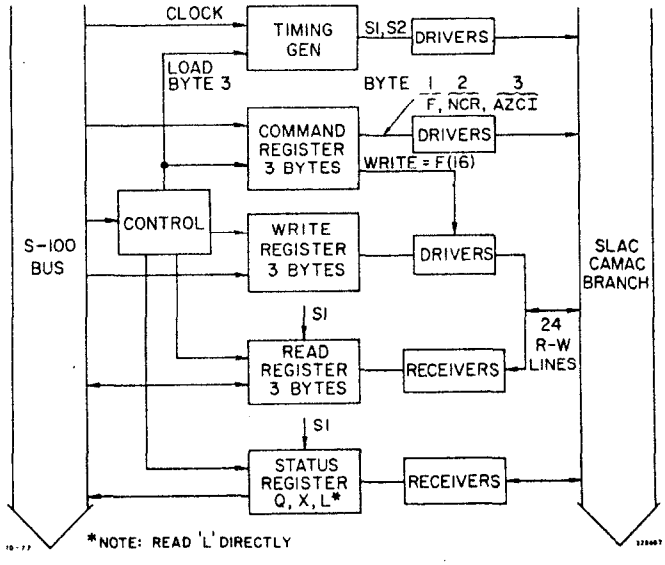


Fig. 3. Block Diagram of CAMAC Interface

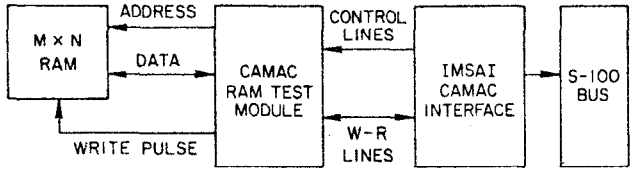
Write register are each 3 byte ports on the Digital Output bus, loaded when the appropriate 8 bit address is accompanied by OUT and WRITE. Likewise, the 24 bit input register and the 3 bit status register are read as four byte input ports. The F(16) bit in the Command register controls the flow of information from the Write register to bi-directional data lines on the SLAC Branch. The 3 usec CAMAC cycle runs from the 2 MHz clock and is automatically initiated when loading Byte 3 of the Command register (i.e., when loading A, Z, C, I). Thus in performing a Write operation one first loads the Command Bytes 1 and 2, loads the Write register, and then performs the CAMAC operation by loading the subaddress (Byte 3). In doing a Read operation the Read register is loaded by the S1 strobe. Q, X, L can be checked after a CAMAC cycle by reading the Status register. L can actually generate an interrupt by connection to the interrupt request bus but there is normally no need for this when testing modules.

The necessary machine codes and bit assignments are shown in Table I. Machine code operations and port addresses are Hexadecimal, and the corresponding decimal port address equivalents are shown for use in BASIC, which is decimal oriented. Of course, in BASIC the data byte must also be in decimal; to handle CAMAC operations in IMSAI BASIC the available functions (OUT A, X) and (X = INP (A)) are used, (where X is the data byte in decimal, A is the decimal port number). Decimal equivalents of the data bits may either be calculated or directly converted. Note from Table I that station number, function code, and subaddress convert directly to decimal when the crate address is "0" and there is no Z, C, or I.

RAM Test Example

A simple example of testing a RAM chip will be described to illustrate how a test module is configured, and how test code is written.

First, a CAMAC module to carry the memory chip is designed and built, as shown in Fig. 4. Since run time is



RAM TEST CODING:

N·F(17)·SA(0)·SI	LATCH 12 BIT ADDRESS REGISTER FROM WRITE LINES
N·F(16)·SA(0)·SI	WRITE DATA INTO MEMORY
N·F(0)·SA(0)	READ OUT DATA ON READ LINES

Fig. 4. RAM Test Module

generally of secondary importance, the hardware in the module is minimized for reliability and flexibility, leaving the remainder of the task to the software. In essence, the module consists of conventional CAMAC decoding, a memory address register loaded by F(17), and CAMAC readout gates for the memory data. Such a module has been designed and built with a 12 bit address register and up to 9 bits of data, with paralleled sockets on the front for several popular RAM chips used in our systems.

Second, a test criteria is established, and a flow chart is developed. In this case, for demonstration purposes we have arbitrarily decided on the procedure charted in Fig. 5. This procedure detects stuck-at-zero, stuck-at-one, and "shorted"

Table I

CAMAC Port Assignments

OP CODE (HEX)	PORT ADDRESS HEX	PORT ADDRESS DECIMAL[b]	D7	D6	D5	D4	D3	D2	D1	D0
D3 (OUT)	F0[a]	240[a]	I[e]	I[e]	C	Z[c]	A8	A4	A2	A1
	F1	241	W8	W7	W6	W5	W4	W3	W2	W1
	F2	242	W16	W15	W14	W13	W12	W11	W10	W9
	F3	243	W24	W23	W22	W21	W20	W19	W18	W17
	F4	244	CR4	CR2	CR1	N16	N8	N4	N2	N1 (d)
	F5	245				F16	F8	F4	F2	F1
DB (IN)	F0	240						L[f]	X	Q
	F1	241	R8	R7	R6	R5	R4	R3	R2	R1
	F2	242	R16	R15	R14	R13	R12	R11	R10	R9
	F3	243	R24	R23	R22	R21	R20	R19	R18	R17

Notes a. CAMAC cycle (S1, S2) is initiated by loading port $(F0)_H$, 240_{10}

b. Decimal port addresses used in BASIC OUT AND INP statements.

c. Performing Z operation automatically sets I=1.

d. In the SLAC branch N is 0-23, CR is 0-6. N=31— All Modules, C=7— All Crates.

e. There is a flip-flop for I. Bit D6 sets I, Bit D7 resets I.

f. L is presently read as Status Bit. Can be connected as Interrupt.

adjacent bits, but it is not meant to be an optimum memory test, a highly complex subject on its own.

The actual code implementing the flow chart is shown in Table II. For anyone with beginning knowledge of BASIC, the program is self-explanatory. Note in particular that the OUT and INP functions handle the CAMAC interactions, and that the CAMAC cycle is initiated by OUT 240, A.

Experiences and Future Plans

This system has already proven an invaluable tool in testing complex CAMAC systems and modules, and was responsible for the rapid completion of the Mark II trigger system, reported elsewhere in this Symposium.[2] It has also been used to test a complex CAMAC branch driver module containing a 4K × 16 bit RAM. Another use has been to measure the linearity of a 14 bit A/D converter; in this application the computer averaged 100 measurements and converted the binary data to decimal for direct plotting of many points. Another test utilizes multiple operations on CAMAC modules to look for marginal operation or intermittents. All of the tests described above would be impossible without a computer based test facility. Indeed, this approach to testing has reduced the need for specialized test equipment and greatly speeded system debugging.

There were some difficulties in bringing the system to reliable operation due primarily to a few poor solder joints, and some "slow" memories, the latter defect finally diagnosed by the IMSAI service department. Since these problems have been corrected the system has run reliably with no component failures, although we have experienced some unexplained system crashes (loss of memory contents) when entering programs from the keyboard. The IMSAI service department suggests that these are caused by an imperfect BASIC interpreter, and has supplied a new version that we have not yet used. Other software improvements have been made, such as correcting a non-functioning exponential function. Eventually when this software settles down we probably will commit the BASIC to EPROM, for improved system operation. It is of some interest to note that a teletype is necessary in system development to read paper tapes containing the system software.

The tape unit has proven quite reliable, and fundamental to the use of the system. To eliminate the need for tape searching a single tape is dedicated to the testing of a particular module or system, and filed for future use. Soft read errors do occur sometimes, and a re-read takes less than a minute. A more reliable, faster, file oriented automatic tape or disk system would streamline operation, but so far the low cost audio cassette has been acceptable.

The use of IMSAI BASIC for testing has proven quite successful, and the procedure is easily learned by technicians and engineers. Even the byte oriented CAMAC driver statements have proven easy to work with, but a bit oriented capability for data would obviously be a worthwhile improvement. The 8K program space has so far been adequate for test programs.

The system is slow in execution, and for large memory testing this is an obvious limitation. For example, to do a FOR-NEXT loop including one OUT statement takes about 26 ms, for a "loop rate" of 38/sec.

We understand that faster versions of BASIC are available. Moreover, other versions of the 8080 family, such as the Z-80, run up to twice as fast as the present 8080A.

We have found that even for "fast" electronic systems, testing at the much reduced rate of the computer detects a high percentage of defects. That is, once "high speed" operation has been confirmed in prototype tests, further production tests can be performed at the lower computer speed.

The use of the 30 CHAR/sec thermal printer-keyboard has proven quite successful. There have been no failures over six months and the low audible noise is appreciated in the laboratory environment.

Acknowledgments

The authors gratefully appreciate the support of John Steffani in bringing the system to operation, providing the necessary EPROMS to load paper tapes, and integrating the Tarbell subroutines on EPROMS with IMSAI BASIC.

Lichen Wang provided important guidance in debugging and testing the system.

Dave Gustavson designed the CAMAC interface board.

References

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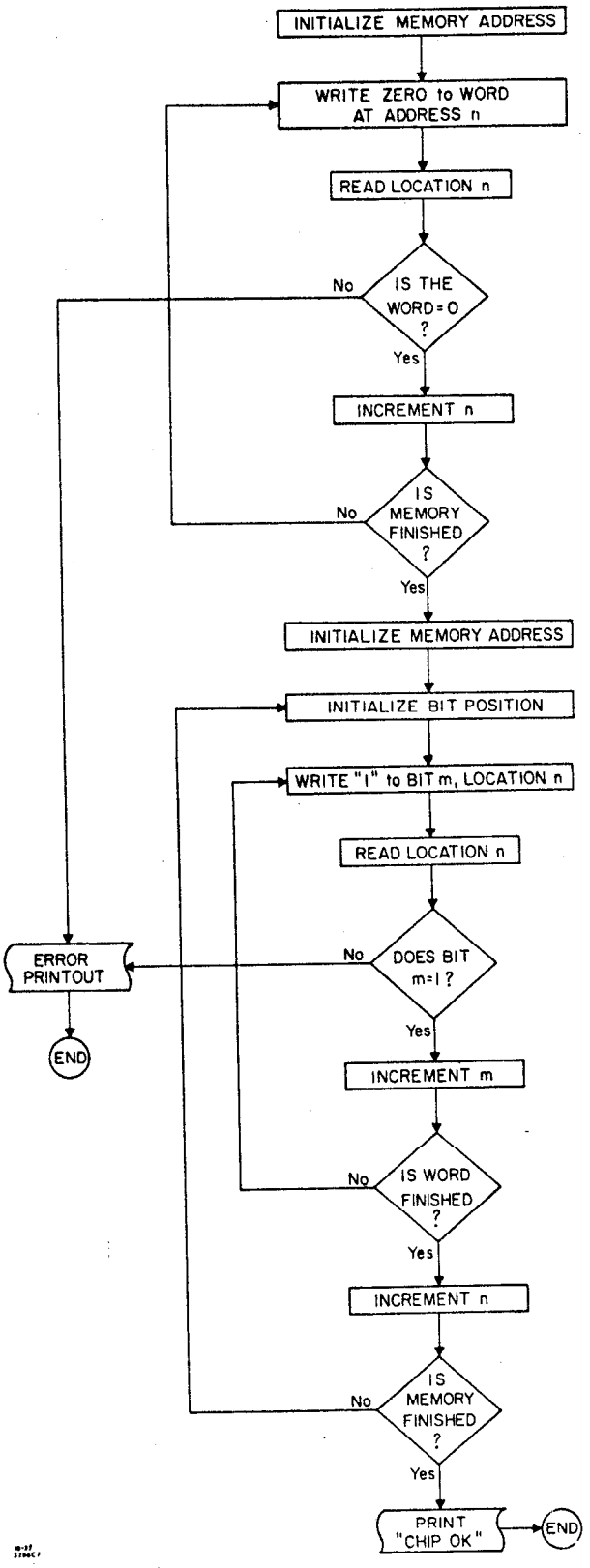

Fig. 5. RAM Test Flow Chart

Table II

RAM Test Program in BASIC

	BASIC PROGRAM	COMMENT
10	REM BEGIN ZERO TEST	M bit × N word memory
		M ≤ 8 bits
		N ≤ 8 bits
20	OUT 244,0	Address module 0, crate 0
30	OUT 240,0	Subaddress 0
40	FOR J=0 to N-1	Begin address count
50	OUT 245,17	F(17)
60	OUT 241,J	
70	OUT 240,0	Latch address in module
80	OUT 245,16	F(16)
90	OUT 241,0	
100	OUT 240,0	Write "0" into address J word
110	OUT 245,0	F(0)
120	OUT 240,0	Read address J word into interface register
130	X = INP(241)	Input word
140	IF X=0 THEN 160	Read test OK
150	GOSUB 360	Go to error report
160	NEXT J	Repeat for N words
170	REM BEGIN TRAVELING BIT TEST	
180	FOR J=0 to N-1	Begin address count
190	OUT 245,17	F(17)
200	OUT 241, J	
210	OUT 240,0	Latch address in module
220	FOR I=0 to M-1	Begin bit scan
230	OUT 245,16	F(16)
240	OUT 241, 2↑I	
250	OUT 240,0	Write "1" in bit I, address J
260	OUT 245,0	F(0)
270	OUT 240,0	Read address J word
280	X = INP(241)	Input word
290	IF X = 2↑I THEN 310	Check word
300	GOSUB 360	Go to error report
310	NEXT I	Repeat for M bits
320	NEXT J	Repeat for N words
330	PRINT "CHIP OK"	
340	GO TO 370	
350	REM ERROR REPORT	
360	PRINT "ERROR DETECTED IN WORD" J, "END OF SCAN"	Report address of error, exit routine
370	END	