SLAC-PUB-2033
October 1977
(I)

FAST TRACK-FINDING TRIGGER PROCESSOR FOR THE SLAC/LBL MARK II DETECTOR*

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Summary

The SLAC/LBL Mark II Magnetic Detector consists of various particle detectors arranged in cylindrical symmetry located in and around an axial magnetic field. A versatile, programmable secondary trigger processor has been designed and built to find curved tracks in the detector. The system operates at a 10 MHz clock rate with a total processing time of 34 μsec, and is used to "trigger" the data processing computer, thereby rejecting background and greatly improving the data acquisition aspects of the detector-computer combination.

Introduction

The SLAC/LBL Mark II Magnetic Detector is a large solenoidal detector for the SPEAR and PEP storage rings. It consists of a series of concentric detectors in an axial magnetic field, designed to track the particles generated from a positron-electron collision. As a particle leaves the central interaction region it passes through the following detector layers:

1) A scintillation counter called the pipe counter.
2) 16 layers of drift chambers. These consist of 6 axial layers (parallel to the beam line) and 5 each with ± 3° stereo angle. The number of cells in a layer varies from 144 on the inside to 252 on the outside.
3) A layer of 48 scintillation counters.
4) The magnet coil.
5) A liquid argon shower counter.

Some particles will emerge at small angles to the beam axis. These may go through some of the cylindrical drift chamber layers and then into a liquid argon endcap detector. The liquid argon endcap detector has several sets of strips for position determination. Among these are sets of radial "fan blades" which determine the azimuthal angle.

The purpose of the trigger logic is to decide when an interesting interaction has occurred so that the event can be logged and analyzed. The requirements on this trigger are stringent. The beams consist of very short bunches which collide every 780 ns at SPEAR and every 2.4 μs at PEP. During each collision, low energy photons and other backgrounds can generate random hits in the detectors which can simulate events. The trigger logic should eliminate these, while accepting real events.

The Mark II trigger logic utilizes a two "tier" decision process: The primary trigger decides in <500 ns whether an event is of further interest, and the secondary decision is made only if the primary decision is positive. The secondary trigger (track finding) takes more than the inter-collision time to find tracks and make its decision, so the primary trigger must be used to limit the deadtime caused by the track finding.

The track finding logic is expected to reduce the number of logged events to an amount that can be reasonably analyzed. Each time there is a primary trigger the secondary trigger scans selected data. If it finds an appropriate set of tracks, then the event is logged. Otherwise the detector electronics is reset and another event awaited. While the track finding logic is operating, the detector is insensitive to other events, thus introducing a deadtime. With a primary trigger rate of 1 KHz, the deadtime fraction can be held to 3% if the track finding logic operates in 30 μs, the design goal of the track finding processor.

The track finding is expected to be completely efficient for tracks coming from the interaction region and reaching the outer scintillation counters. These tracks are helicies and, in transverse projection, are arcs of circles which start at the beam line and extend through the drift chambers (see Fig. 1). This projection is produced by the 6 axial drift chamber layers. Thus the track finding logic attempts to find all sets of points that lie along circular arcs and to reject all noise points.

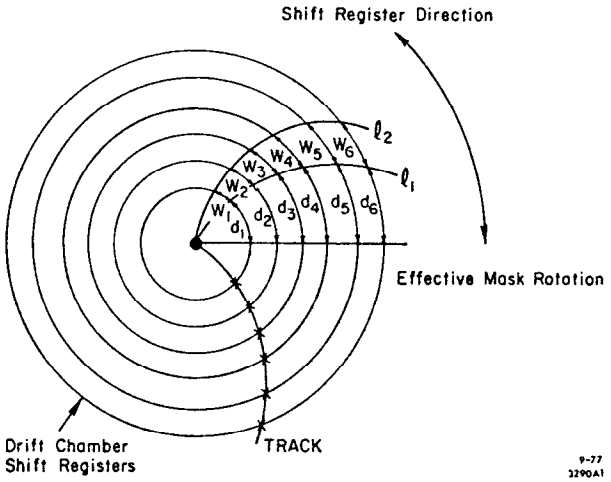

Fig. 1 Track Finding Principle

In addition to tracks going through all the drift chamber layers, it is desirable to find tracks going towards the endcaps. This requires using data from the endcap liquid argon detectors and checking if tracks which start in the inner layers of the drift chamber extrapolate to the endcaps. This is done by mapping the "fan blade" layers of the endcaps into shift registers. The track finding logic will accommodate up to 12 channels of data shift registers. We expect to use 6 channels for the axial drift chamber layers, 3 channels for the endcap system, and the remaining channels for the scintillation counters or inner stereo drift chamber layers.

A further requirement of the secondary trigger is to count the tracks that are found so it can make the final trigger decision. This information, along with the curvature and azimuthal angle of each track, should be saved by the hardware for later use by the computer. In addition, the hardware should be fully programmable so that changes in the trigger logic can be easily made as experience is gained. Since the experiment is dependent on this logic, it should be easy to diagnose and repair faults.

It is hoped that this track finding logic will make possible a trigger that requires only one or more charged particles reaching the outer scintillation counters. In contrast, the

* Work supported by the Department of Energy.

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(Presented at the IEEE 1977 Nuclear Science Symposium, San Francisco, Ca., October 19-21, 1977)

earlier Mark I Detector required at least two charged particles of momenta considerably higher than that required to just reach its scintillation counters. This complicated trigger had an efficiency which was difficult to calculate, and the uncertainty of this efficiency caused the largest uncertainty in the measured cross sections. The single particle trigger should have a very high efficiency (approx. 92%) with a very small uncertainty, because the efficiency is mainly determined from geometric considerations.

General Principle of Operation

The general track finding principle as illustrated in Fig. 1 employs shift registers to effectively "rotate" the circularly arranged track data (all stored in data shift registers) past a multiple input coincidence or multiplicity gate. It is apparent that straight tracks originating at the center produce time coincident data and can be detected quite directly in this approach. Moreover, by artificially extending or "widening" the data bits a "road" can be effectively generated. Such a technique based upon shift registers has been used before in fast track finding processors for physics.[1,2]

In order to detect curved tracks it is only necessary to introduce the necessary delays in each of the circular rings of data to transform the curved track into a straight track where the data is again time coincident, and can be detected by a coincidence, or multiplicity gate. Fig. 1 shows how the variable delays and data wideners would be set to generate a road to detect the particular track shown. Thus after the delays and wideners are set, and the data is rotated once, any curved track originating at the center and falling within the road width is detected regardless of angular position. In order to detect the wide range of curvatures of interest within one rotation of the data, a number of such roads (Curvature Modules) must be operated in parallel. Alternatively one could perform multiple rotations of the data, changing the delays and wideners for each rotation, but the system clock rate must then be significantly increased to meet the original 30 μsec goal.

In our case, where there are a maximum of 252 elements in a ring, the use of a 10 MHz clock permits the use of TTL components, achieves 360° rotation in 25 μsec, but requires the use of the parallel processing approach as described above.

Computer Simulation

To verify and optimize the system performance a computer simulation was run. In this simulation, we could easily vary the number of curvature modules and try various algorithms for setting the delays and widths which make up the roads. Then having set the simulator parameters, we generated random tracks, calculated what parts of the detector they would pass through, inserted the appropriate shift register bits, ran the simulator program, and checked to see if the track was detected. In this way we verified that the system had 100% efficiency for tracks coming from the interaction region. Figure 2 also shows how this detection efficiency decreases as the distance of closest approach of the track to the beam line increases. For this curve the simulator was run with our final system configuration of 24 curvature modules and with the requirement that at least 5 out of the 6 axial drift chamber layers have hits within a road. Note that the efficiency is rapidly decreasing at 30 cm, showing that the system provides good cosmic ray rejection for particles more distant that this.

The simulator was also used to determine noise sensitivity. For this calculation, random bits were inserted in the shift registers and the track finding logic operated to measure how often a false track was found. Figure 3 shows this probability as a function of the number of random points inserted. Each point on the graph represents 1000 runs of the simulator, each with a different set of random points.

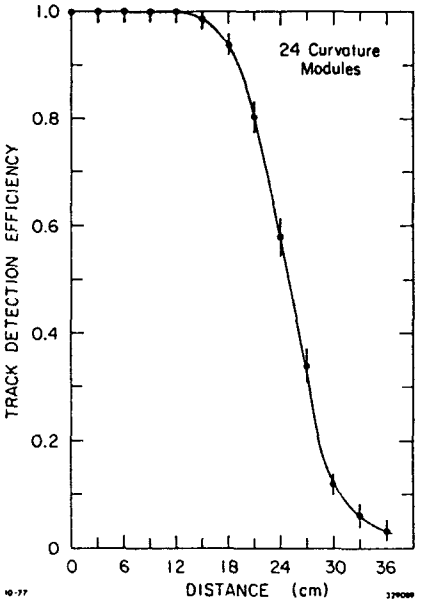

Fig. 2 Track Finding Efficiency as a Function of Distance of the Track to the Beam Line.

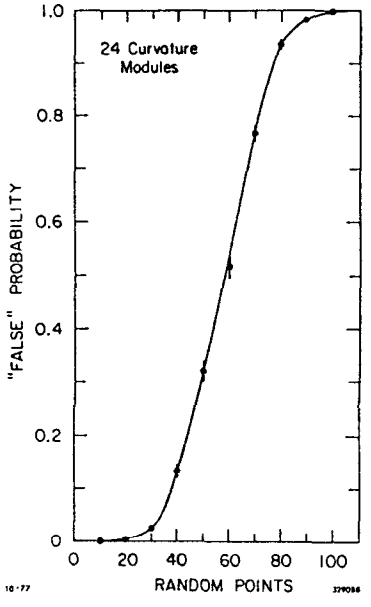

Fig. 3 Sensitivity to Random Noise Points in the Detector

From existing Mark I data we expect one noise point per drift chamber layer. Noise sensitivity information such as this was used to decide on the number of Curvature Modules to use in the system. Decreasing the number of modules increases the sensitivity to noise because each road must be wider to span the same total curvature range, and thus is more likely to contain enough random points to make a false track. The simulation shows that increasing the number of Curvature Modules beyond 24 did not appreciably improve the false track rate.

Another use of the simulation program has been to check the hardware. By running the same data through the simulator and the hardware we can verify that the hardware is working properly. Finally, the simulator demonstrates the power of special purpose parallel processing. What the trigger logic system does in 34 microseconds takes an IBM 370/168 one second; that is, the 168 would need to have a cycle time of roughly three picoseconds to be as fast as the trigger logic for this application.

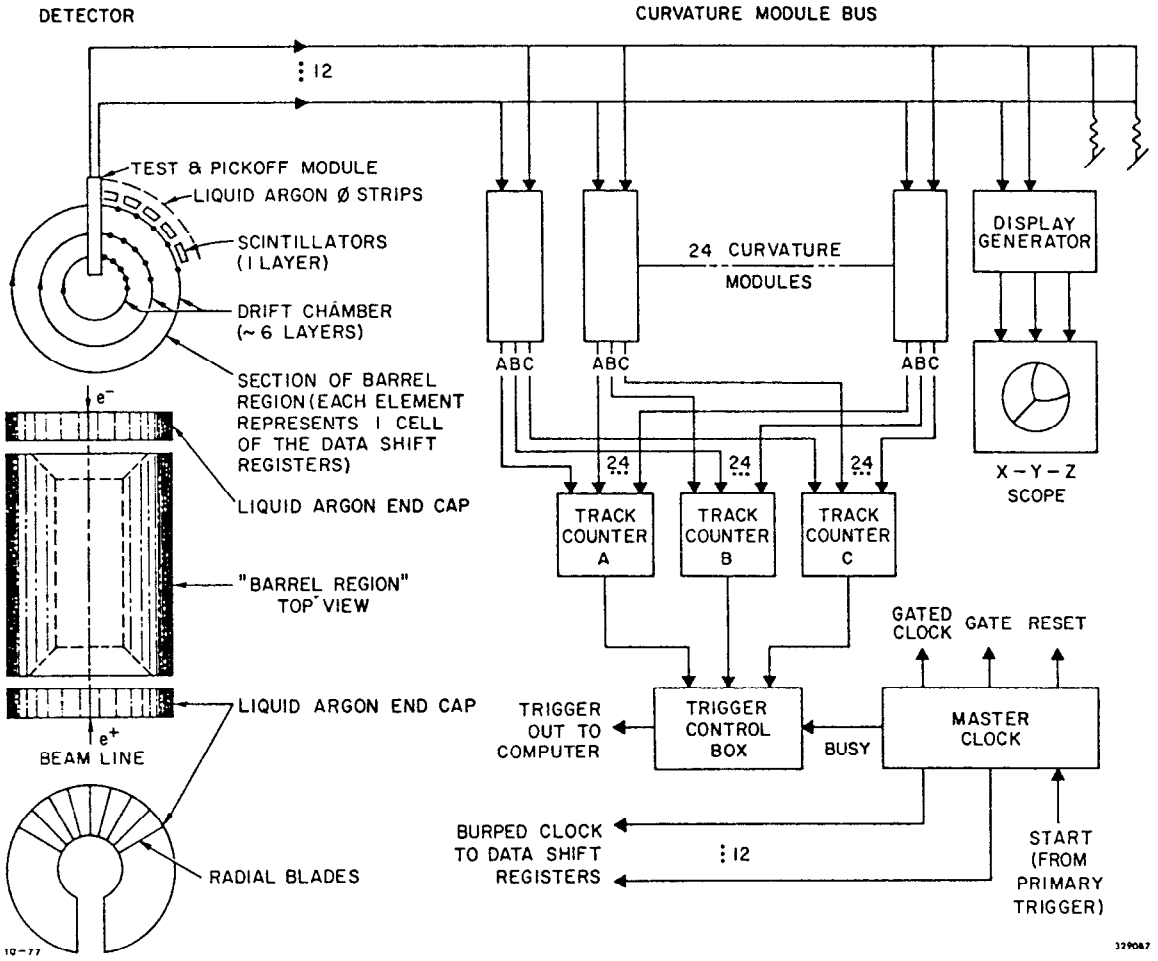

Fig. 4 Trigger System Block Diagram

Description of the Processor System

The complete system with its basic components is shown functionally in Fig. 4. All of the data, whether from drift chambers or the liquid argon detectors, is stored in data shift registers connected in re-circulating circular loops. Data from each detector layer is extracted in the Test-Pickoff module, and sent in 12 parallel paths to the 24 Curvature Modules, each of which contains variable length shift registers (VLSR's) and wideners programmed to sweep the data with a particular curvature road. The 12 channel Curvature Modules can also classify the tracks into 3 classes (A, B, C) depending on the combination of the channels that contain "hits." The three Track Counters merge the track data from the 24 Curvature Modules, decide how many discrete tracks occurred in each class, and store track azimuthal angle and curvature data for subsequent use by the data processing software. Finally the Trigger Control Box examines the summarized data from the Track Counters and decides whether the event is to be recorded, or the detector re-enabled for a new event.

The entire operation, starting with the primary trigger (start), is controlled by the Master Clock which generates the proper sequence of reset, clock, gate, and busy signals; the latter signal is used to kill primary triggers for 34 μsec while the secondary trigger processor is operating.

The data from the circularly arranged shift registers is stored in a display module, which displays "raw" data on an X-Y-Z scope in a concentric circular pattern simulating the arrangement of the actual detectors. In this way tracks will be made visible; excessive noise and some types of failures will become obvious.

Test capabilities are built into the system. For example, simulated track data can be inserted into the data shift registers via the Test-Pickoff module, re-circulated and read back to verify the data shift registers, then processed by the track finding system to verify overall performance. In addition each Curvature Module includes an output latch which can be read independently by the computer to verify operation and/or locate defective modules. Extensive diagnostic software has been written utilizing these test capabilities.

All of the components of the system are constructed as CAMAC modules which simplifies packaging, interconnections, maintenance, and the computer interfacing of the system. In the case of the Curvature Module, packaging in CAMAC was made possible primarily by the use of low power Schottky circuits which kept the current per module to about 3.5A. The 10 MHz data signals from the data shift registers are distributed to the curvature modules on a special back plane at the upper rear of the crate, which is carefully constructed and terminated for optimum signal transmission. All data signals and clocks in the system are TTL levels. The entire system is interfaced to the XDS Sigma 5 computer via a previously developed, highly flexible CAMAC interface system. At the time of this writing (October 1977) the entire system is running using a hardware simulator for the data shift registers. The simulator is loaded from the Test-Pickoff module just as the actual data shift registers will be loaded for test purposes.

The Burped Clock and Other Timing Considerations

An interesting complication in the operation of the system is the varying numbers of data elements in the drift chambers, the scintillation counters, and the liquid argon chambers.

These numbers vary from 48 to 252 elements per layer. This complication was overcome by rotating the data shift register for each layer using a "burped" clock, which rotates each layer at the same average angular speed (radians/sec) to scan the detector volume with the curvature roads. Thus the outer drift chamber containing 252 elements is clocked 252 times in a revolution by the 10 MHz clock, but the next chamber containing 216 elements is clocked only 216 times in a revolution by omitting 36 clock pulses. These must be omitted as evenly as possible, hence out of every 7 pulses for the outer chamber the next one receives 6 (hence the term "burped" clock). For 144 elements, 108 clock pulses are missing, or 3 out of every 7. Such a scheme has its imperfections, of course, but simulations have shown that overall track detection/noise rejection performance is acceptable. This approach requires larger roads to achieve 100% track detection efficiency.

The burping pattern is contained in PROM's located in the Master clock. RAM's were not used since the detector geometry changes exceedingly slowly--there is no need to change the burping pattern once the optimum pattern has been verified by simulation.

Although it is necessary to clock the data shift registers in this manner, it is not necessary to "burp" the Curvature Modules. Instead, the continuous 10 MHz clock is used in each channel; the VLSR's are set to detect a particular curvature by normalizing to the maximum 252 elements. That is, each channel is delayed the same amount as if that particular layer had 252 elements. The resulting simplification in the hardware is obvious--the Curvature Modules all operate on the same 10 MHz clock.

It should also be recognized that because the VLSR's in the Curvature Modules contain up to 64 bits of delay, the rotation of the data shift registers must exceed one revolution. To allow for the VLSR's, the wideners, and the burped clock, the total number of clock pulses is increased from 252 to 341 to achieve full angular detection efficiency. However, since there is now more than one data revolution it is necessary to provide a gate after the Curvature Modules, open for 252 clock pulses (one revolution) to count tracks only once. The Master Clock generates this gate at the required time in the scan cycle.

The Curvature Module

Each curvature module is programmed to generate one road. As indicated in Fig. 5, there are 12 identical channels each consisting of a track widener programmable from 0-15 bits and a VLSR programmable from 1-64 bits. The 12 channels of widened and delayed data are used to address a 4K word × 2 bit track logic memory which contains arbitrary track detection criteria pre-programmed from the computer. In this manner a completely arbitrary logic function is generated by software; the 2 memory bits permit classification into 3 classes labelled A, B, C; i.e., every possible combination of the 12 address bits is classified as null, A, B, or C tracks.

Since the wideners and VLSR's are fundamental to the system, being duplicated 288 times, a detailed schematic is shown in Fig. 6. The VLSR is based on a fast RAM and a 6 bit CAMAC programmable counter (W5-W10), the output of which is used to address the RAM. The cycle time of the counter, specified by the pre-programmed delay period, determines the address cycle time of the memory. Data from the widener is first written into a memory cell, and after the pre-programmed delay period the same cell is again addressed and the data is read and stored in an output latch before the same cell is again written. Hence a shift register of variable length is achieved. Note that a memory read-write cycle takes place in 100 nsec, corresponding to the 10 MHz data rate.

Test points are available at the final output and after the VLSR. The prototype Curvature Module was first tested at 10 MHz; thereafter, all production testing was based upon a simple computerized CAMAC test system described elsewhere in this Symposium.[3]

The Curvature Module consists of about 140 chips in a double width CAMAC module

The Master Clock

The Master Clock module is shown functionally in Fig. 7. Its time base is a crystal clock. The scan cycle is started with a primary trigger, after which it first generates a system reset, followed by burped clocks, gated clocks, the gate, and a busy signal. The burped clock's sequence is derived from PROM's. All signals are TTL and capable of driving 50 Ω.

Track Counter

The Track Counter is the most complex component of the system and provides many important but somewhat subtle functions. A block diagram is shown in Fig. 8. Each class (A, B, C) track is processed by a separate Track Counter having 32 inputs permitting the use of up to 32 Curvature Modules. Since the roads overlap in order to achieve 100% detection efficiency, the Track Counter collects the 24 Curvature Module outputs and "merges" outputs occurring within a short time interval, counting these as one track. This time interval is referred to as the anti-chatter interval, and is programmable from 1 to 16. At the end of the anti-chatter interval, thirty-two bits recording which Curvature Modules fired, along with an 8 bit time count is stored in a 64 word, 44 bit memory for each discrete track counted.

At the end of the complete scan the track data memory contains all the data for the tracks detected in that particular class; the 6 bit track counter (MAR) addresses a 64 word by 2 bit trigger logic memory which contains trigger logic criteria for that class which has been pre-programmed from the computer. The two memory outputs classify the number of tracks into 4 arbitrary groups. The 3 sets of outputs from the 3 track counters are then combined in a final Trigger Control Box.

One of the more subtle functions of the track counter is to account for an anti-chatter interval that is left unterminated at the end of the scan. This is done in order to count and store

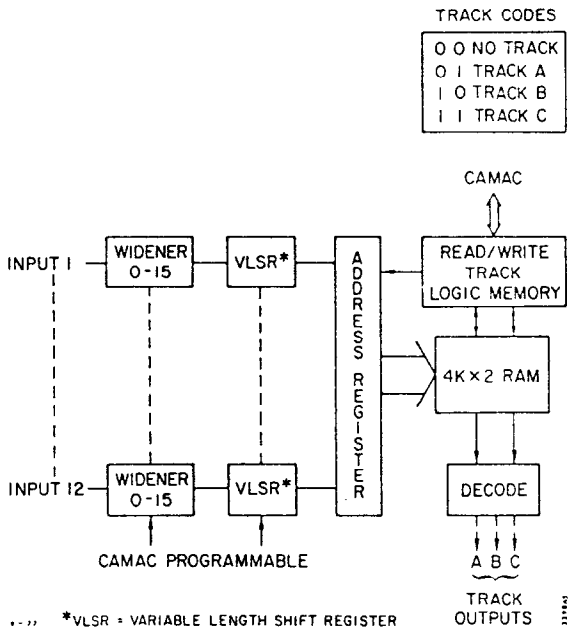

Fig. 5 Curvature Module Block Diagram

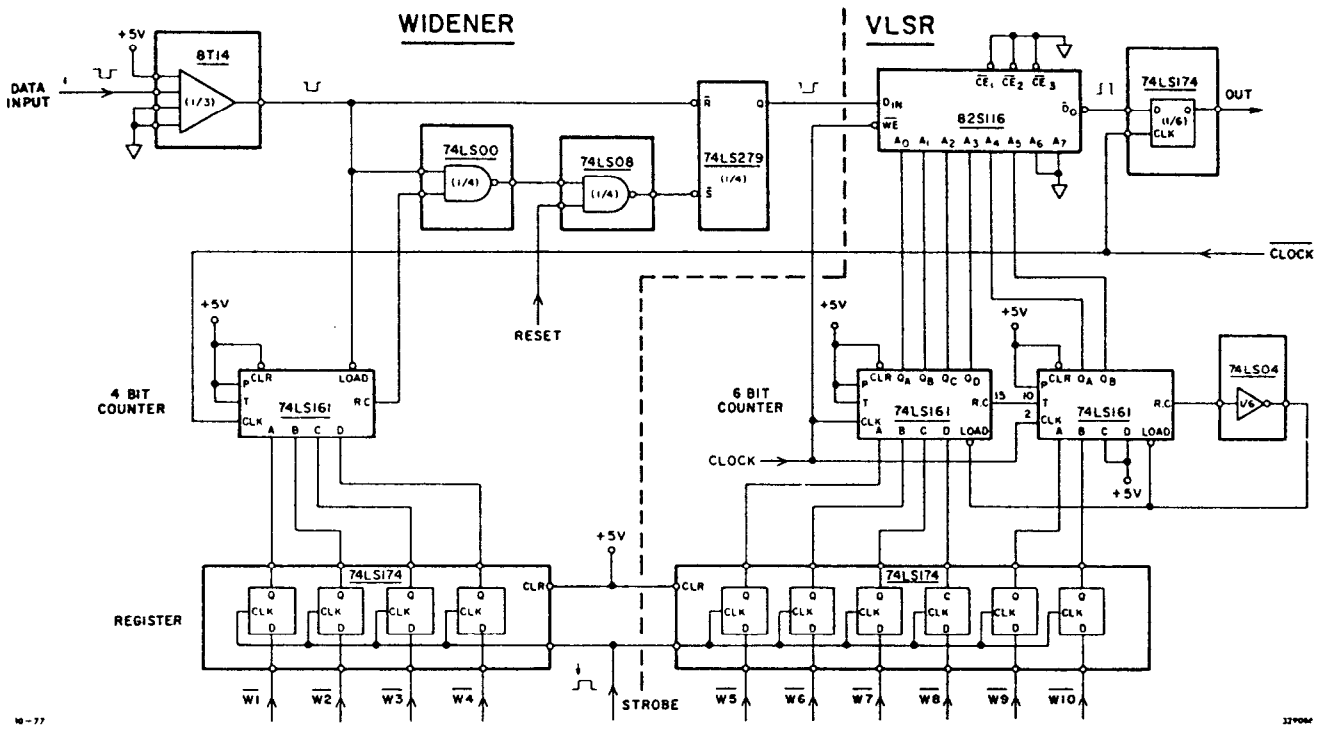

Fig. 6 Widener and VLSR Logic

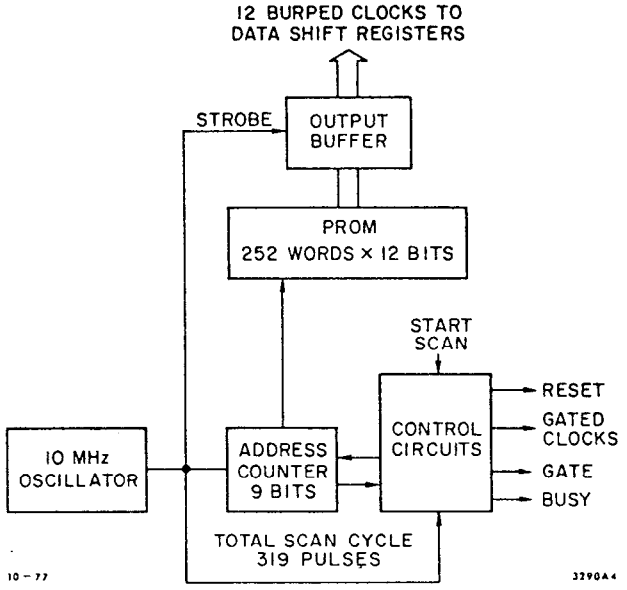

Fig. 7 Master Clock Block Diagram

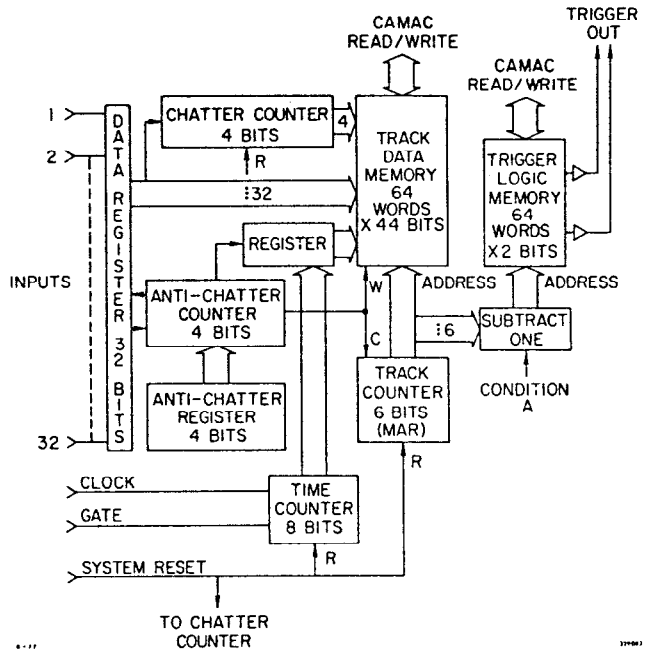

Fig. 8 Track Counter Block Diagram

tracks that would otherwise be lost. A further subtlety is the possibility of an overlap of the anti-chatter interval across the beginning-end scan boundary. Under these conditions, termed "Condition A," one is subtracted from the number in track counter (MAR) before addressing the trigger logic memory in order to correct for the double counting of the same track.

Packaging Concepts

A photograph of the Curvature Module is shown in Fig. 9. Due to the large number of units a conventional printed circuit was made for each of the two boards. These are interconnected with 3M flat cable, and swing open for service. Latches on the track outputs A, B, C drive 3 LED's on the front panel, and can be read by CAMAC.

Due to the low number of duplicate units the remainder of the modules were wire-wrapped.

The full trigger processor, excluding the input data shift registers, is shown in Fig. 10, and occupies 3 CAMAC crates. The 12 data signals from the Test-Pickoff module drive the special backplane via a 36 pin upper rear connector. Gate and reset are carried on the backplane and are driven from the Master Clock. The 10 MHz gated clocks are distributed via coax, connected in daisy-chain fashion and terminated.

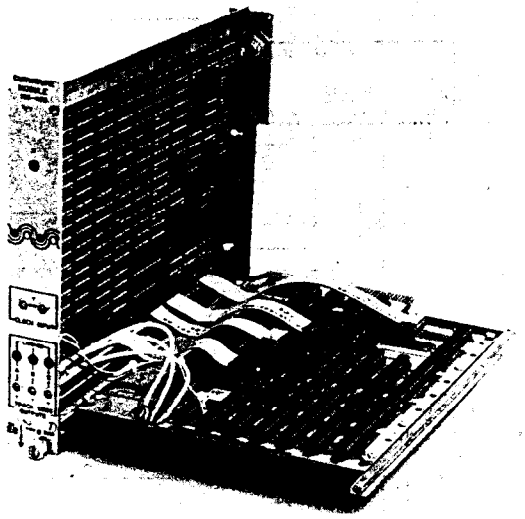

Fig. 9 Photograph of Curvature Module

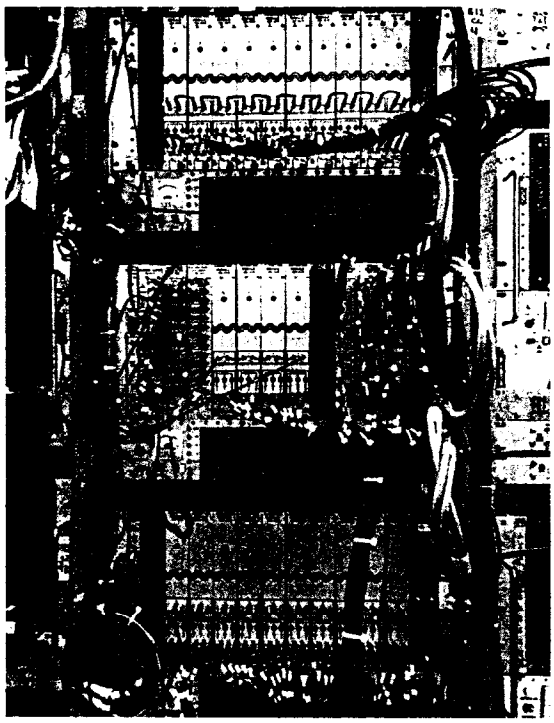

Fig. 10 Photograph of the Trigger Processor

Acknowledgments

Bob Melen was instrumental in the conceptual design of this system and was also responsible for the CAMAC interface system for the Sigma 5 computer. Len Shustek of Stanford Computer Science Department suggested the RAM techniques for the VLSR's, a key component of the system. Eric Dorsey and David Feinstein did early work on the computer simulation. The authors thank the Electronics Assembly Shop under F. Generali for their fine support in the construction of the many components.

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