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DRIFT CHAMBER AND PULSE HEIGHT READOUT SYSTEMS USING ANALOG MULTIPEXING*

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Abstract

Drift chamber and pulse-height readout systems are being developed for use in a new large scale detector at the SPEAR colliding beam facility. The systems are based upon 32 channels of sample-and-hold together with an analog multiplexer in a single-width CAMAC module. The modules within each crate are scanned by an autonomous controller containing a single ADC and memory plus arithmetic capability for offset, gain and linearity corrections. The drift chamber module has a facility for extracting hit wire information for use in trigger decision circuitry.

1. Introduction

In recent years, the size of high energy physics detectors and their associated electronics has increased dramatically, mainly due to the advent of various sorts of multiwire chambers and multi-element solid, liquid or gas counters. This has presented a challenge to electronics designers to match these developments with efficient designs, in order to make arrays of many thousands of channels economically and physically feasible.

The system to be designed requires over 3000 channels of drift chamber electronics and a similar number of channels of analog measurement. The drift chamber measurement requires a nominal range of about 500 ns with a resolution of 2 ns (8 bits) to provide a spatial resolution in the chamber approaching 0.1 mm. The analog measurement requires a $\leq 1\%$ resolution over a dynamic range of 30:1, which leads to a required ADC resolution of 11 bits. With present techniques, an approach using a dedicated 11- or 12-bit ADC per channel would be very expensive; thus it was decided to develop a system of multiplexed analog modules which could be processed in large groups by a single ADC per group. Such a system has general applicability for TDC, ADC, as well as slow analog measurement, such as recording of phototube high voltages, wire chamber dc voltage settings, etc.

2. System Considerations

2.1 General

Any multiplexed analog system must sacrifice processing speed compared with a system using a dedicated ADC-per-channel. One must therefore weigh the advantages or disadvantages of this approach against the design characteristics of the particular detector, especially its projected event rates. The detector being designed is a large cylindrical array of drift chambers and liquid argon shower counters, particularly designed for e^+-e^- storage ring application at Stanford Linear Accelerator Center's SPEAR machine. The SPEAR beam consists of e^+-e^- interactions occurring at a rate of 1.28 MHz, i.e., every 780 ns, within a time window which is known to a fraction of a nanosecond; thus the detector front-end circuitry must be capable of accepting this rate. These beam characteristics are sufficiently similar to the new proposed storage ring at SLAC, called PEP, that the detector will be directly usable at the new machine. The detector also has a cylindrical array of conventional scintillation trigger counters for use in fast primary trigger decisions.

The most important characteristics of the detector electronics are (a) a large number of channels, suggesting as high as possible packaging density and minimum components per channel; (b) rapid reset time (abort) such that, if an event trigger is not received, data can be continued to be accepted at a beam interaction rate of 1.2 MHz (780 ns between interactions); and (c) ability to extract trigger information from the drift chamber electronics for use in special track-finding hardware, to determine whether to further process and transfer the data into the host computer.

2.2 Data Rates

The detector has the usual set of fast NIM trigger logic to identify "raw" events; this electronics uses the outputs from the aforementioned cylindrical arrays of scintillation trigger. This trigger logic produces an output in a time of about 450 ns from the machine trigger pulse which is correlated within a fraction of a nanosecond to the time of the e^+-e^- beam interaction in the center of the detector. The rate of "raw" events is projected to be ~1 kHz, or roughly one every 1000 beam crossings. Thus, the front-end electronics will be sampling new data every 780 ns, and about once every millisecond will enter a hold condition. At this point, more precise trigger information is rapidly extracted from the drift chamber modules, and in 30 μs a decision is made as to whether to convert and transfer the data, or whether to abort (in ~200 ns) and proceed again to sample new data. This portion of the electronics is called the secondary trigger logic system; this will be the subject of a future SLAC publication.

If an event passes the secondary trigger logic decision, processing and subsequent data transfer to the host proceeds. The expected number of events passing the secondary trigger logic test is approximately 1 per second. A typical event has been estimated to cause relevant data to occupy about 10% of the channels in a more-or-less random way; thus a processed event may consist of approximately 600 words of data. The total data acquisition time is therefore approximately

$$T = t_{st} + t_s + t_a + t_b$$

where

t_{st} = secondary trigger decision time = 30 μs
t_s = total scan time (depends on channel occupancy)
t_a = time to acquire computer channel
t_b = block transfer time .

The system configuration must be selected to keep this total time low enough so as not to add a significant deadtime to the experiment. Note that the above equation does not include the computer-to-tape transfer time.

2.3 System Organization

The basic organization selected is shown in Fig. 1.

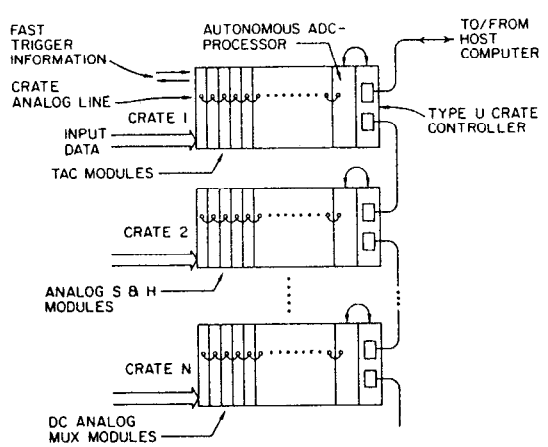

Fig. 1. System organization.

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Each crate contains up to 640 channels (20 modules X 32 ch/module) of multiplexed analog data. Each crate also contains a dedicated autonomous controller with a 12-bit ADC and local memory. The multiplexers could in fact proceed at the maximum CAMAC rate of 1 μs per channel; thus the scanning speed depends primarily upon the slower conversion speed of the ADC, as well as internal setup times. In the 12-bit system being built, the time for conversion is 2.5 μs, and the average processing time per data point with 10% channel occupancy is about 4 μs, leading to a total scanning time for all channels of 2.6 ms. Obviously, the hold circuits must contribute negligible errors for this length of time. As stated earlier, this scanning does not commence until certain secondary trigger logic track-finding criteria have been satisfied.

The above scanning speed of about 2.6 ms is an average for a polled system. Note that, since each crate has an autonomous processor, the average scanning speed is independent of the number of crates in the system. In principle, more sophisticated scanning algorithms could be designed into the modules and controller in order to speed up the total system. In the present detector system, however, the above rate is very adequate, and it was thus decided to keep the module design as simple as possible in order to gain maximum packaging density and economy.

2.4 Autonomous Processor—ADC

To allow use of an autonomous controller in a CAMAC crate, one requires separate access to the N, A and F lines; this is done through a Type U controller (SLAC 135-315) which makes these lines available on an upper rear connector. Enabling of the crate autonomous processors is under the supervision of the system host. Once enabled, the processor has the following general capabilities:

1. Reads, converts and records pedestal values
2. Reads, converts and records system calibration data
3. Decides whether to store data in memory based upon comparison with pedestal value
4. Applies stored programmable gain constant or nonlinear correction to data from each channel
5. Assembles data together with channel address in a memory block, ready for transfer to host.

With a built-in capability to dynamically update pedestal and calibration constants, normal long-term thermal drifts which would be bothersome in making sensitive measurements in such a large system, will be calibrated out of the final data. This of course requires very reliable system calibration techniques. These on-going calibration system developments will be reported in detail in a later SLAC publication.

3. Module Design Summary

The following is a description of the important circuit features of each system module.

3.1 Drift Chamber Module

Drift chamber signals are amplified at the chambers (using LRS 604 hybrid amplifiers) and sent as ECL logic pulses to the channel electronics. The block schematic of a single channel is shown in Fig. 2. The operation is straightforward: The beam gate FET is normally open, and the fast reset pulse is applied at the maximum beam rate of 1.2 MHz to keep C_S discharged. When a drift chamber signal is received, it actuates the input flip-flop and switches I_S from Q1 to Q2 to begin charging C_S with a constant current. At the end of the maximum drift period allowed in the chamber, a load pulse is applied to record the state of all flip-flops in a shift register, and the common stop pulse is applied to reset the current source. At this point, the charge is held on C_S, but the FET beam gate is not yet closed. If no primary event trigger is received during the charging time, the RESET signal is applied to reset C_S, and the circuit is ready to receive data from the next beam pulse. If a primary event trigger is received, the latches and the reset circuit are inhibited from further action.

At this point, the shift register is read into the secondary trigger logic system. If the secondary trigger test is not passed, the RESET is applied and sampling of input data continues. If the test is passed, multiplexing and processing of the analog data proceeds.

The START-COMMON STOP method of operation is preferred in order to minimize switch drive current and switch voltage offsets. Figure 3 shows a section of the detailed schematic; Fig. 4 is the timing diagram. A photograph of the complete 32-channel board is shown in Fig. 5. The multilayer board has 5 layers: 2 outer for signal wiring (odd and even channels on opposite sides), 2 inner for power bussing, and one ground place in the center.* Table I is a summary of the specifications of the module.

*Computer-generated artwork and layout by commercial vendor.

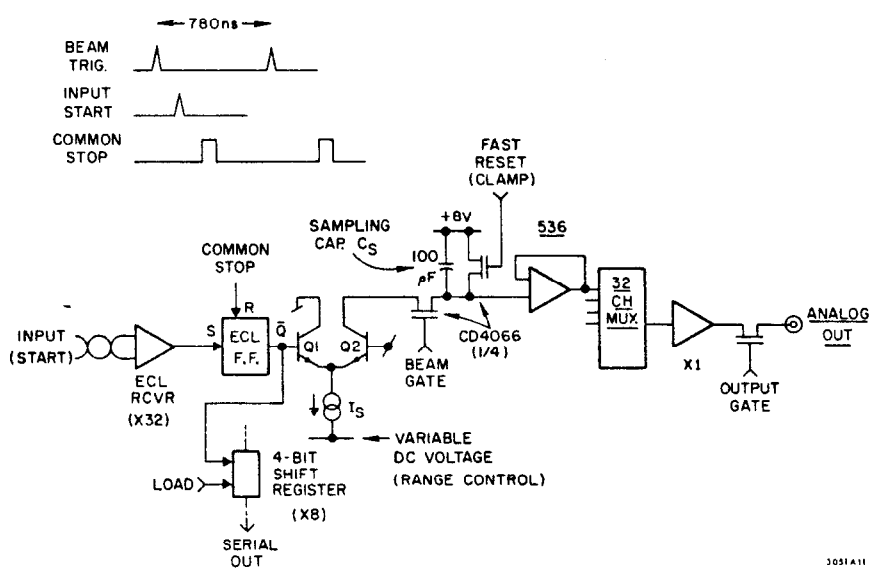

Fig. 2. TAC channel block diagram.

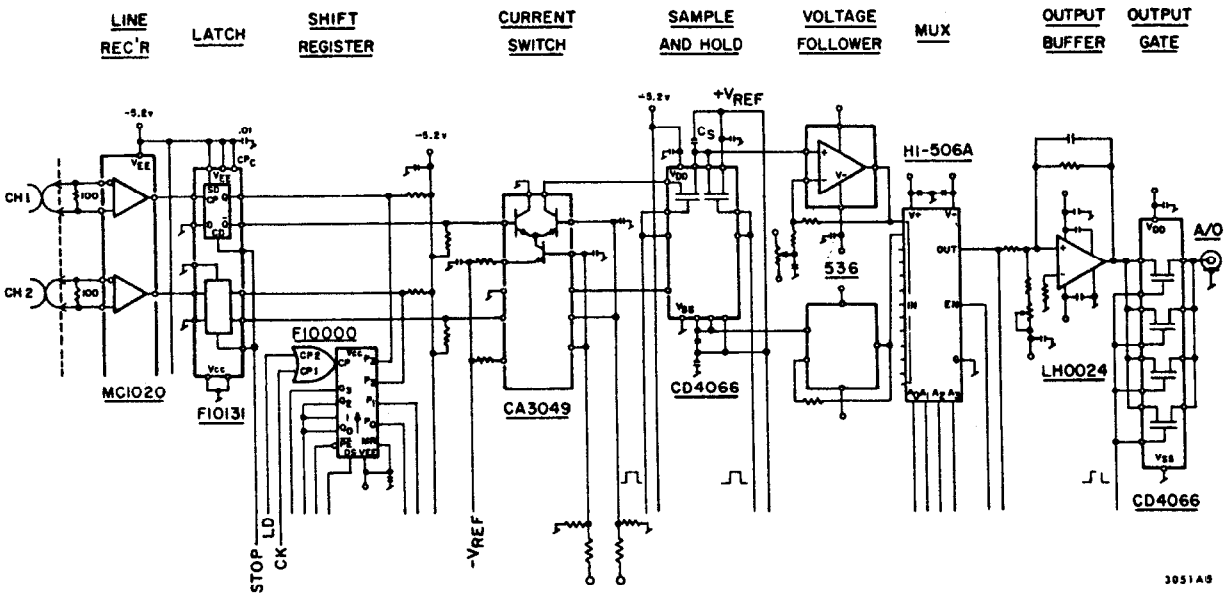

Fig. 3. TAC channel details.

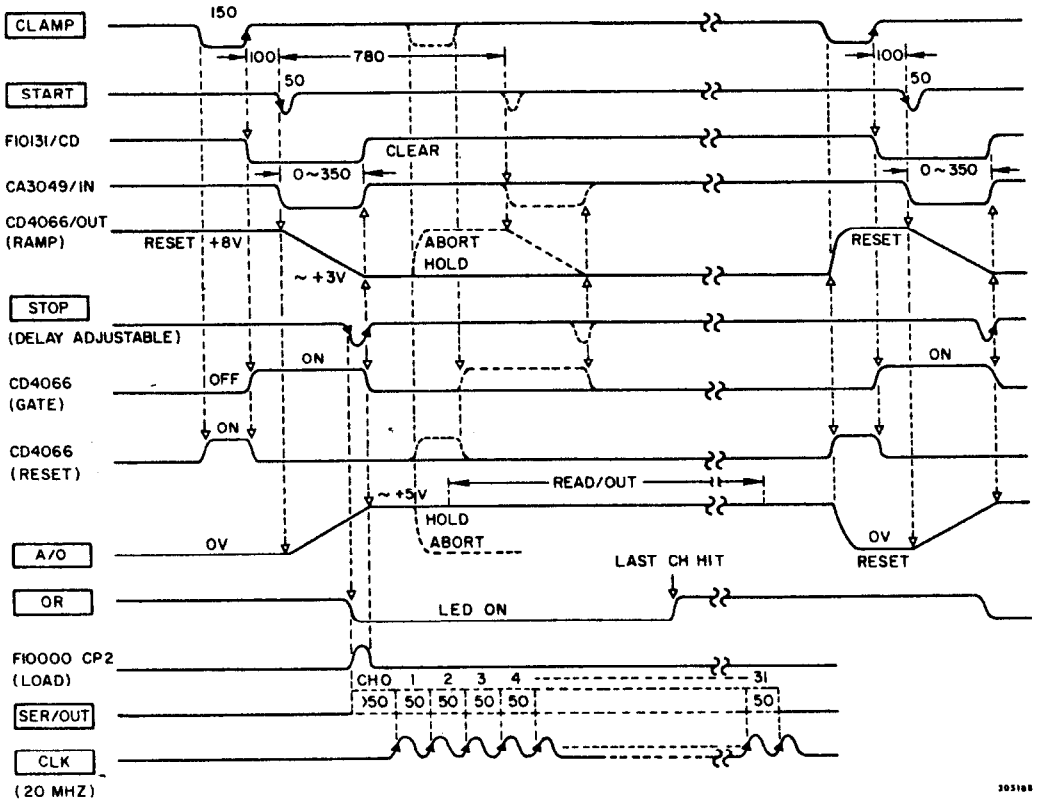

Fig. 4. TAC timing diagram.

The overall performance of the system depends upon the timing stability of the ECL preamplifier, receivers, and switches, upon the stability of the current source, and upon the offsets, hold stability and temperature stability of the analog section. It should also be noted that the nonlinearity of the chamber drift time itself may require a quadratic correction. All possible precautions have been taken to guarantee excellent stability of special supply voltages and current sources. The 4066 switch offsets are quite large when the switches are operated very fast (~100 millivolts) which is necessary to guarantee the fast reset capability. Thus an individual offset trim has been provided to match each channel to zero. Small drifts about zero are then compensated by the ADC processor and calibration system.

3.2 Analog Input Module

A second module has been designed to process 0-5 volt analog data from liquid argon shower counters. The input

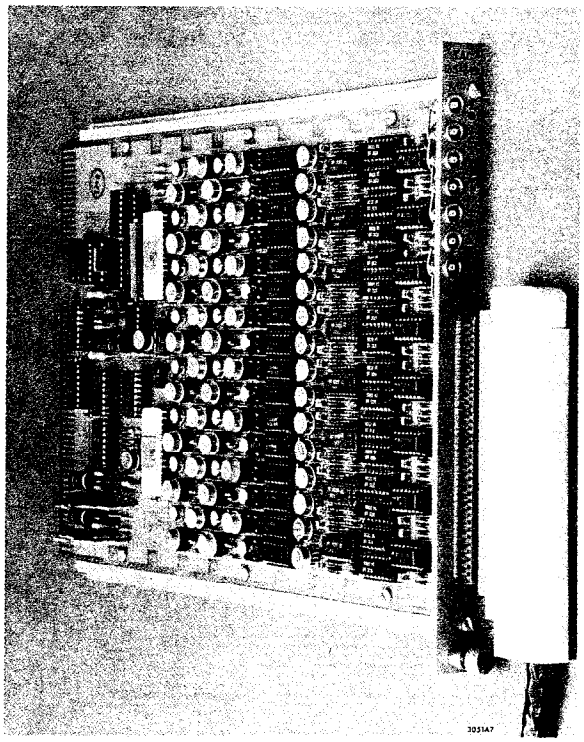

Fig. 5. (Photo) 32-channel TAC board.

data is in the form of a shaped bipolar pulse, with a time-to-peak of approximately 600 ns; the data is obtained from preamplifiers designed at the Lawrence Berkeley Laboratory.

The basic circuit is shown in Fig. 6. The FET switches are rearranged to produce a sampled signal which is positive with respect to ground. The multiplexing scheme is identical to that of the TAC circuit. A section of the detailed design is shown in Fig. 7, and the specifications are summarized in Table II.

Two modes of operation are possible. If high per-channel data rates are expected, a primary trigger decision will be obtained within about 150 ns of the beam crossing, and will be used to inhibit the RESET signal and enable the SAMPLE signal to the entire system. The fast reset will prevent signal pile-up. In the more usual case, where very low rates are expected on a given cell, the SAMPLE gate will be operated on every (delayed) beam crossing, and inhibited only after an event trigger signals that the current sample should be retained for further examination. In this mode, the RESET gate is not used, and the pedestal value will be established as the SAMPLE gate offset with no input data present.

Following the aforementioned secondary trigger decision, the data will either be processed by the autonomous controllers, or aborted so that sampling can recommence.

Table I. TAC Module Specifications

Number of channels	32
START input	MECL level differential pulse, ~50 ns width $Z_{in} = 100\ \Omega$
STOP input	50 ns wide MECL negative signal, delayed 0 to t_{max}[a] with respect to start signal
Current input to sample and hold (internal)	Adjustable 2 mA to 6 mA, corresponding to 350 ns to ~1 μs full scale
ANALOG output	0 to +5 V from $Z_{out} = 20\ \Omega$
Offset control	Individual channel ±950 mV, overall +500 mV
Linearity	Maximum deviation <2.5% peak Standard deviation <±0.5% rms
Crosstalk	<0.5% worst case (all channels full scale except for channel being measured)
Mux addressing rate	1 MHz max to settle to 0.3% 100 kHz max to settle to 0.05%
RESET	200 ns wide MECL negative signal
SERIAL INPUT	MECL, positive signal to 32-bit shift/register
SERIAL OUTPUT	MECL, positive signal from 32-bit shift/register
CLOCK	20 MHz MECL clock to 32-bit shift/register
OR	OR-ed NIM true output
OR LED INDICATOR	OR stretched to 30 ms
CAMAC commands	Read Ch 0 to 15: N.A.F(0).S1 Read Ch 16 to 31: N.A.F(1).S1
Power Supply Requirements	
+6 V at 0.4 A -6 V at 2 A +24 V at 0.2 A -24 V at 0.2 A	CAMAC crate power supply
+8 V at 60 mA -12 V to -24 V at 60 mA max	Separate system power supply
Packaging	
Module	Single width CAMAC module
Analog input connector	Edge card to mate with Viking 3VH36/1JN5
Analog output connector	LEMO
Stop signal connector	LEMO
Reset signal connector	LEMO
Serial/In signal connector	LEMO
Serial/Out signal connector	LEMO
Clock signal connector	LEMO
OR signal connector	LEMO
+8 V power	CAMAC P1 connector (Finger No. 1)
-12 V power	CAMAC P1 connector (Finger No. 9)
All other power	CAMAC P1 connector

[a] t_{max} is the range of the unit which is adjustable from 350 ns to 1 μs full scale.

3.3 Multiplexer Module

A trivial extrapolation is required to obtain a 32-channel multiplexer module; a section of the block diagram for one channel is shown in Fig. 8. The circuit can accept ±5 or ±10 volt signals, with input protection diodes connectable to ±6 or ±12 volts.

3.4 Autonomous Processor—ADC Module

This module is still in design so will be reported only briefly here; the details will be the subject of a later paper. Figure 9 shows the basic block diagram; Fig. 10 shows the flow diagram.

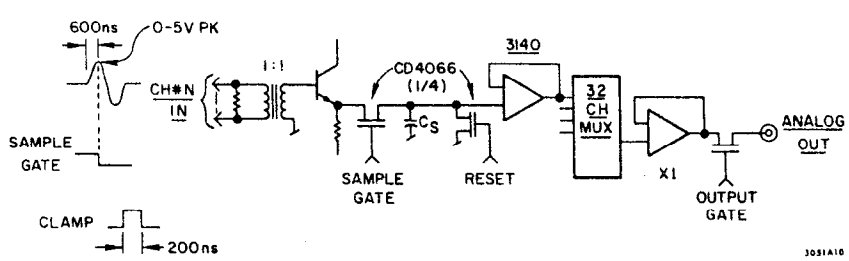

Fig. 6. Analog sampling circuit block diagram.

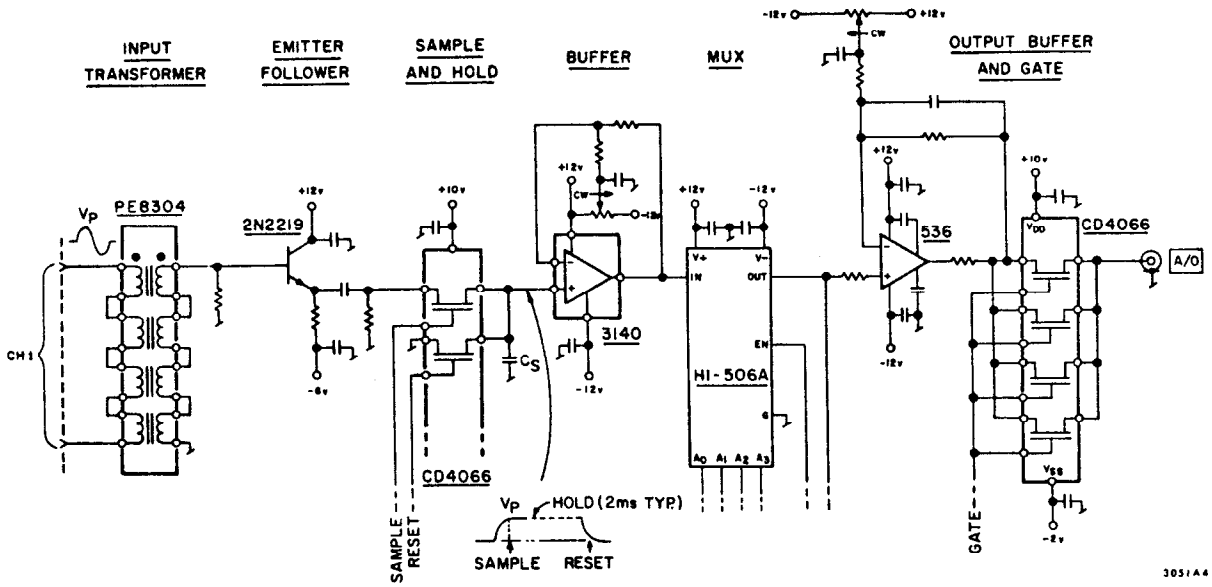

Fig. 7. Analog channel details.

Table II. Liquid Argon Sample and Hold Module Specifications

Number of channels	32
Analog input	0 to +5 V transformer coupled differential input. $Z_{in} = 120\ \Omega$
Analog output	0 to +5 V from 120 Ω
Gain	$A_v = 1$ nominal, noninverting, nonadjustable
Offset control range	±500 mV
Linearity	Integral 1.4%, differential 0.4% peak-to-peak
Slew rate	10 V/μs
Mux rate	~500 kHz max to settle to ±0.2% (approx.)
Sample gate input	TTL compatible—samples on positive edge
Sample aperture time	15 ns
Reset input	TTL compatible—reset when low
Reset time (abort)	150 ns to settle within 1 mV of normal offset
CAMAC Commands Required	
Read Chan 1-16: N.A.F(0).S1	
Read Chan 17-32: N.A.F(1).S1	
Power Supply Requirements	
+6 V at 0.1 A	0.6 W
-6 V at 0.7 A	4.2 W
+12 V at 0.9 A	10.8 W
-24 V at 0.2 A	5.3 W
	20.9 W max
Packaging	
Module	Single width CAMAC
Analog input connector	Edge card fingers to mate with Viking 3VH36/1JN5
Analog output connector	LEMO
Sample gate connector	LEMO
Reset (abort) connector	LEMO
Power and CAMAC command input	86 finger edge card CAMAC standard

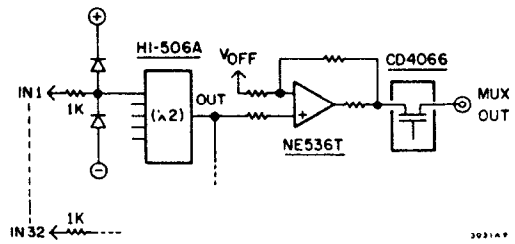

Fig. 8. Multiplexer channel block diagram.

The module design is dictated by event data rate requirements. The total time required for a valid event data acquisition cycle is expected to be about 20 ms from event to tape. This of course obviates the need for the fastest (all pipelined hardware) approach, and allows a 16-bit microprocessor (μP) to be used as the module controller. Hardware pipelining has been used in the sample-and-hold ADC circuits as well as in the μP. This results in good throughput as well as all-software ALU functions and simplified μP circuits.

All module operations will be performed via μP routines initiated through the CAMAC I/O or the front panel START. The 4K × 16-bit memory contains all constants, pointers, and data. Initializing the ADC consists of downloading data correction algorithm constants and pointers from the host CPU (Sigma 5) via CAMAC block transfer at a maximum rate of 2 μs/data word. A data word consists of 12 bits of data plus sign, plus 11 bits of address, stored in two 16-bit μP memory locations.

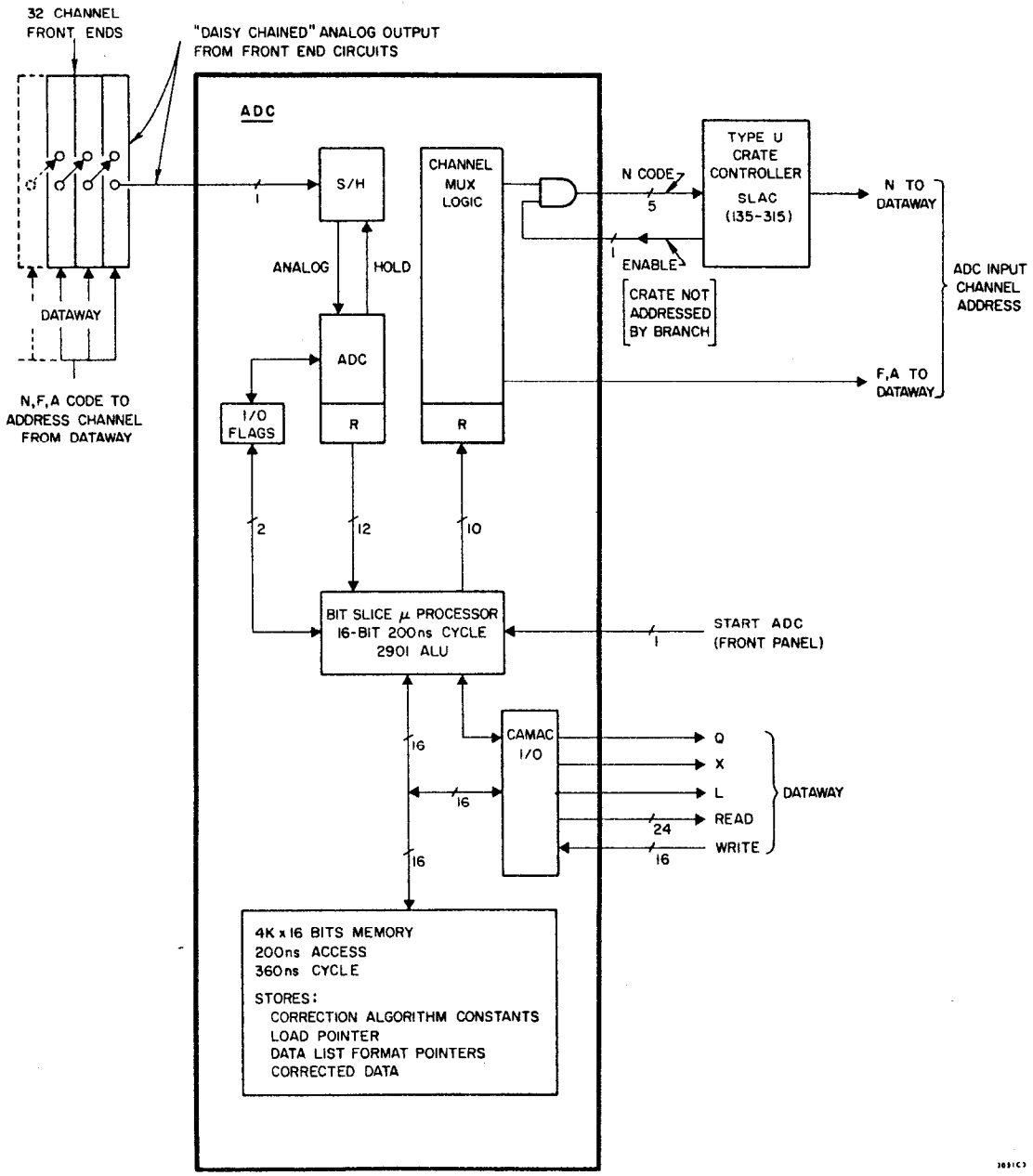

Fig. 9. Autonomous processor—ADC block diagram.

Upon receiving a start command from CAMAC or the front panel, the μP jumps to the scan routine in its microprogrammed ROM, initializes registers, etc. and executes the scan/correction algorithm for 640 channels. This consists of addressing each channel in turn, waiting for the ADC data, checking for good data and (a) correcting and saving it or (b) discarding it. Saved data is formatted by associating it with a calculated address (wire number, cell number, etc.) and storing in two 16-bit memory locations. At the end of this scan the module L-Flag is raised if data were saved. The saved data is read from the memory via CAMAC Q-scan block transfer at a maximum rate of 2 μs/data word.

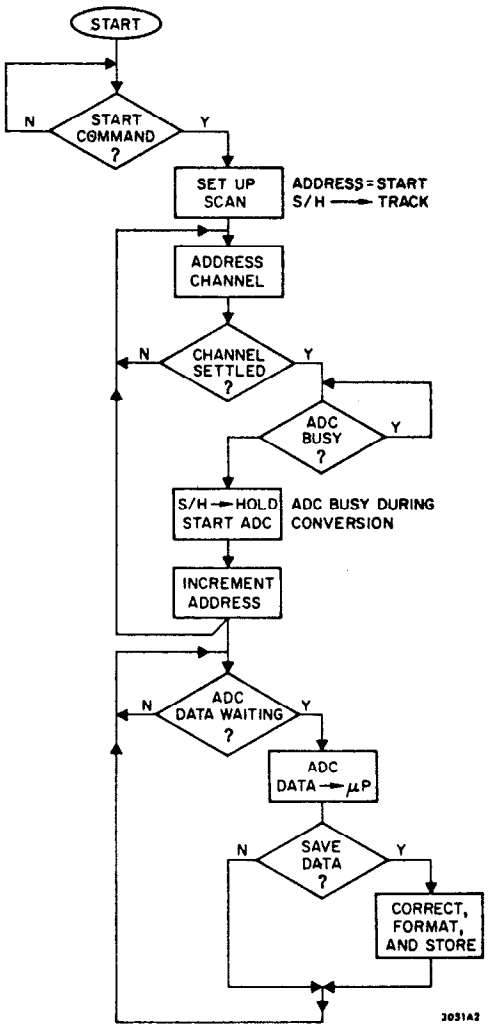

Fig. 10. Processor—ADC flow diagram.

4. Summary and Conclusion

A system using analog multiplexing to provide readout for drift chamber, liquid argon and dc analog data, has been described. The technique offers the advantages of low cost per channel for the resolution obtained; programmability of the autonomous processor for each subgrouping of modules; high front-end rate capability due to the abort feature; and dynamic drift correction and calibration capabilities. The autonomous processor concept also has the major advantage of unloading the calibration and constant storage tasks from the host processor, and in providing high overall speed due to the parallel processing configuration of the system.

5. Acknowledgments

The authors acknowledge the significant contributions made to the system concept by M. Breidenbach of the Mark II Detector Project, by many helpful discussions with D. Horelick and J. Kieffer, and the ongoing contributions to the autonomous processor work by D. Porat, E. Frank, and L. Shustek.