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CC80-A MICROCOMPUTER CRATE CONTROLLER FOR CAMAC*

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Abstract

A microcomputer crate controller has been developed for use in CAMAC based instrumentation, control, and data processing systems at the Stanford Linear Accelerator Center. This unit may be used in multicrate branch highway systems to provide local processing capability within each crate, or in a single crate to form a stand-alone CAMAC system.

Introduction

Intelligent CAMAC modules, capable of programmable data processing and control tasks, are very useful in many systems applications. The availability of powerful microprocessor circuits and low cost semiconductor memory has spurred the development of a variety of such modules. At the device or single-function module level, the microprocessor may be used to replace hardwired logic, or provide dedicated data processing capability. For example, a multiplexed ADC module with a microprocessor can have programmable scanning modes and execute data normalization and formatting algorithms. At the CAMAC crate level an intelligent crate controller extends this processing power to all modules within its crate.

Each device controlled through, or function implemented with a module in the crate can be operated under microprocessor software control. Requirements for a small system can be satisfied with a single stand-alone CAMAC crate, where the microprocessor crate controller functions as the host computer. Larger multicrate systems may employ intelligent crate controllers for distributed local processing, in order to reduce branch highway traffic and reduce system host computer loading.

This paper describes the design and development of a general purpose microcomputer crate controller. Detailed specifications are given and application examples are used to demonstrate different features of the module.

General Module Description

CC80 is a CAMAC crate controller packaged in a 3-unit wide module. The prototype is shown in Figs. 1 and 2. It must reside at crate locations 23 through 25. All remaining 22 crate locations may be used for any arrangement of CAMAC compatible modules. The 3 pc boards of the unit contain an 8 bit microprocessor with a type 8080 CPU and 16 K words of memory (8 K RAM and 8 K EPROM), interface logic for a microprocessor extension port, a manual front panel facility, a serial port, the crate dataway and the parallel branch. Figure 3 shows a functional block diagram.

There are two basic modes of operation. The parallel branch mode makes the crate controller transparent to the branch driver and allows the system host computer normal control of all modules in the crate including the microprocessor itself. The microprocessor mode puts the crate under control of the microprocessor. All dataway operations may be performed. Attention of the parallel branch host computer is gained by posting a LAM. The asynchronous serial port may be used to drive a TTY or a CRT terminal, to connect to a modem, or to implement a custom, high speed serial branch.

Most control logic is realized in firm-ware, minimizing hardwired functions and optimizing application flexibility. The CC80 module utilizes approximately 200 DIP packages with integrated circuits and discrete components. The cost of parts for the prototype unit was $3000.

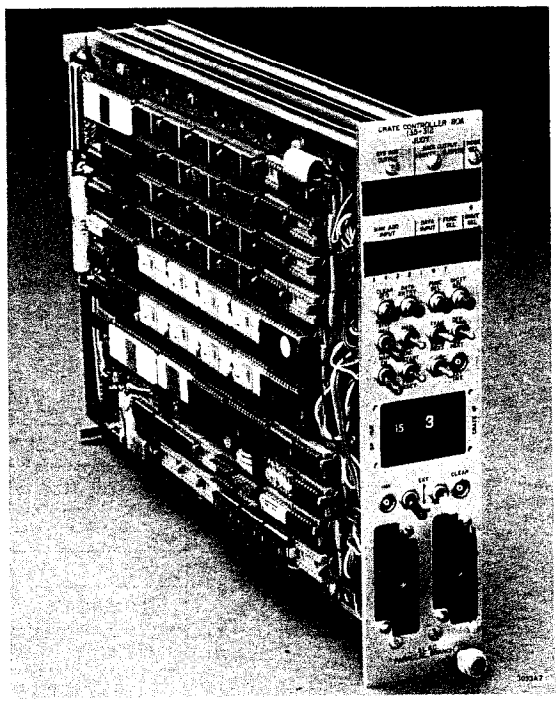

Fig. 1. CC80 prototype, front panel and microprocessor board.

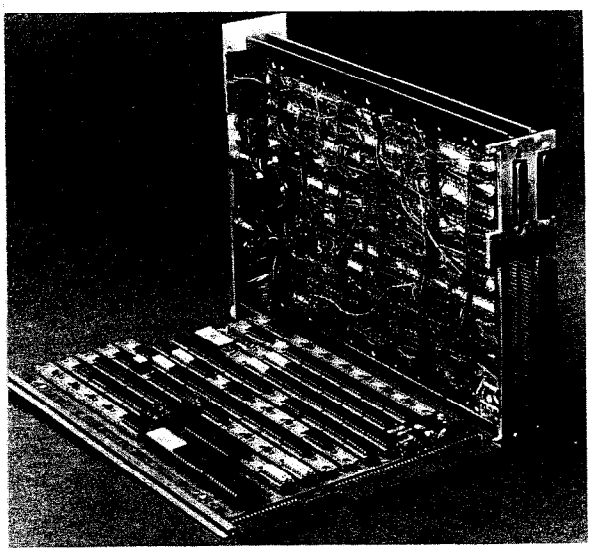

Fig. 2. CC80 prototype, rear panel and CAMAC interface board.

Microprocessor

The 8-bit microprocessor utilizes a type 8080A CPU. This provides a minimum execution clock cycle time of 350 ns. The read-write memory has a capacity of 8 K words of 8-bit length. Operation is static with 225 ns access time and 400 ns cycle time. Read-only memory size is 8 K words with 450 ns worst case access time. Memory contents are

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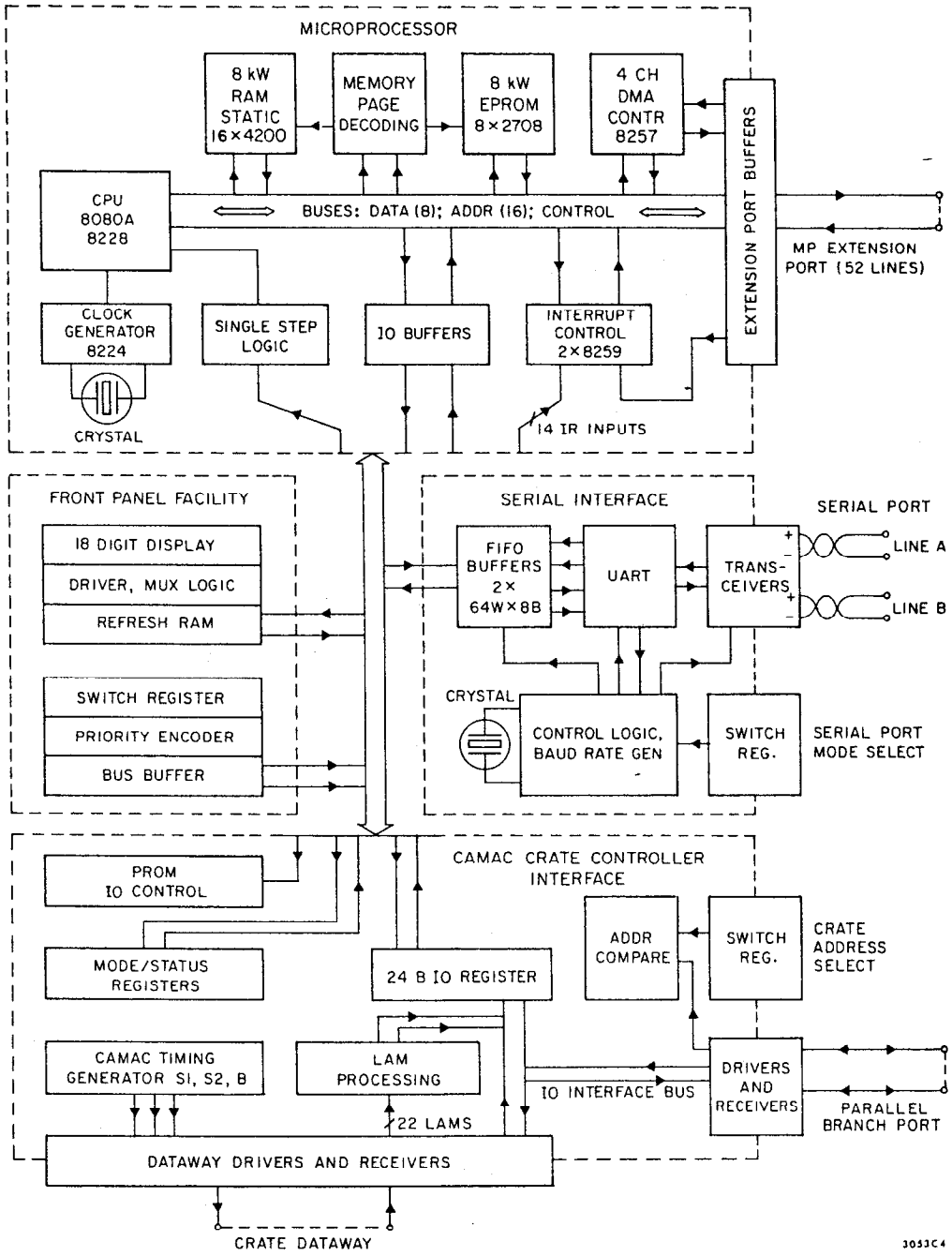

Fig. 3. CC80 functional block diagram.

erasable with UV light and electrically reprogrammable. Memory address control includes a bank switching bit to allow expansion above 64 K words of memory.

The CPU interrupt structure has 15 input levels with masking capability and several programmable modes of operation (see Intel 8259 description).[1] One interrupt line is available for an external input through a front panel coax connector.

A programmable DMA controller provides a 4-channel DMA interface (see Intel 8257 description).[2] The DMA channel connection is made through the microprocessor extension port. Consecutive DMA cycles are possible within 4 clock cycles each (or 1.4 μs per word, burst mode). The worst case completion time of a peripheral service request, which includes waiting for HLDA (hold acknowledge) from the 8080 CPU, will be 11.5 clock cycles (~4.0 μs).

The microprocessor extension port is accessible through the 52 contact auxiliary rear panel connector at crate location 23. The port allows a general extension of the microprocessor system to add memory, input-output functions, DMA channels and interrupt levels. The port contains the 8-bit MP data bus, the 16-bit MP address bus and a collection of control signals related to CPU, DMA and interrupt functions.

A signal assignment and description for the extension port is given in Table I.

A manual front panel input-output facility is provided for software diagnostic. It consists of a software driven 18-character hexadecimal display and an array of switches. The facility may be used by programmers to display the contents of the CPU address bus, data bus, all internal CPU registers, to access at random any location in memory and display or alter its contents. Controls are available to single-step the CPU, to perform a RESTART at address location zero, and to force a hardware power RESET. Front panel diagnostics may, as a software option, include specific CAMAC related tests such as read and write operations of 24-bit words.

Table I. MP Extension Port Signal List

Pin No.	Direction	Signal Name	
1-8	IO	Data Bus D0-D7 (DB)	
9-24	IO	Address Bus A0-A15 (AB)	
25	I	DB Direction Control	
26	I	DB Disable Control	
27	IO	$\overline{\text{MEMR}}$	System Control
28	IO	$\overline{\text{MEMW}}$	
29	IO	$\overline{\text{IOR}}$	
30	IO	$\overline{\text{IOW}}$	
31	IO	$\overline{\text{INTA}}$	
32	I	Ready EN	CPU Control
33	I	$\overline{\text{Single Step}}$	
34	O	$\overline{\text{Wait}}$	
35	O	Reset	
36	O	$\overline{\text{MPØ2}}$	
37	I	$\overline{\text{Hold Req}}$	
38	O	HLDA	
39	I	AB Direction/Disable Control	
40	O	TC	4 Channel DMA Control
41	I	DRQ 0	
42	O	$\overline{\text{DACK 0}}$	
43	I	DRQ 1	
44	O	$\overline{\text{DACK 1}}$	
45	I	DRQ 2	
46	O	$\overline{\text{DACK 2}}$	
47	I	DRQ 3	
48	O	$\overline{\text{DACK 3}}$	
49	O	CAS 0	Interrupt Extension
50	O	CAS 1	
51	O	CAS 2	
52	I	IRE	

CAMAC Interfaces

CC80 is equipped with interface circuitry for the parallel branch and the crate dataway.

The parallel branch interface is compatible with the standard SLAC branch.[3] The controller module may be used anywhere in a multicrate system except at the parallel branch driver location. To accommodate the autonomous nature of the microprocessor, 2 handshake signal lines have been added to the branch (crate controller busy, branch crate demand).

The crate dataway interface conforms to standard CAMAC specifications.[4] All drivers utilize 3-state outputs with external pull-up resistors. All output lines can be deactivated under program control. Hence any other module in the crate may take control of the dataway.

In the microprocessor mode the CPU loads a set of registers with module address, function code and data. Then a timing generator performs the dataway cycle. The timing generator offers four program selectable timing sequences as shown in Fig. 4. One sequence is a standard 1 μs dataway cycle. Other sequences may be programmed to synthesize custom timing cycles with a 50 ns least count and approximately 13 μs maximum duration based on a 20 MHz master clock.

A general WRITE cycle requires 5 processor output operations plus 5 internal processor data transfer instructions plus a dataway cycle, or approximately 41 μs. A general READ cycle is equal in duration.

In the parallel branch mode the controller is transparent and operates at full CAMAC speed after a setup procedure of typically 22 μs. For consecutive branch cycles the setup overhead is incurrent only once at the start.

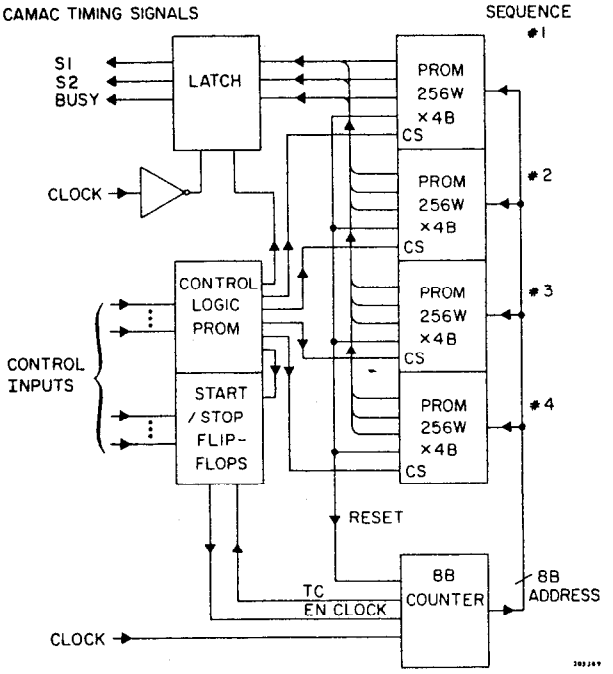

Fig. 4. CAMAC timing generator.

CC80 provides the user with multifunctional LAM handling (Fig. 5). The parallel unprocessed LAM word can be read as a data word by the parallel branch or the processor. For the 8080 CPU this is a 3 byte INPUT operation. A 24-bit LAM sampling register synchronizes the LAM input lines.

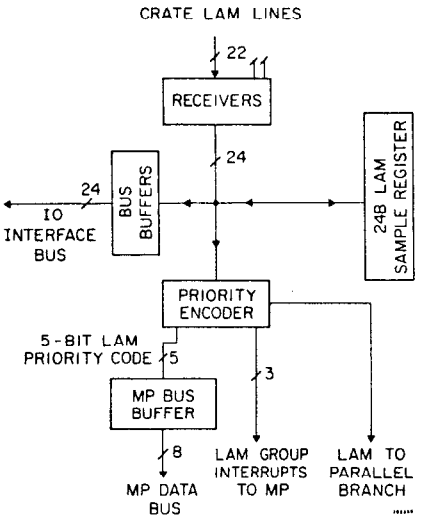

Fig. 5. LAM processing.

A hardware priority encoder generates a 5-bit LAM address and 3 LAM group interrupt signals for the processor. After a LAM interrupt has been posted the processor has a choice of the following actions in response:

a) Read 3 bytes of unprocessed LAM lines as data;
b) Read 1 byte of unprocessed LAM lines as data as called for by group interrupt;
c) Read 1 byte status input word containing the encoded LAM address.

Finally, all crate LAM lines are available externally at the auxiliary connector of the crate slot 25 pc board of the CC80

module for independent processing. All portions of internal LAM handling and processing may be enabled or disabled under program control.

Serial Port Interface

An asynchronous serial IO port to the microprocessor is implemented with a UART and two FIFO buffer functions. The port may be used to connect a teletype (TTY), a CRT terminal, a modem, or a custom serial branch of a multicrate system. A mode and transmission control logic allows the following selections by means of a front panel thumbwheel switch:

Port ON/OFF;
Serial Branch Mode: -at full speed;
-at partial speed;
-with/without error checking;
TTY Differential Line Mode at 4 standard baud rates;
TTY Single Line Mode at 4 standard baud rates.

Full transmission speed is 12.5 K baud which results in a 1K rate of 8-bit words. All standard baud rates are crystal controlled and cover the range from 50 to 9600 baud. The processor IO operations through the serial port require 8 μs per 8-bit word. The FIFO buffers allow block transfers of 64 words of data in each direction.

In other words the processor can load the FIFO buffer at 8 μs/word with a block of 64 words, branch to some other task, and return for the next data block once the serial transmission is completed. Similarly the input FIFO buffer may asynchronously accumulate up to 64 words of data before the processor starts to read the buffer at full speed.

The port may be used to implement a custom serial branch for a multicrate CAMAC system by defining a suitable transmission protocol in software. Within such a system the CC80 module may be used both as a host computer driving the serial branch and as a crate controller along the serial branch highway. Connections to the serial port are made with a standard terminal equipment type connector at the rear panel of the module. Parallel input-output connections are available at the connector for TTL single line, TTL differential line, RS-232-C, and TTY current loop interfacing standards.

Summary and Conclusions

A prototype module of the CC80 unit has been fabricated and is undergoing extensive tests. Design and development work is in progress on a modification of the serial port interface, a printed circuit board implementation of the entire crate controller module, and 2 types of memory extension modules to be used with the microprocessor extension bus. The modified serial port interface will utilize a 200 K baud UART to provide a corresponding full speed data transmission rate in the serial branch mode. The two memory extension units will be single-width CAMAC modules with 24 K words of RAM and 48 K words of EPROM respectively.

The flexibility of the CC80 module is demonstrated in the 3 different general system application examples shown in Figs. 6, 7 and 8.

In stand-alone systems, CC80 is used as host computer and the serial port allows connection of an interactive operator terminal. In multicrate systems, CC80 controllers are employed to add distributed processing at the crate level.

The first proposed application of a CC80 crate controller is the new liquid hydrogen target control system shown in Fig. 9. A single stand-alone CAMAC crate with a microprocessor crate controller monitors and controls the various transducers, detectors and devices of the hydrogen target. A CRT terminal with keyboard is provided for operator interaction. The estimated size of software is 4 K words, with 2 K words devoted to the basic CAMAC operating system of the MP crate controller.

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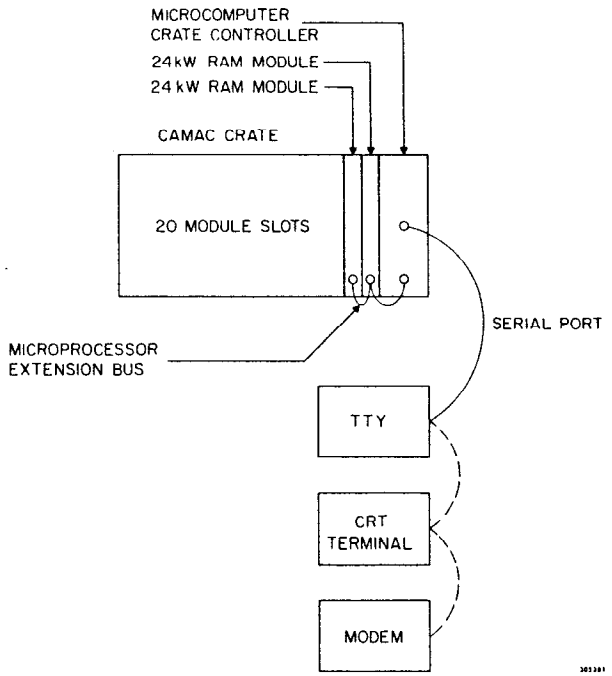

Fig. 6. Stand-alone CAMAC system with 65 k words memory and operator terminal or modem.

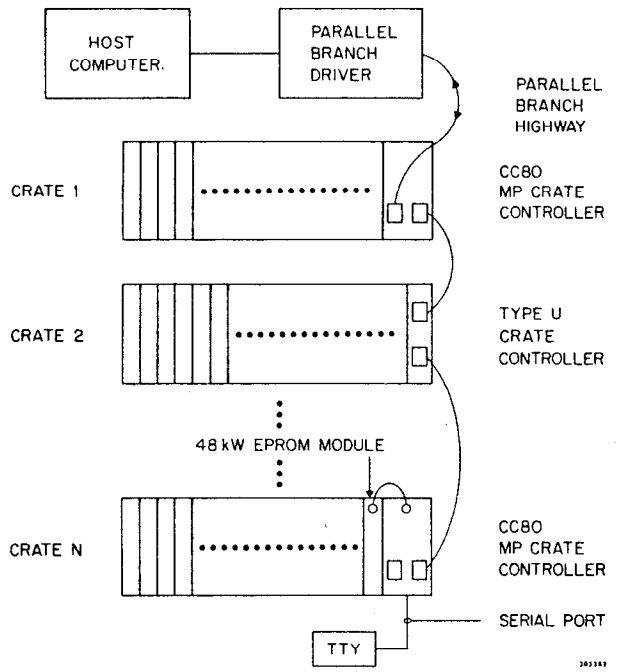

Fig. 7. Parallel branch multicrate CAMAC system with distributed processors.

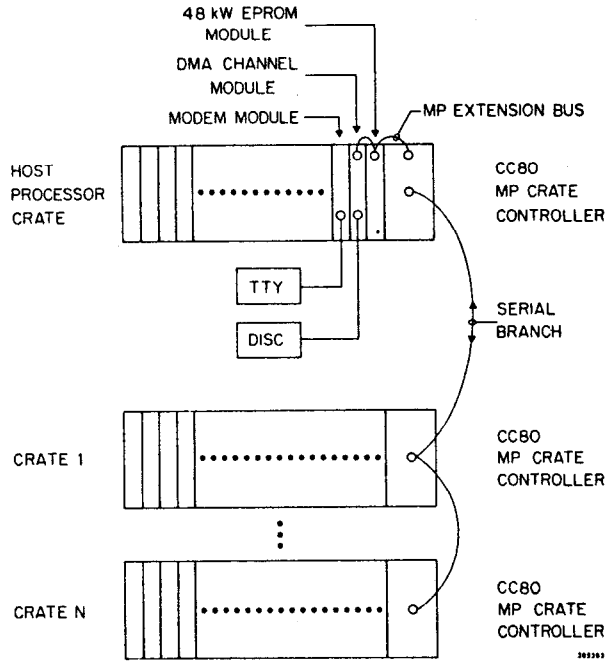

Fig. 8. Custom serial branch multicrate CAMAC system with distributed processors.

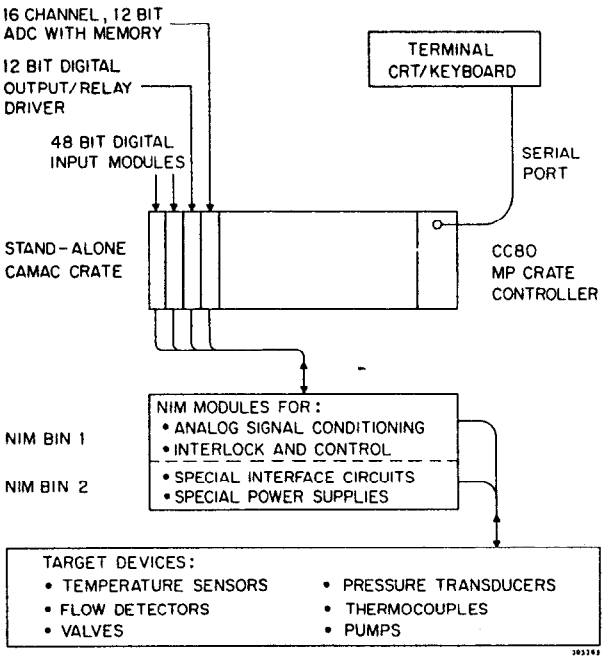

Fig. 9. Liquid hydrogen target control system application.

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