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A LOW COST PHOTOMULTIPLIER HIGH-VOLTAGE READOUT SYSTEM†

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ABSTRACT

A low-cost high-voltage readout system has been implemented to offer stand-alone digital readout capability as well as fast data transfer to a host computer.

The system is flexible enough to permit use of a DVM or ADC and commercially available analogue multiplexers.

DESIGN PHILOSOPHY

The Large Aperture Solenoid Spectrometer (LASS) at Stanford Linear Accelerator Center (SLAC) requires monitoring over 300 voltages. This data is recorded on magnetic tapes along with the event data. It must also be displayed so that operators can easily monitor and adjust the voltages.

It is obvious, due to the high event data rate, that it would be too time-consuming for the data acquisition computer to step through all analogue signals, record them and display them at the experimenter's discretion. On the other hand, it is too expensive to have an ADC for each signal.

The system we designed is housed in a CAMAC crate and the goal towards low cost and flexibility was reached by designing three modules: a scan controller, an ADC and a memory buffer.

Any sequentially addressable multiplexer can be used. Either a DVM or ADC with a remote control input is part of the system.

Three independent systems are in use at SLAC: two at LASS and one at the Stanford Positron Electron Asymmetric Ring (SPEAR).

SYSTEM OPERATION

A typical configuration is shown in Fig. 1. In this application we use high speed 16-channel single-ended CAMAC multiplexers manufactured by Standard Engineering Corporation. The channel address of each multiplexer is controlled from the state of a 4-bit counter, in each module, which can be incremented by an external pulse via a front panel LEMO connector (Scan Trigger In). Each time the module receives this pulse, the multiplexer steps to the next successive channel. Upon reaching the last channel, a flip-flop (Next Module Flip-Flop) is set, the following pulses are then routed to the Scan Trigger Out LEMO connector and the analogue multiplexer is put into a disabled state. The multiplexer output is wired to two 3-pin LEMO connectors which are bussed together (Analogue In and Analogue Out). A CAMAC Clear (C*S2) resets the channel address and the Next Module Flip-Flop to zero, which in turn enables the multiplexer. With these features, the channels of several multiplexer modules can be stepped through sequentially with a single control signal by daisy-chaining the Scan Trigger Out of one module to the Scan Trigger In of the next one and bussing the Analogue In and Out together. However, after the Clear pulse, all the multiplexers are enabled and their outputs are shorted together. Thus only one module should have an input voltage to the first channel and in our case this is a standard reference voltage.

The overall analogue output is fed to a 12-bit ADC. This module, built at SLAC, uses a fast hybrid ADC circuit with a unipolar range of 5 volts. The front end is designed to

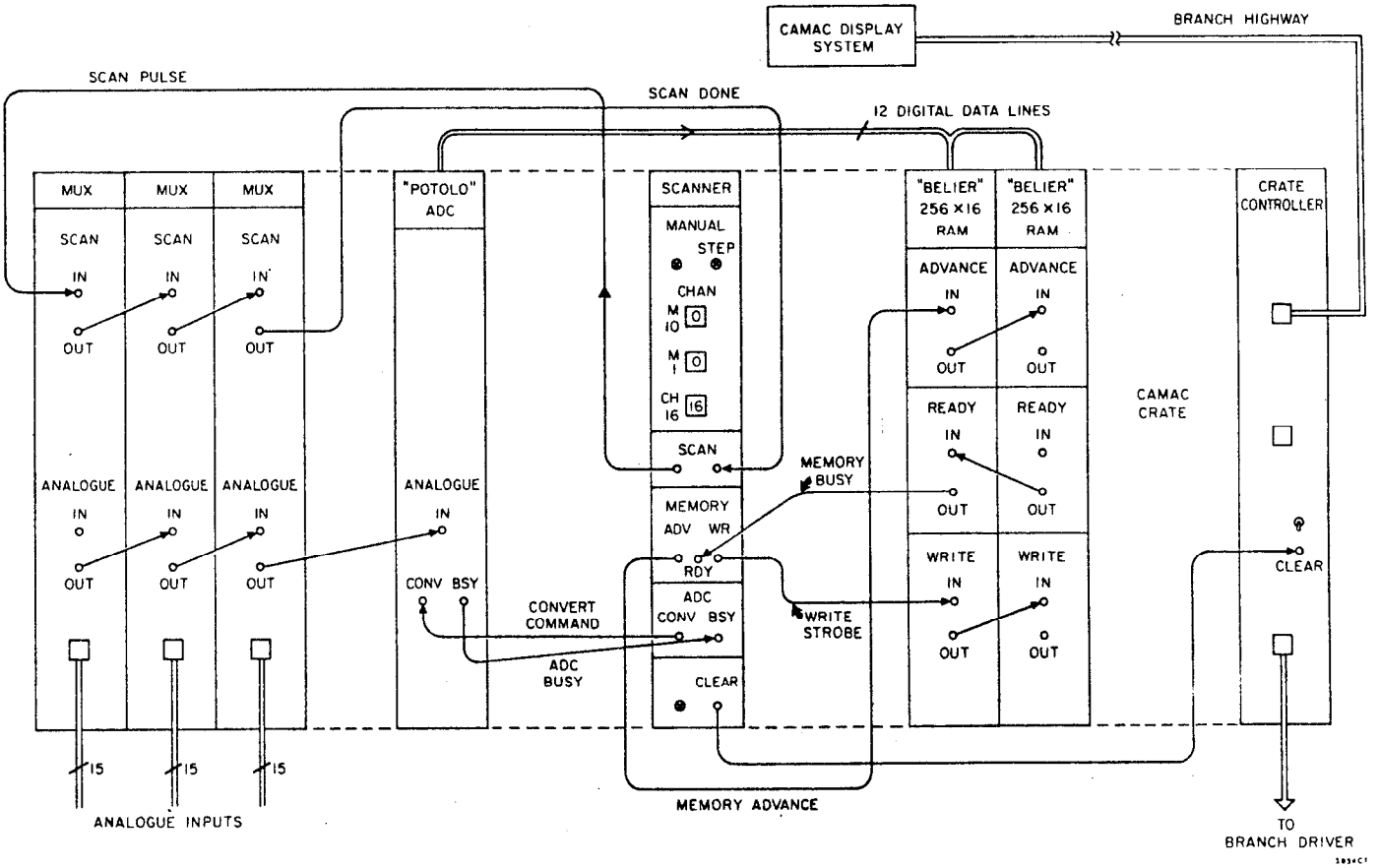

Fig. 1

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present a high input impedance and accept either positive or negative voltages using an absolute value amplifier. The resolution is within 0.1% with no noticeable drift.

The digital output from the ADC is fed to a CAMAC memory buffer module via a rear connector. This unit contains 256 words of 16 bits and was designed as a general purpose module for the facility. For simplicity only one mode of operation is described herein. The memory location is specified by either one of two address registers, called the Write Address Register and the Read Address Register. The Write Address Register is reset by a CAMAC Clear and incremented by a pulse applied to a front panel connector. The Read Address Register is set by a CAMAC Write Command (N*F(17)*A(0)) and is incremented with each CAMAC Read (N*F(0)*S2). The memory can thus be read by a Stop Mode Block Transfer.

The data presented to the memory input port is strobed when a Write signal is applied to a front panel connector. When the Write Address Register overflows, the following Advance and Write signals are routed to the Advance Out and Write Out LEMO connectors, respectively. Thus, similar to the multiplexers, the memory modules can be daisy-chained for expansion in increments of 256 words.

The system is controlled by the scanner module. It controls the time sequence of signals in the system so that the multiplexers are stepped through their channels and the memory address incremented, the analogue to digital conversion started, and the data strobed into memory when ready. The last multiplexer in the chain passes the Scan Trigger pulse back to the scanner when its Next Module Flip-Flop is set; it is interpreted as a Scan Done pulse. The scanner then generates, via a LEMO connector, an external CAMAC Clear to the Crate Controller to reinitialize the multiplexers and the memory Write Address Register. The scanning process then resumes, starting with the first channel and first memory location. Therefore each memory location contains the digital voltage value corresponding to a unique analogue channel. To provide more flexibility, the scanner can also be controlled manually or by a host computer via CAMAC. A single channel selected in manual mode can be continuously monitored because the memory location is continuously updated. In the free running mode, the channels are scanned at a rate of about 1 msec per channel. Thus, even with over 300 channels presently in the LASS system, each memory location is updated more than twice a second.

READOUT OPERATION

Computer Readout

The host computer may obtain the voltages data at any time by reading the content of the memory buffer module via the Dataway in a block transfer STOP mode. During readout operation the scanner is disabled by a memory NOT READY signal. When reading is completed, the scanner resumes where it left off since the memory Write Address Register is separate from the Read Address Register.

Digital Readout

The display used is provided by a master controller originally designed to display data from blind scalers.[1] It generates sequential CAMAC addresses and sends them onto the branch highway; the returning parallel binary data is converted to BCD data and sent together with BCD channel address to quad display units. The scan is discontinued and the branch address inhibited when the computer branch driver asserts a single disable line. When such a unit is used the host computer should reset the Read Address Register to zero (F(11) command to the memory module) before reading the content of the buffer.

The scale of the ADC amplifier has been set so that a voltage of 8.192 volts produces 5.000 volts at the input of the hybrid circuit. Thus the digital output is 4096, decimal, which, when shifted one bit to the left at the module output, gives 8192. The sign bit is put into the least significant bit to the memory. Therefore a positive voltage appears as an even number and a negative voltage as an odd number on the display since a sign display is not provided.

CONCLUSION

The reliability of this system has been very good and this method of displaying the phototube voltages was easily accepted by the LASS users. The system installed at SPEAR is similar to the one described above but uses 32 channel multiplexer modules manufactured by Joeger Enterprises, Inc.

The cost of the system, including the cost of the CAMAC Crate and Controller, is around $25 per channel for a 256-channel system, while it can be as low as $20 per channel for a 512-channel system.

The ADC could be replaced by a DVM in systems that require improved precision but it would slow down the scan rate. The multiplexers could be replaced by almost any multiplexer using a stepping pulse or by a multiplexer requiring an address with a simple adaptor module.

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REFERENCE

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