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Design of ePixM, a fully-depleted monolithic CMOS active pixel sensor for soft X-ray experiments at LCLS-II

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Abstract: The LCLS-II Free Electron Laser (FEL) will produce X-ray pulses with a repetition rate of up to 1 MHz and energies between 250 eV and 5 keV. Experiments conducted at LCLS-II will require 2D imaging detectors with a unique set of features, such as high-spatial resolution, low-noise performance, high-dynamic range and high-frame rates up to 1 MHz. We present the design of ePixM, a fully-depleted monolithic CMOS detector tailored for soft X-rays applications at high-repetition rates FEL. It consists of an array of 384×192 active pixel sensors, with a pixel size of 50×50 μm^2 and a total sensitive area of 2×1 cm^2. ePixM has been designed in a 150 nm CMOS technology on high-resistivity substrate to achieve full depletion of the substrate. Each pixel includes a Charge Sensitive Amplifier (CSA) with gain auto-ranging capability and a noise-shaper performing Correlated Double Sampling (CDS). A novel technique named correlated pre-charging removes the excess noise introduced by the gain-switching mechanism. The performance of the design has been evaluated through post-layout simulations. The Equivalent Noise Charge (ENC) of 11.3 electrons enables single-photon detection at X-ray energies down to 250 eV, and the dynamic range exceeds 10^3 photons at 500 eV thanks to the auto-ranging circuitry.

Keywords: X-ray detectors, Instrumentation for FEL

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Contents

1 Introduction

Over the last decade, X-ray Free-Electron Lasers (FELs) have found countless applications in many scientific fields [1]. The Linear Coherent Light Source (LCLS) is an X-ray FEL located at SLAC National Accelerator Laboratory. The ongoing upgrade of LCLS, named LCLS-II, will produce a uniformly-spaced train of X-ray pulses with a repetition rate of up to 1 MHz [2]. In order to take full advantage of the unique capabilities of LCLS-II, many beamlines will rely on 2D imaging detectors with a pulse-by-pulse readout at frames-rates up to 1 MHz. Because of the high brilliance of FEL sources, each pixel must be able to process up to 10^4 photons per pulse. At the same time, single-photon resolution is needed for photon energies as low as 250 eV, pushing the limits in terms of low-noise performance down to a few electrons.

Combining these specifications in a single detector presents significant design challenges and existing instrumentation does not meet all the requirements. Detectors developed for the European XFEL take advantage of its characteristic bunching scheme to achieve frame rates up to 4.5 MHz, but only in "burst-mode": a local memory is implemented in the front-end electronics either before [3, 4] or immediately after the digitization stage [5], allowing users to acquire only a limited amount of frames at the highest frame rate. Other detectors designed for storage rings or FEL operating at lower rates cannot meet the required performance in terms of noise and/or frame rate [6, 7]. Therefore, a large R&D effort has been started at SLAC in order to develop the new generation of ePix detectors [8] and to satisfy the needs of future experiments at LCLS-II.

We present the design of ePixM, an Application Specific Integrated Circuit (ASIC) tailored for soft X-ray experiments at LCLS-II. Section 2 reviews the benefits of monolithic CMOS detectors while section 3 introduces the ePixM architecture. The active circuitry implemented in each pixel and the correlated pre-charging are described in sections 4 and 5, respectively, followed by simulation results in section 6. A summary and a brief outlook on future plans are given in Section 7.

2 Fully-depleted monolithic CMOS detectors

Since early 1990s, monolithic CMOS active pixel sensors have found many applications in imaging and high-energy physics (HEP) applications [9]. Monolithic CMOS detectors combine the sensing element, typically an array of diodes, and the readout electronics on the same die. In early developments, charges generated by incoming radiation or particles are collected by diffusion [10]. The long charge collection time due to the diffusion mechanism increases the probability of charge recombination before the signal is read out by the front-end electronics. On the contrary, in fully-depleted CMOS sensors[1] charges are collected by drift [11], resulting in faster charge collection times, higher charge collection efficiency and lower charge-sharing among neighboring pixels. These detectors have been made possible by modern CMOS process with high-voltage options and/or high-resistivity substrates, which enable full depletion of the sensitive layer [12].

Fully-depleted monolithic sensors are an attractive option for several reasons. First, having the diodes array and front-end electronics on the same die eliminates interconnection capacitances. Second, such die can be connected to a separate ASIC containing fast analog-to-digital converters (ADC) through conventional bump bonding techniques. This approach increases the parallelism of the system, which is of paramount importance to achieve high frame rates, without the need of complex packaging technologies such as 3D interconnections. Lastly, it allows designers to independently optimize the analog front-end and the mixed-signal back-end, e.g. by choosing different CMOS processes.

3 ePixM pixel architecture

ePixM is a fully-depleted monolithic active pixel sensor designed on a commercial 150 nm CMOS technology on high-resistivity substrate (>2 kΩ · cm). A pixel cross-section and layout are shown in figure 1.

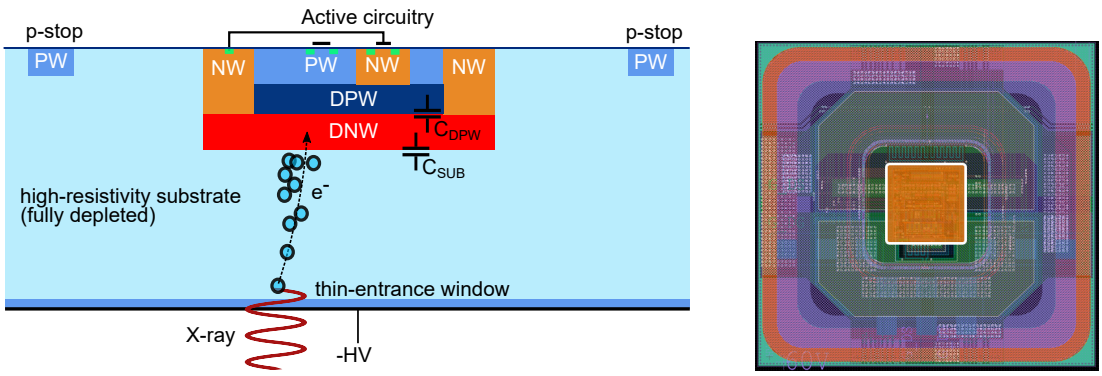

Figure 1. Left: cross-section of one pixel (not in scale). Right: layout of one pixel with a size of 50×50 μm^2. The circuitry occupies an area of approximately 10×10 μm^2 (highlighted in the middle).

The substrate is depleted by applying a negative high-voltage from the back-side. The depth of the depletion region depends on the exact resistivity of the Si wafers substrate and on the maximum

[1] Another term found in the literature is Depleted Monolithic Active Pixel Sensors (DMAPS).

voltage which can be applied before causing break-down of the front-side structures. For a resistivity of 4.7 kΩ · cm and an applied potential of −120 V we have estimated a depletion depth of 236 µm, a value which matches well with previous measurements reported in the literature [13]. Depending on the measured depletion depth, wafers will be thinned and then processed at SLAC to form a thin-entrance window on the back-side, a crucial step in order to achieve high quantum efficiency for low-energy X-rays [14].

The active circuitry is implemented in p-/n-doped wells (PW/NW), which are connected to analog ground/supply. The circuitry is enclosed by a deep n-well (DNW) implant, which shields the transistor wells from the depletion region. The DNW also acts as collection node for charges generated in the sensitive volume by incoming radiation. An additional deep p-well (DPW) is required to isolate the DNW from the NW. The total detector capacitance is determined by the sum of two contributions. The first one, C_{SUB}, is due to the reverse-biased junction between the DNW and the p-doped substrate and its value decreases for higher depletion depths. The second one, C_{DPW}, is formed by the DNW/DPW junction and can be detrimental for the noise performance: noise due to switching activity of the circuitry in the PW can couple to the DNW node through such capacitance.

P-stop structures featuring metal overhangs isolate each pixel from the neighboring ones. All the substrate junctions have been drawn with rounded edges to reduce the electric field at the corners and increase the break-down voltage. The diode matrix and the chip periphery (also enclosed by a large DNW) are surrounded by guard rings to minimize the leakage current of the sensor. Different guard rings designs have been submitted together with the full-scale ASIC and will be characterized before and after irradiation.

4 Pixel circuitry

The architecture of each pixel is shown in 2. Because all transistors are implemented inside the DNW, minimizing the area of the active circuitry is critical in order to reduce the detector capacitance and meet the requirements in terms of noise performance. The pixel circuitry occupies an area of 10×10 µm^2, as shown in figure 1, and draws 10 µA of current. The input node (DNW) is DC coupled to the input of the Charge Sensitive Amplifier (CSA). A test mode circuitry allows us to inject a known input charge through C_{Inj} for calibration purposes.

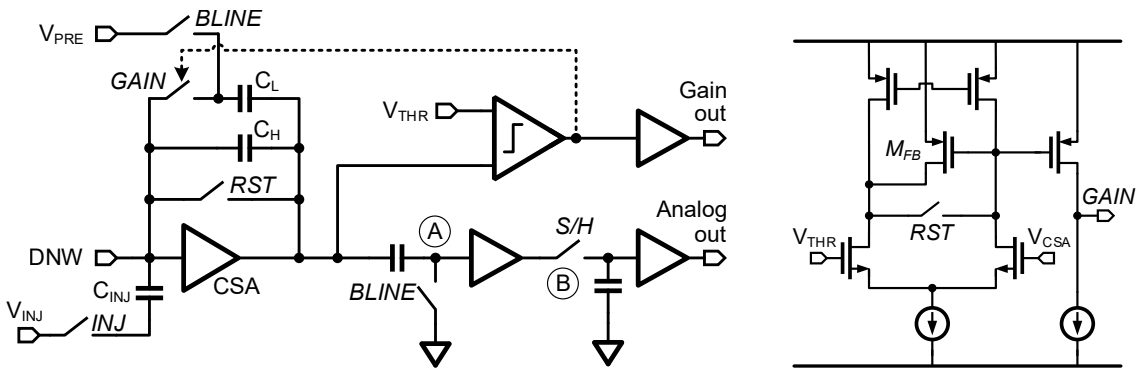

Figure 2. Left: schematics of the circuitry in one pixel. Right: schematics of the comparator.

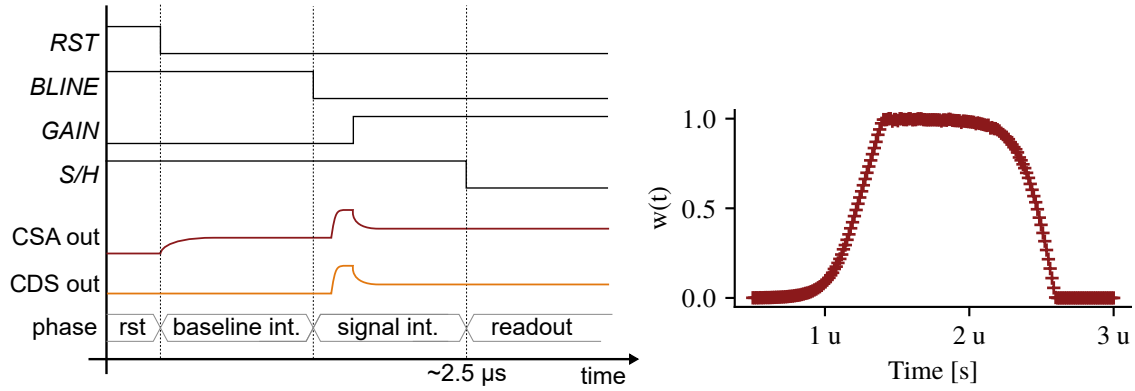

Figure 3. Left: Timing diagram (not in scale) showing the operation of the pixel in the case the gain is switched from HG to LG during the signal integration phase. Right: Normalized noise weighting function.

Gain-switching. Two different gain-settings are possible. A readout cycle always starts in high-gain (HG) mode, as shown in Figure 3. When the CSA output V_{CSA} crosses V_{THR}, the comparator connects C_L in parallel to C_H, switching to low-gain (LG) mode until the read-out phase is completed. The comparator schematics are shown on the right in Figure 2. It consists of a differential pair with class-A output stage, in order to minimize the switching activity and reduce the noise injected into the input node DNW through the inter-well capacitance C_{DPW}. Positive-feedback is applied through the transistor M_{FB} which causes the comparator to maintain its state once V_{CSA} crosses V_{THR}. In this way, the comparator also acts as memory element, storing the information about the current gain-setting until the next RST phase. The comparator is reset by shorting the two branches of the differential pair while $V_{CSA} \ll V_{THR}$, i.e., during the CSA reset phase.

Noise shaping. In time-variant circuits, the contribution of the white series noise to the overall noise is proportional to the slope of the weighting function [15]. In other ASICs of the ePix family, a low-pass filter placed before the CDS stage reduces the slope of the weighting function, thus optimizing the noise performance [16]. However, due to the area constraints discussed in the previous section, a different approach has been adopted in ePixM: the slope of the weighting function is reduced by introducing two poles in the frequency response at two different nodes, shown as node A and B in figure 2. In both nodes, sampling capacitors of hundreds of fF are needed to minimize KT/C noise. Since these capacitors are implemented as Metal-Insulator-Metal capacitors (MIMcap) between the top-metals of the chip, they do not contribute to the area of the DNW implant. Node A acts as the dominant pole of the CSA stage when the CDS capacitance is connected to signal ground during the integration of the baseline. This pole acts on the leading edge of the weighting function. However, during the signal integration phase, the capacitor is connected in series to a source-follower. The capacitance seen at the output node of the CSA is reduced and moves its dominant pole to higher frequencies. This would result in a steep trailing edge of the weighting function. To compensate for this effect, another pole is introduced at node B by tuning the on-resistance of the S/H switch. The resulting noise weighting function is shown in Figure 3.

5 Correlated pre-charging

Excess noise in gain-switching architectures. In a gain-switching architecture followed by a CDS stage, the signal-to-noise ratio is degraded for input signals above the switching point. Excess noise comes from the fact that the gain of the circuit is set to HG during the baseline sampling phase, while the gain-switch happens during the signal integration phase. A timing diagram illustrating this effect is shown in Figure 4. When the RST switch is opened at $t = t_1$, noise from different sources is injected into the CSA producing an output voltage equal to ΔV_η. The CSA output is sampled on the CDS capacitor at $t = t_2$ and then subtracted during the signal integration phase when $t > t_3$. In other words, the CDS output is zero if no input signal is collected for $t > t_2$. Now let us assume that at $t = t_3$ the gain is forced to switch from HG to LG. The charge $q = \Delta V_\eta C_H$ stored on the feedback capacitor C_H is now re-distributed across both feedback capacitors, so the CSA output becomes $\Delta V_\lambda = \Delta V_\eta C_H/(C_H + C_L)$. However, the value ΔV_η is still stored on the CDS capacitor, so the signal at the CDS output becomes:

$$\Delta V_{CDS} = \Delta V_\lambda - \Delta V_\eta = -\Delta V_\eta \left[1 - \frac{C_H}{C_H + C_L}\right] = -\Delta V_\eta \frac{C_L}{C_H + C_L}. \tag{5.1}$$

The noise ΔV_η is re-introduced at the output node, attenuated by a factor $\alpha = C_L/(C_H + C_L)$. This effect degrades significantly the noise performance in the low-gain region, since the input charge is now amplified by a factor $\approx 1/C_L$, while the noise introduced by the RST switch is amplified by $\alpha \cdot 1/C_H \approx 1/C_H$ (in ePixM, $\alpha \approx 0.92$).

A solution adopted in similar architectures [3, 6] and based on the "lesser of two evils" principle is to bypass the CDS stage entirely when the gain is switched. In this way, the excess noise is removed at the expense of losing the CDS noise-shaping functionality. In the case of ePixM, the right side of the CDS sampling capacitor (node A) is connected to signal ground during the baseline integration to maximizing the signal swing. During the integration phase, this node is connected to a source-follower. Bypassing the sampling capacitor would shift the DC potential at the input of

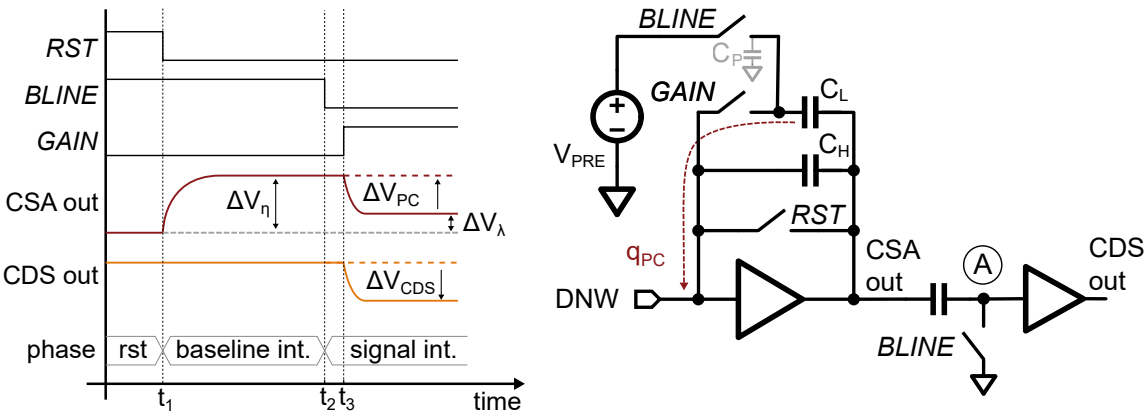

Figure 4. Left: timing diagram of the correlated pre-charging circuit. In this diagram, no signal is generated at the input DNW and the gain is forced to LG at instant t_3. The dashed lines show the signals at the output of the CSA and CDS when the correlated pre-charging circuit is enabled. Right: schematics of correlated pre-charging circuit.

the source-follower towards the supply, thus reducing significantly the dynamic range of the overall circuit.

Circuital implementation. The novel solution adopted in ePixM, here named *correlated pre-charging*, removes the excess noise due to switching while preserving the noise-shaping functionality and maintaining the full dynamic-range. The main idea behind the correlated pre-charging circuit shown in 4 is the following: when the gain is switched, the circuit generates a signal ΔV_{PC} at the output of the CSA which compensates the one stored on the CDS capacitor. This can be achieved by injecting a charge q_{PC} at the input of the CSA, so that $q_{PC} \cdot Gain_{LG} = \Delta V_{PC} = \Delta V_{CDS}$. By substituting ΔV_{CDS} calculated in Equation 5.1 we obtain:

$$q_{PC} = -\Delta V_{CDS}(C_L + C_H) = \Delta V_\eta (C_L + C_H)\left[\frac{C_L}{C_H + C_L}\right] = \Delta V_\eta C_L \tag{5.2}$$

Thus, sampling ΔV_η on capacitor C_L at $t = t_2$ results in an injected charge at $t = t_3$ which compensates exactly the offset stored in the CDS, thus removing any excess noise. The switch controlled by the BLINE signal implements this functionality by connecting the left side of the C_L capacitor to a fixed potential V_{PRE} during the sampling of the baseline. It can be easily demonstrated that this implementation is immune to parasitic capacitance C_P which might be present on the left-side of the capacitor: due to the capacitive divider formed by C_L and C_P, the voltage ΔV_L stored on C_L is $\Delta V_L = \Delta V_\eta \cdot C_L/(C_L + C_P)$. However, the charge injected at the input is still $q_{PC} = \Delta V_L(C_P + C_L) = \Delta V_\eta C_L$. Moreover, the dynamic range of the pixel circuitry can be optimized by tuning V_{PRE}, similar to what is done in similar developments [6].

6 Simulation results

The post-layout simulation results reported in this section have been obtained assuming a conservative value of 70 fF as total detector capacitance. Moreover, when expressing the input signal in terms of photon energy, it is assumed that the photons energy is fully converted into electrical charges collected at the input node. Figure 5 shows the response of the pixel for different integrated energies and different gain regions. The performance in terms of dynamic range and Equivalent Noise Charge (ENC) is summarized in Table 1 along with the Poisson statistical limit for 250 eV photons[2].

Gain [mV/fC]	Range [keV]	ENC [e^-]	Statistical limit [e^-]
HG: 187	0 - 50	11.3±0.4	69.4 (1 γ)
LG: 17	50 - 500	90.8±5.2	989.9 (14 γ)

Table 1. ENC and dynamic range for different gain settings. In both cases, the ENC is well below the Poisson statistical limit for 250 eV photons.

[2]For the sake of simplicity, we assume that the intensity variation of X-ray photons is described by a Poisson distribution. However, as explained in in [17], pulse-to-pulse intensity variations should also be taken into account when calculating photon statistics at FELs.

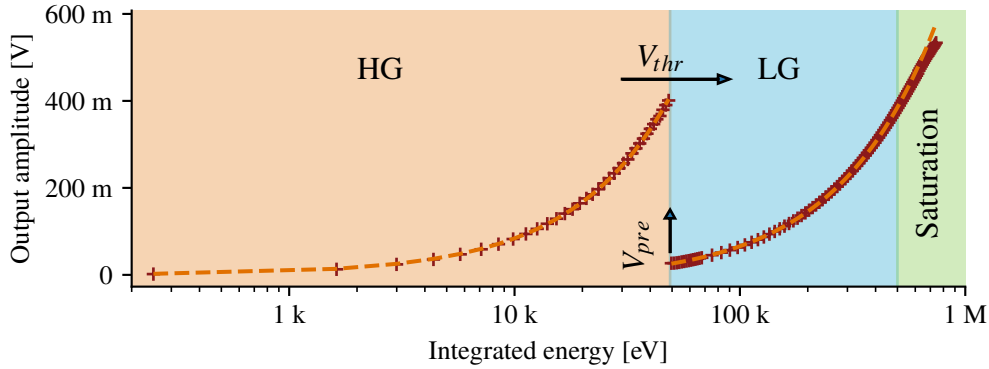

Figure 5. Output amplitude versus total input charge obtained through post-layout simulations. The two different gain regions (HG and LG) are highlighted. A linear fit for both gain regions is plotted as a dashed line. The output saturates for energies above 600 keV. The switching point and the pedestal of the LG region can be tuned by adjusting V_{THR} and V_{PRE}, respectively.

7 Conclusion and outlook

The design of ePixM has been completed and the results obtained from post-layout simulations meet all requirements in terms of noise and dynamic range. A full-scale die contains an array of 384×192 active pixel sensors resulting in a total sensitive area of 2×1 cm^2. Small-scale test structures, each one containing an array of 48×48 pixels, have been submitted together with the full-scale matrix and will allow us to independently characterize the performance of the front-end electronics. In the final detector system, a full-scale matrix will be connected through flip chip technology to a read-out ASIC containing an array of ADCs. Each ADC will be connected to a group of 96 pixels, which will be readout in a pseudo-column-parallel fashion. Since each ADC operates with a sampling-rate of up to 1 MHz [18], a frame rate of 7 kHz is expected for the first phase of the detector system development. Higher frame rates can be achieved by increasing the parallelism of the system and/or by improving the sampling-rate of the ADCs in the back-end ASIC. At the moment of writing, both the ePixM front-end and the readout ASIC are under fabrication at the different foundries. A complete characterization of the full system is expected by the end of 2019.

Acknowledgments

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