Discrete Element Transmission Line Beam Spreader Kickers for LCLS-II

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***Abstract*— The LCLS-II project requires a beam spreader to distribute the 929 kHz electron beam between two undulators and a dump. Three kicker sections and a septum are required to divert beam for each undulator. When the kickers are not pulsed, beam proceeds to the dump. Each kicker magnet is approximately one meter in length and composed of multiple sections. Each section consists of a ferrite and a capacitor to form a lumped element transmission line. The output magnetic field is a <250 ns base-to-base pulse with an amplitude of 4 mT. This paper presents the unique challenges of designing a transmission line kicker and driver with >500 kHz pulse rate. Provided experimental data illustrates pulse-to-pulse repeatability of approximately 100 ppm, transverse field quality, and field-settling time. Additional discussion includes thermal considerations and circuit protection. Adaptation of the kicker system for a low field long flattop pulse is also considered.**

I. Introduction

A beam spreader system is designed and under construction for implementation in the LCLS-II [1] free electron laser system. A superconducting linac generates 4 GeV electron bunches at a frequency of 929 kHz. The 929 kHz electron bunches can then be distributed via the beam spreader system between a soft x-ray undulator, hard x-ray undulator, and a beam dump. The beam spreader is composed of two diversion systems, each containing three pulsed kickers and a septum magnet, allowing arbitrary distribution of the beam bunches. The kickers operate simultaneously to produce an integrated magnetic kick of 12 mT-m to steer the beam into the high field region of the septum magnet. To accommodate high vacuum and the required beam stay clear, a 10 mm ID ceramic beampipe is installed in each kicker magnet. The magnet is composed of multiple ferrite sections, each capacitively coupled to the return conductor creating a lumped element transmission line, terminated into a nearby load. The three combined kickers systems are required to demonstrate a repeatability of 70 ppm rms. Additionally, the subsequent, non-kicked pulse, occurring a minimum of 1.08 µs later, must not be exposed to a remnant field exceeding 60 ppm of the kicked pulse. A prototype pulser and magnet system, operating at 500 kHz, was implemented to demonstrate the required parameters.

II. General Considerations

To avoid radiation damage and decrease MTTR the bulk of the kicker electronics are located outside of the tunnel and connected via 20 m of cable. To accommodate the high repetition rate it was necessary to construct a matched impedance transmission line system to avoid reflections in the cables. Due to their high frequency switching attributes, MOSFETs were chosen as the primary switching device. For simplicity, series MOSFET configurations were avoided, thus limiting the voltage to 900 V for COTS devices with appropriate voltage overhead capable of switching tens of amps at ~1 MHz. With a required stay clear aperture of 10 mm, the voltage required for a strip-line kicker structure far exceeds 900 V. Therefore, a ferrite loaded transmission line kicker magnet topology was selected. Long high vacuum ceramic tubes with sufficient straightness are difficult to manufacture, thus the kicker length was limited to 1 m.

A thorough description of transmission line kicker theory is provided in [2]. The magnet is composed of multiple ferrite cells. Each cell is coupled to the return conductor via a capacitor as shown below.

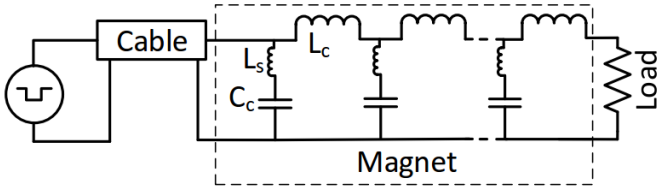

Fig. 1. Diagram of transmission line magnet system. L_c and C_c are the ferrite inductance and discrete added capacitance respectively. L_s is the parasitic inductance in series with each cell capacitor.

The ideal impedance of the magnet, Z, and fill-time, τ, are given by:

$$Z = \sqrt{L_c/C_c} \tag{1}$$

$$\tau = \frac{L_T}{Z} \tag{2}$$

where L_T is the sum of each ferrite's inductance and is primarily determined by the magnet's gap volume. To accommodate a reasonable beampipe wall thickness of ~5 mm, the magnetic gap is 20 mm, requiring a current of 64A to produce 4 mT. While the gap and magnet length set the magnet inductance, the added capacitance can be changed to

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set the impedance which must be low enough to accommodate the required current given the design voltage. Alternatively, it is advantageous to keep the magnet impedance high to reduce the required fill-time and thus allow the maximum time for the field to settle to zero before the unkicked bunch transverses the structure. To take advantage of common cable impedances, a 12.5 Ω system impedance (four parallel 50 Ω cables) was selected, yielding an ideal fill time of 101 ns. However, in practice each cell has a self-resonance which limits the effective fill time. The cell cut-off frequency, f_c, is given by [3]:

$$f_c = \frac{1}{\pi\sqrt{(L_c + 4L_s)C_c}} \quad (3)$$

This has the effect of increasing the fill-time of the constructed magnet to 123 ns.

The number of sections was determined via spice modeling. A simple ten cell system was modeled with a single inductor-capacitor set forming each cell. The current in all inductors was summed and the resulting waveform did not settle to 50 ppm until 1.44 μs after the main pulse. A 20 cell system settled to 50 ppm within 0.82 μs. The final design contains 18 cells.

Limiting parasitic capacitor inductance is critical to efficiently transmitting a high frequency pulse. Thus multiple C0G low loss surface mount capacitors are mounted in parallel. Parallel copper flags are extended from the supply and return busbar and attached to the capacitator carrying PCBs. In addition to low inductance, this arrangement allows for an easily tunable capacitance value by adding or subtracting discrete capacitors.

For simplicity, a c-core magnet geometry is chosen. The gapped magnet cores are composed of Ferroxcube's 4M2 NiZn soft ferrite [4]. The material's resistivity, 10^5 Ωm, is suitably high to prevent eddy currents and provide insulation between bus voltages. Additionally the hysteresis loss of the core is extremely low, even at high frequencies. The power loss in the ferrite can be approximated by calculating I^2R losses given a calculated ferrite resistance, R_f, of:

$$R_f = 2\pi f_0 L_f \tan\left({}^{u''}/_{u'}\right) * \frac{PRF}{2f_0} \quad (4)$$

Where u' and u'' are the real and imaginary permeability given at the fundamental frequency of the output pulse, f_0. L_f is the ferrites inductance, excluding the dominating inductance contribution of the gap. The second term, scales the power loss result to the *PRF* (pulse repetition frequency). For the 100 ns pulse and geometries of the constructed kicker, a 9 W/m ferrite loss is calculated.

The ceramic beampipe is internally coated with a thin layer of titanium with a sheet resistivity of 23 Ω. The coating prevents charge build-up in ceramic. The coating thickness was experimentally determined, where the thickest coating possible was applied without generating excessive eddy current losses and maintaining the beampipe well under 200°C, the Curie temperature of the ferrite. At 500 kHz, no portion of the beampipe exceeded 93°C. A photo of the prototype magnet is shown below:

Fig. 2. Photo of transmission line magnet.

III. PULSED POWER SUPPLY

The pulsed power supply is the combination of three power handling chassis: a capacitor charging supply, a capacitive filter chassis, and a switching driver chassis as shown below:

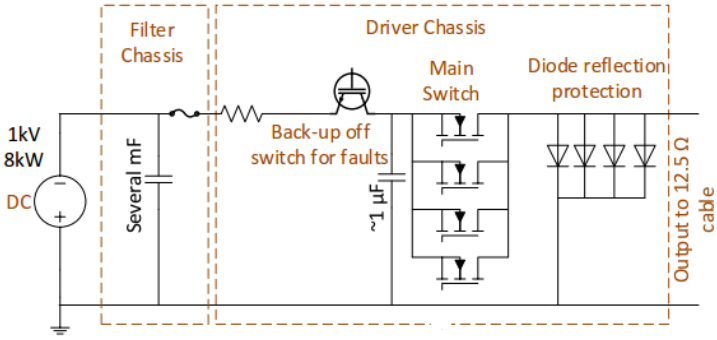

Fig. 3. Pulser diagram.

A. *Switching*

The driver chassis contains four parallel 1.2 kV MOSFETs which switch in unison to generate output pulses. In publication [5], single event MOSFET failure is presented as a likely significant cause of failure at DC voltages near the peak operation value and the following experimentally based curve fit is provided:

$$failure_{rate} = 10^{(0.19 \times V_{stress\%} - 14.3)} [\% \cdot year^{-1} \cdot cm^{-2}] \quad (5)$$

Where $V_{stress\%}$ is the percentage of rated voltage applied. For 90%, 80%, and 75% the rated voltage stresses the respective failure rate per year for a 1 cm^2 device is calculated as 631%, 8%, and 0.9% respectively. Therefore a 75% maximum operating voltage of 900 V was selected to achieve reasonable reliability.

Transient voltage stress can be induced by two sources: di/dt during turn-off and shorted magnet reflections. Because of the high repetition rate, snubbers are unrealistic to implement due to excessive heat losses. A local on-board filter capacitance of 1.1 µF is located close to the MOSFETs such that the pulse current inductive loop is minimized, ensuring no switching induced over voltage. The filter capacitance is composed of parallel C0G type ceramic capacitors. The mounting inductance of film capacitors proved too high, leading to an unstable output.

To prevent voltage doubling across the switch caused by reflections generated in a magnet short, fast diodes are installed to absorb the reflection. Several diodes are used in parallel to limit the diode drop to less than a few hundred volts. The control system monitors the load's voltage divider and trips the system off if a load pulse is not detected. Unfortunately, excessive diode heat is generated due to current flow through the parasitic capacitance of the diodes during normal operation. Some of this heat may also be attributed to partial turn-on of the diode caused by small magnet reflections. At 800 kHz operation the diode overheats and shorts limiting higher rate operation.

In initial experiments the source of the MOSFETs were tied to the output, but the rapid output transient induced unreliable triggering, likely due to gate oscillations. Therefore the system was configured with the source tied to the stiff bus voltage which was configured to be negative such that n-type MOSFETs could be utilized.

A rapid rise-time pulse excites magnet cell resonances that take significant time to dampen. Thus series MOSFET gate resistors were added to reduce the rise time to ~20ns (0%-90%). The rise-time chosen is a compromise between switching losses and limiting cell resonance excitation. A photograph of the driver chassis is shown below.

Fig. 4. Photo of driver chassis. Each MOSFET is clamped to a grounded water cooled plate on the PCB underside and driven with a dedicated driver.

B. DC Source

An 8 kW COTS capacitor charging power supply is used to charge a large capacitive filter chassis. A capacitor charging power supply was chosen for two reasons. First, at the time of design it was one of few readily available COTS 1 kV power supplies with high power density. Second, the stiff DC source supplied by the large capacitor bank is optimum to minimize turn-on oscillations. The size of the capacitor is set by ensuring the voltage change produced from one bucket of power supply charge is less than the voltage required to achieve pulse repeatability [6]. The inductance between the filter bank chassis and on-board capacitors located near the MOSFET switches is roughly 1 µH. When the MOSFET pulse pattern begins initial amplitude instability is induced due to the settling time of the LRC circuit formed by the charging inductance, on-board capacitance, and charging resistor. The purpose of the charging resistor is to minimize the settling time by setting its value (less than a few ohms) to critically dampen the charging resonance.

C. Cables and Load

Four parallel 50 Ω cables connect the pulser to the magnet. Due to the resistivity of the cable inducing dispersion, the pulse has a long decay tale at the 0.1% level. The tail can be decreased by shortening the cable or increasing the cable radius. The decay time of the cable is solved analytically in [7] and [8]. To connect the pulser located in a service building with the magnet within the tunnel, the required cable length is 20 m, requiring a 7/8" cable to decrease the decay to 54 ppm of the main pulse, 1.08 µs after the peak of the pulse when the unkicked bunch traverses the magnet.

To limit the total cabling required and prevent excessive cable pulse decay time, the load is located near the magnet. The load is composed of five 2 kW water cooled thick film resistors. Four resistors, capable of absorbing 8 kW make-up the bulk of the power handling capability, providing 31% overhead for the calculated power generated at 929 kHz. An additional trim resistor is added in parallel to tune the total resistance to the system impedance. The surface mount power resistors have substantial parasitic capacitance to the cooling plate. To prevent this capacitance from interfering with the matched system impedance the plate is electrically isolated. An RC voltage divider is mounted to the load feeding a 50 Ω cable that carries the signal to the load controller.

IV. Measurements

Measurements were made to quantify how quickly the pulse returns to zero, the pulse repeatability, and the transverse magnetic field quality.

A. Remnant Field

Bdot measurements, the traditional approach to measuring fast pulsed kicker fields, are not sensitive enough to measure the low fields required, <0.24 µT, following the 4 mT pulse. An alternative approach of measuring the sum of cell voltages was implemented. The remaining energy in the kicker following the pulse resonates between the inductance and capacitance of each cell. Thus, the ratio of the sum of voltages

remaining at a given time post pulse to the sum of peak voltages is equivalent to the ratio of remaining integrated magnetic field to peak integrated magnetic field.

In order to measure the small remnant fields following the main pulse, it was necessary to shunt the 900V peak pulse to avoid saturating the scope. This was achieved by diode clamping the pulse using the configuration shown below.

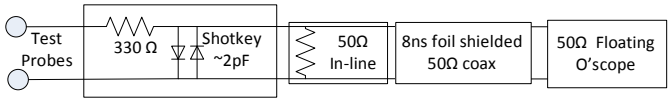

Fig. 5. Diagram of probe used to measure remnant voltages in magnet.

The voltage measurement was made following each ferrite using a floating scope. The resulting waveforms were summed, and the results are shown below.

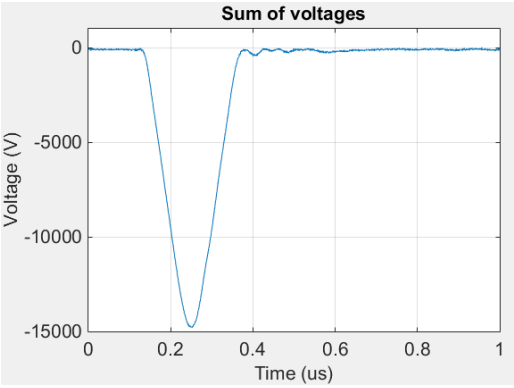

Fig. 6. Using standard oscilloscope probe, the voltage waveforms across the capacitor following each ferrite are captured and summed.

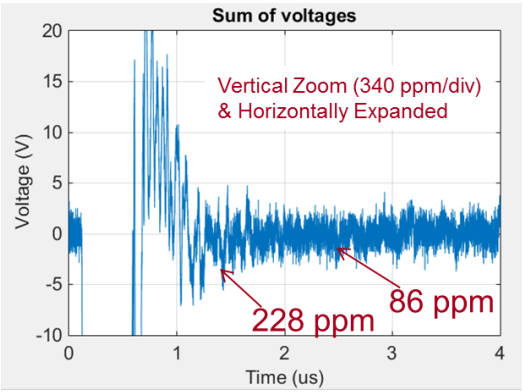

Fig. 7. Using a custom probe, the same voltage measurements as fig. 7. is made. The resulting summed waveform is zoomed vertically by a factor of 500 and the horizontal scale is expanded a factor of four.

The worst case remaining field at ~1 μs following the pulse peak is 228 ppm. However, the post pulse remnant field pattern is highly repeatable. Thus by phase shifting the output pulse, it's possible to reduce the field to acceptable levels. The worst case remnant field ~2 μs later is 86 ppm.

B. *Pulse Repeatability*

The pulse repeatability was measured by zooming in on a portion of the load voltage waveform. The voltage signal was fed into a COTS offset amplifier such that the oscilloscope could maximally amplify the peak of the waveform with zero scope offset. A 20 MHz hardware filter was used to limit background noise. This smooths the pulse ripple but does not reduce voltage variations that affect the entire pulse. The standard deviation of the mean value of a small portion of the peak waveform was measured by the scope. All measurements of standard deviation at rates from 10 kHz to 500 kHz measured instabilities of less than 101 ppm. Given that multiple independent kicker systems work in summation, the effective repeatability is reduced by sqrt(n).

C. *Transverse Field Quality*

The transverse magnetic field deviation was measured by inserting an in-house built 50 Ω Bdot probe down the entire length of the magnet. Shims were used to change the vertical position of the Bdot, while adjustment screws could adjust the horizontal position.

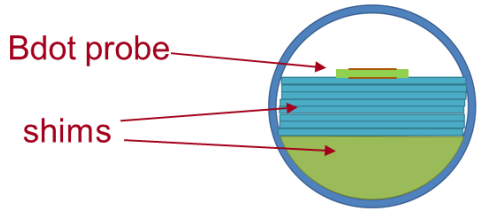

Fig. 8. Beampipe cross section diagram of shimming method to support Bdot probe. A screw is used at each end of the magnet to set horizontal position.

Bdot measurements were taken at distances from the center between 1.6-1.9 mm. In each location ten measurements were made, integrated, and averaged. The maximum resulting magnetic field deviation from the center of the magnet is 0.27%, meeting specification.

V. ONGOING WORK

Work is underway to increase the maximum operating rate from 500 kHz to 1 MHz. At the moment the key area of focus is decreasing heat dissipation in the pulse reflection protection diodes.

Other areas of study include applications that require lower field, but at longer flat-top while still achieving 1 MHz rate. At lower field, the MOSFET voltage requirements can be scaled down, allowing for a lower voltage MOSFET with lower drain-source resistivity. Additionally, the load power drops with the square of the voltage. Both these effects allow the pulse width to be increased substantially. Also, since fill-time becomes less significant in a long pulse system, it's possible to series several magnets to one driver.

ACKNOWLEDGMENT

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