SLAC-PUB-16893

Wrapped-Around Conductive Traces

A. Tomada, J. Segal, C. Kenney, M. McCulloch

***Abstract*– Most microsystem interconnections are formed using wire bonds or bump bonds. Industries and national laboratories have been jointly pursuing a partially 3D interconnect technology, which has the potential to increase the amount of circuitry per pixel by a factor of 2-3 This development effort has taken considerable time and resources, while producing very modest results due to the intrinsically difficult nature of the processing involved. In contrast, the technology presented here is less expensive, simpler, and can increase the circuitry per pixel. Fabricating wraparound conductive traces is a key element of the success of this technology.**

I. Introduction

Most microsystem interconnections are formed using wire bonds or bump bonds, both of which have enabled cutting-edge science such as nEXO, LHC, Fermi, LCLS, and CDMS[1][2]. Wire bonding is an intrinsically one-dimensional process, while bump bonding is two-dimensional process limited to connecting a pair of parallel substrates. Several national laboratories, concurrently with commercial foundries, have been jointly pursuing 3D interconnect technology [3]. While such 3D interconnects have already achieved considerable market penetration in consumer applications, i.e. stacked image sensors for smart phones [4], the use of this technology for scientific applications is still very rare. For small volumes the required vendor chain for full 3D integration is complex and the resulting turnaround times are much longer than for established ASIC development. 3D Integration technology can offer very high interconnect densities, but it is has a number of drawbacks: it is complex, needs special ASIC design which takes the TSV rules into account, and it is currently done with only 2 or 3 tiers (layers of electronics), thereby increasing the circuitry available for each pixel only by that factor of 2-3.

In contrast, the technology presented here offers lower interconnect density, but is considerably simpler. It could increase the circuitry available per pixel by a factor between 10 and 100. Fabricating wrapped-around conductive traces is a key element of the success of this technology. In this work we demonstrate the ability to form metal traces that wrap around a chip edge. Tests have shown that these traces are electrically conducting around the corner and that there are no shorts between neighboring traces. In addition, bumps (either indium or solder) could be applied on an ASIC with wraparound traces, both on the front and the back side, such that this ASIC can be bump-bonded to a sensor on the front side and then bump-bonded to a PCB on the backside. This will eliminate the usual wire-bonding, minimizing the packaging footprint.

This work is supported by the Department of Energy, Laboratory Directed Research and Development funding, under contract DE-AC02-76SF00515.

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II. Research

We initially investigated evaporating Aluminum traces on small quartz chips by using a simple shadow mask with a large pitch of 500µm, as shown in Fig.1.

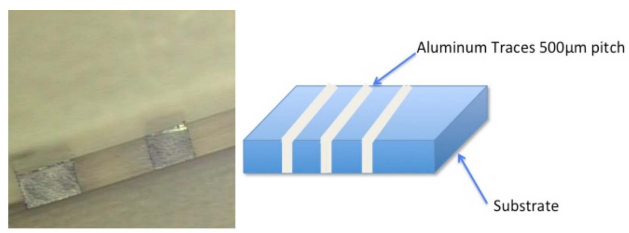

Fig. 1. Aluminum traces wrapping around the edge of a glass chip on the left, and a cartoon of top-to-edge traces on the right.

Testing these traces demonstrated electrical continuity around the corner edge of the chip, proving that the evaporation step created a wrapped-around trace.

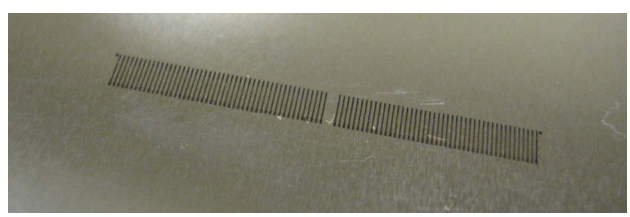

Fig. 2: Stencil pattern on SS plate 50 µm thick.

After obtaining these preliminary results, we started exploring how we could create thinner traces (60 µm) with smaller pitch (200 µm).

The second approach was to laser cut a stainless steel stencil. The stencil came in a 2 inch by 2 inch square, which we then had to bend around the chip. See Fig.2 & 3.

We manually aligned the stencils to our in-house ASIC chip, which is 2 cm by 2 cm in size. The alignment was performed after depositing a layer of low temperature SiO_2 (about 100nm at 300°C) on the sides and back face of the chip

This material is based upon work supported by the U.S. Department of Energy, Office of Science, Laboratory Directed Research and Development funding, under Contract No. DE-AC02-76SF00515.

to ensure isolations between the traces. Then we evaporated a layer of Aluminum, about 0.5 µm thick for each side. The Al traces are showed in Fig.4.

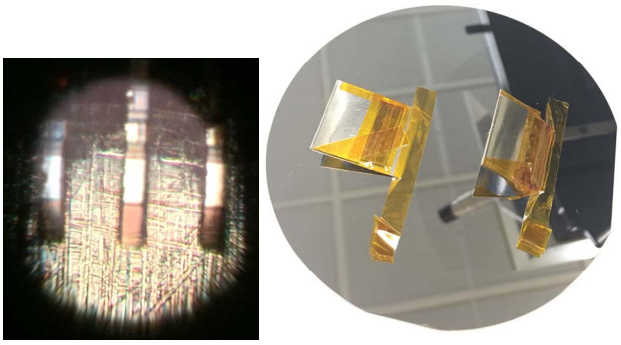

Fig. 3: Two ASICs with stencils mounted on a wafer prior to the Al evaporation, and zoom of the alignment of the trace to the pads.

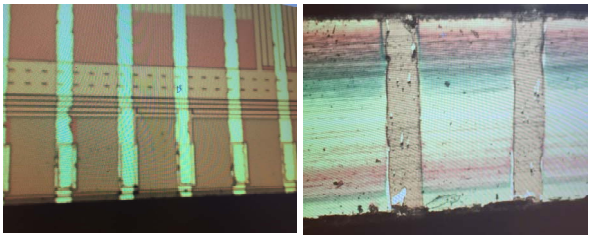

Fig. 4: a) Image of Al traces on the front of the ASIC; b) Image of the Al traces on the ASIC side-wall.

In order to make alignment easier and achieve better resolution on the corners, we explored a third approach. This method involved patterning dicing tape. Using the same design used for the stencil, we patterned the blue dicing tape with a Minitech milling machine with a fine bit of 50µm diameter. Alignment was easier and more accurate.

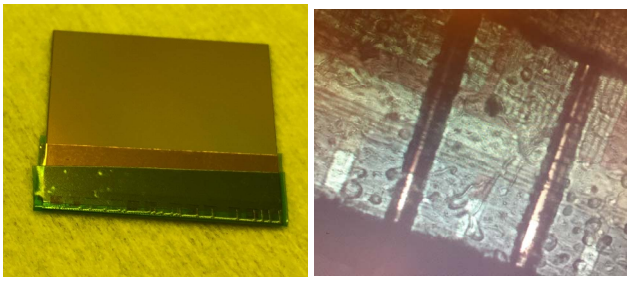

Fig. 5: Shows the ASIC substrate with the dicing tape applied and aligned, on the right the zoom of the alignment and slots.

Post-processing the ASIC substrates led to some unexpected challenges. First we did not take into account some test features located below the wire-bonding pads. These test structures caused shorts between our traces. To overcome this, in our second attempt we trimmed off few hundred microns to remove the possibility of electrical shorts. The second challenge was that the passivation layer on the ASICs is much thicker than expected, about 1.7 µm. Consequently our deposition of 0.5 µm aluminum was not sufficient for step coverage, resulting in electrical opens. We then increased our film thickness to approximately 2µm, which fix the problem.

III. Results

Overall results from the first two approaches were good. When we probed the traces around the corner of the chip we observed electrical continuity on multiple chips. The third technique with dicing tape was less successful. The removal of the dicing tape caused the oxide layer to peeled off as well destroying the metal traces.

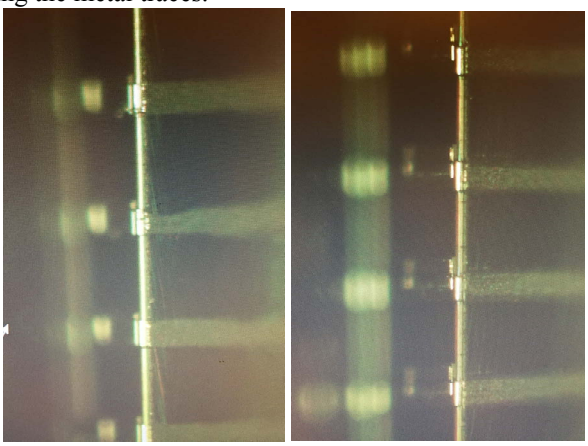

Fig. 6: Shows two side-views of the traces on the corner of the chip. On the left side are the Al bonding pads covered by the evaporated traces that continue on the short side wall of the chip.

IV. Possible applications

There are several possible applications of this technology. In addition to increasing circuit density, this technique can enable other advances such as thicker sensors, for example in a hard x-ray spectrometer camera. As shown in Fig.7, a set of low-capacitance silicon strips would have edge traces deposited, and then be assembled into a stack ten-chips high. Indium bumps will then be deposited on the edges of the stack. A readout ASIC chip will be bump-bonded to the stack edge. The result will be a cube on a side with the ASIC wire bond pads protruding from one corner for mounting on a printed circuit board. Assuming a 5 mm cube, the advantage of this system over a standard bump-bonded configuration is that incident x-rays would traverse 5 millimeters of silicon, which would provide good quantum efficiency up to 40 KeV, in contrast to a typical 0.5 mm thick sensor, which is only efficient up to about 18 KeV. Another advantage is that the circuit chip is located off the photon axis and so can be shielded from the incoming radiation.

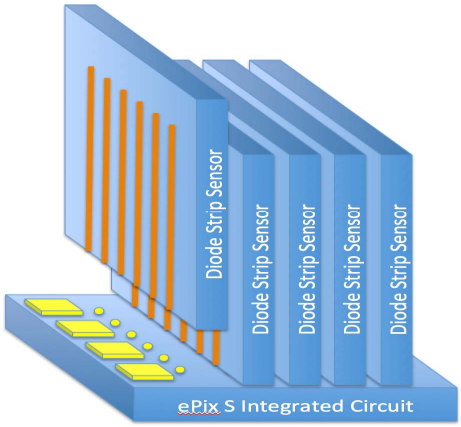

Fig. 7: Stack of strip-geometry diode sensors (x-rays incident for the left) bonded to a low-noise spectroscopy circuit chip to form a pixel with 5 mm of silicon to absorb hard x-rays.

CONCLUSION

We successfully demonstrated the capability of fabricating conductive Aluminum traces -down to 100µm pitch- wrapping around the three sides of a chip. Next step is to build a full system with a stack of chips with wrapped around traces.

ACKNOWLEDGMENT

We would like to acknowledge the Stanford Nanofabrication Facility (SNF) where the conductive traces were fabricated.

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