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Design and Characterization of the tPix prototype: a spatial and time resolving front-end ASIC for electron and ion spectroscopy experiments at LCLS

B. Markovic*, P. Caragiulo, A. Dragone, C. Tamma, T. Osipov, C. Bostedt, M. Kwiatkowski, J. Segal, J. Hasi, G. Blaj, C. Kenney, G. Haller

I. Introduction

Over the past two decades momentum resolving spectrometers have revolutionized electron and ion spectroscopy. Momentum spectroscopy has enabled a new class of experiments in both laser based ultrafast sciences, and x-ray spectroscopy [1]. The fundamental concept of these spectrometers is that the time-of-arrival (ToA) and position of each fragment is measured. From these data the momentum vector of each particle can be calculated. So far delay-line detectors based on a microchannel plate (MCP) and a long wire anode have been used in these spectrometers which are severely limited in their multi-hit capability and therefore not suitable for experiments with fourth generation light sources such as Linac Coherent Light Source (LCLS).

To fully exploit the capabilities of momentum spectroscopy at LCLS, a suitable multi-hit capable hybrid detector system is required. The core of such system would be a pixelated ASIC with a time-to-digital converter (TDC) per pixel. While some time-resolving imagers [2-5] were developed in recent years, they rely on excellent timing and inherent digital response of monolithically integrated single-photon avalanche diodes (SPADs) which are not suitable for momentum spectroscopy or many high-energy physics (HEP) experiments. This kind of applications requires a hybrid detector system in which the acquisition and time measurement chip is bump-bounded to a suitable sensor. Such hybrid detectors were developed for high-energy physics (HEP) experiments at CERN [6] but lack the time-resolution performance necessary for momentum spectroscopy experiments.

Here we present tPix, a signal acquisition and time measurement chip for time-resolving pixelated particle detector Tixel, aimed for momentum spectroscopy experiments at LCLS. The final version of the chip will have an array of 176x192 pixels, while the prototype, reported here, has a smaller 48x48 matrix and a chip periphery, referred to as balcony, complete with all the circuitry of the final version. The chip was fabricated in 0.13µm CMOS technology and its design and initial characterization will be reported here.

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B. Markovic*, P. Caragiulo, A. Dragone, C. Tamma, T. Osipov, C. Bostedt, M. Kwiatkowski, J. Segal, J. Hasi, G. Blaj, C. Kenney, G. Haller are with SLAC National Accelerator Laboratory, Menlo Park, CA (*e-mail: markovic@slac.stanford.edu).

II. tPix Architecture

The block diagram of the chip is shown in Fig.1. It has 100x100µm^2 size pixels which perform analog front-end operations of charge acquisition, amplification and threshold comparison together with digital ToA and time-over-threshold (ToT) measurements. Signals which are critical for time measurement such as global clock GClk and global counter bits GCount[0:7] (implemented as Gray code for power saving purpose) are distributed to pixels through a balanced hierarchical signal tree. The balcony contains circuitry for chip configuration and operation, analog bias generation including a bandgap reference and DACs, time measurement and matrix readout.

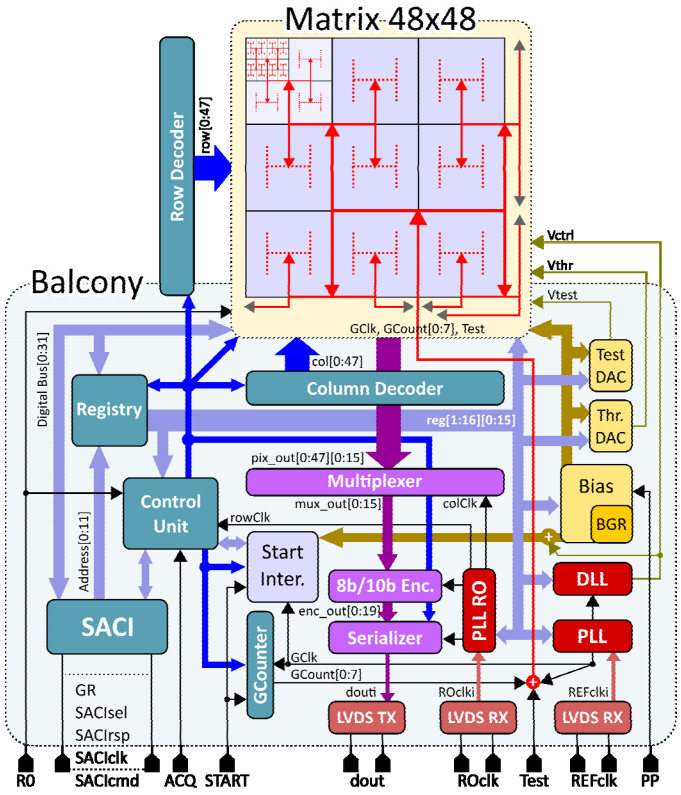

Fig. 1: Block diagram of the chip architecture composed of a 48x48 pixel matrix and peripheral balcony.

In Fig. 2 the operation phases are shown. Configuration is performed using the SLAC ASIC control interface (SACI)

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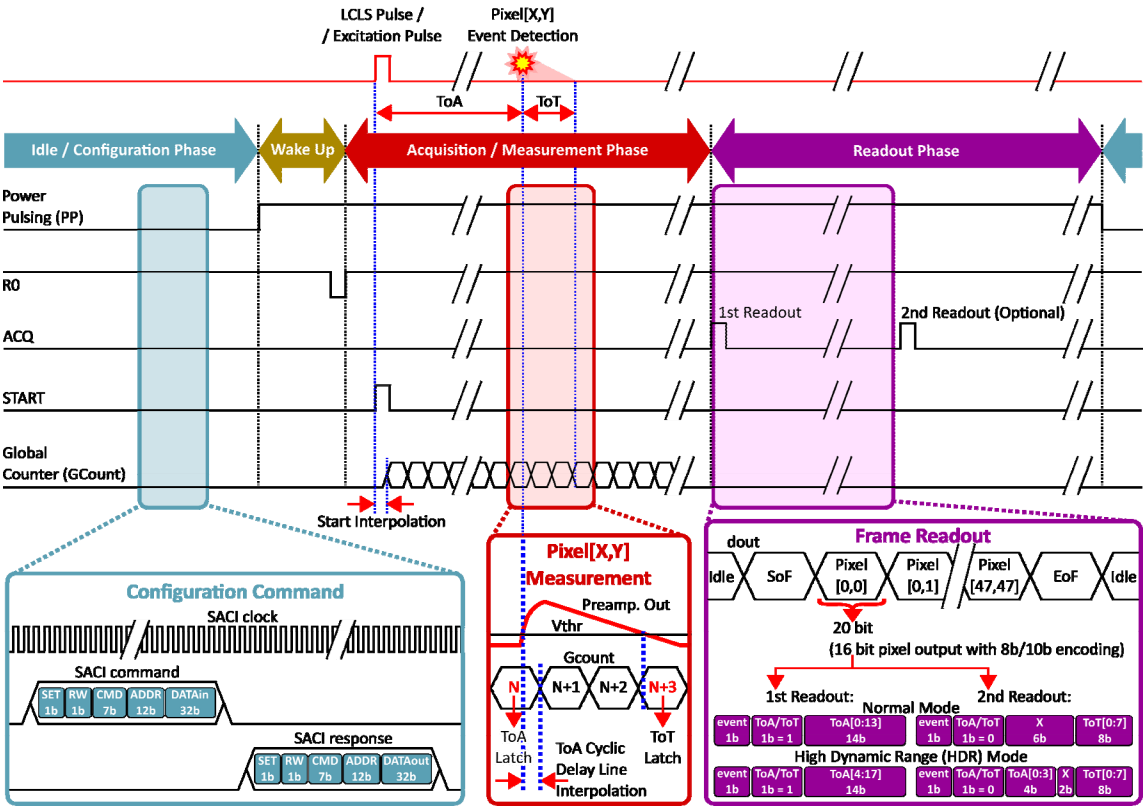

Fig. 2: System operation phases: idle/configuration, acquisition/measurement, readout.

employing a custom serial handshake protocol. The control unit along with SACI enables writing and reading of both global registers that control various aspects of the chip (from PLL and DAC settings to bias current trimming and operation mode selection) and in-pixel registers used for configuration of individual pixels. A power pulsing scheme is used in order to reduce the power consumption of analog front-end in phases in which signal acquisition and time conversion are not performed (idle/configuration phase). This is achieved by current-starving analog sections of the matrix through bias lines generated within the balcony.

The START signal represents the beginning of time measurement and enables an 8b global counter clocked with GClk generated by an internal PLL locked to an external reference clock. The value of the global counter is distributed to each pixel and latched in correspondence of above-threshold signal detection (for ToA measurement) and below-threshold signal decay crossing (for ToT measurement). In addition, each pixel performs a 6b (normal operation mode) or 10b (high dynamic range HDR mode) interpolation of ToA within the GClk period. A start interpolator performs the same kind of interpolation on START pulse, necessary in case the reference clock is not in phase with the START signal. The 16b pixel output consists of two control bits and 14 bits of measurement data. The readout, initialized by ACQ signal, is performed by scanning the matrix by rows and multiplexing the columns on a single 16b bus which is first 8b/10b encoded and then serialized and transmitted using a LVDS transmitter. The first readout provides the 14b of ToA data, while a second readout is necessary if 8b of ToT and additional 4b of ToA (in HDR mode) are required.

The back-end of the chip shares the same architecture as the ePix platform of detectors at LCLS [7], thus enabling an easy and cost-effective integration of the Tixel detector with existing LCLS detector technology.

III. tPix Pixel Architectures

Fig. 3 shows the schematic of the pixel. The analog front-end is composed of a charge-sensitive preamplifier able to achieve peaking times of around 10ns, a 2.8fF feedback capacitor, a linear discharge circuitry necessary for ToT measurements, a comparator and a 4b threshold calibration DAC for pixel-to-pixel mismatch equalization. The output of the comparator is sensed by a control logic which detects the first event after the matrix reset (signal R0) and feed it to the 16-cells long delay line in which the signal propagate cyclically until the arrival of the first following GClk rising edge which samples the state of the delay line using a SRAM. The position of the signal within the delay line stored in the SRAM provides the first 4 bits of ToA interpolation. The number of cycles the signal has accomplished before GClk interrupted the cyclic loop is sensed by a local counter and represents the other 2 (Normal mode) or 6 (HDR mode) bits of ToA interpolation.

The cyclic delay line, shown in Fig. 4, is composed of 16 differential cells whose propagation delay represents the resolution of ToA measurement and it is set by the voltage

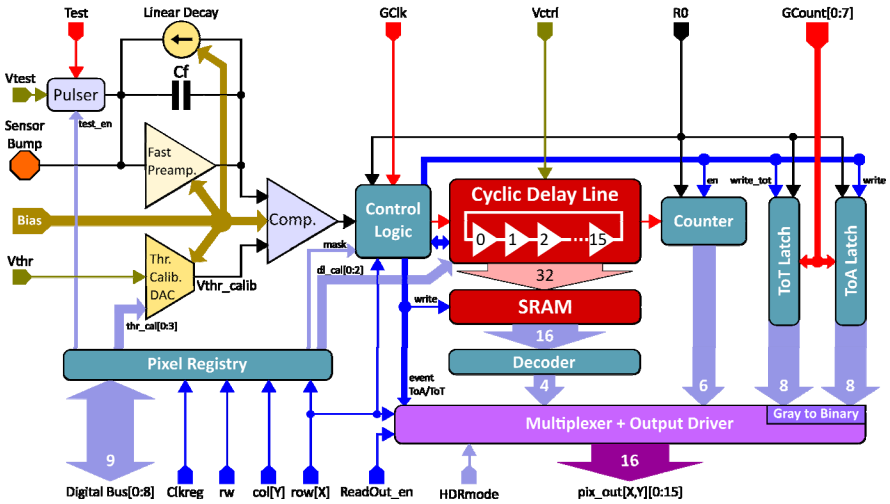

Fig. 3: Pixel block schematic including analog front-end, digital control and configuration logic, time-interpolation cyclic delay line and readout circuits.

Vctrl generated by a delay-locked loop (DLL) inside the balcony. Within the pixel, Vctrl generates voltages Vctrl_n and Vctrl_p used to current-starve the sources of the differential pair, thus limiting the cell switching speed. The role of the DLL is to fix the time resolution to a fraction (1/64 in normal and 1/1024 in HDR mode) of GClk period and to stabilize it in respect to process, voltage and temperature (PVT) variation.

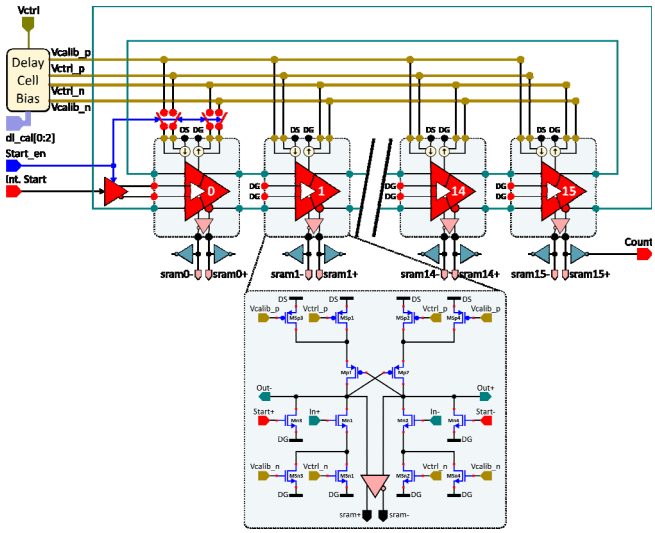

Fig. 4: Schematic of the cyclic delay line composed of 16 differential cells whose propagation delay is controlled by current-starving. A parallel input pair allows for initialization of time-interpolation.

Additionally, voltages Vcalib_n and Vcalib_p are generated by 3 calibration bits, stored inside pixel registry, and used to slightly trim the propagation delay of pixel cells around the value set by the DLL in order to compensate for pixel-to-pixel mismatches. The delay line has to accommodate for both initializing signal input from outside and internal circulation while maintaining the same load for each cell in order to avoid systematic mismatches. This is accomplished with an additional NMOS input pair Mn3-Mn4 activated only in the first cell when event detection is expected. When Mn3-Mn4 are active the cyclic loop is interrupted by turning off the NMOS current sources of the Mn1-Mn2 input pair and adapting the PMOS sources to the strength of Mn3-Mn4 transistors so that the interpolation start signal can enter the delay line. Once the interpolation has been initialized the Mn3-Mn4 pair is turned off and the cyclic loop is closed until the end of conversion determined by the following GClk rising edge.

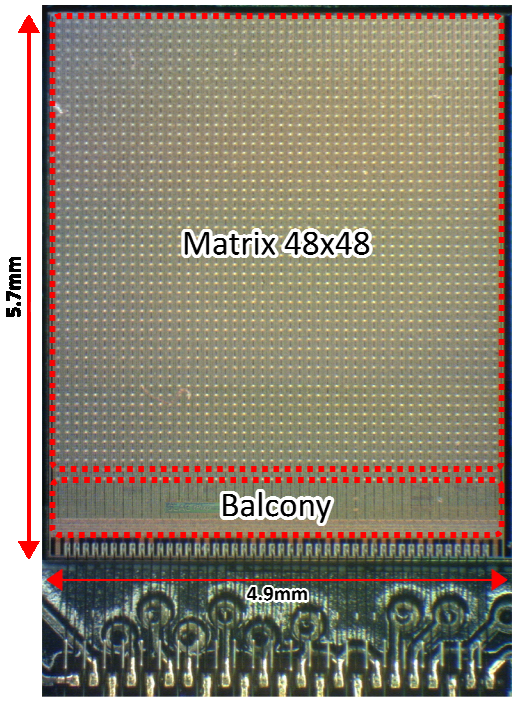

Fig. 5: Photograph of the chip fabricated in 0.13µm CMOS technology with 5.7x4.9mm^2 area.

While the global counter operation is initialized by the START pulse, the in-pixel time-interpolation follows the reverse START-STOP operation principle where the event

detection, i.e. the actual time-measurement STOP signal, initializes the time-interpolation while the following GClk terminates it. In typical experiments the pixel hit occupancy is expected to be low thus the reverse START-STOP operations saves power by initializing the time-measurements only in pixels that received signal above set threshold, instead of starting the measurement in the whole matrix for each measurement cycle.

IV. tPix Prototype Test Results

The tPix prototype has been fabricated in TSMC 0.13µm CMOS technology. The image of the prototype chip is shown in Fig. 5. The prototype testing is under way and initial characterization is reported here. It reaches the time-resolution of 100ps and the measurement rage of up to 26µs (18b in HDR mode).

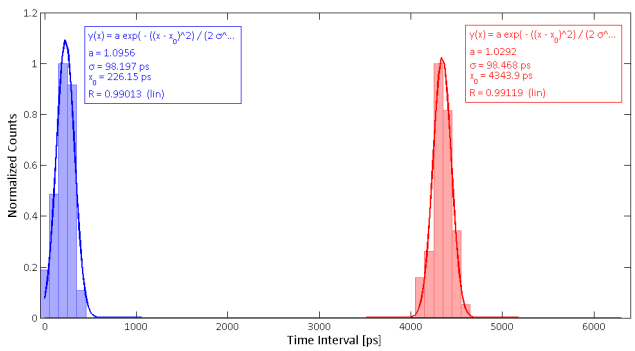

Fig. 6: Example of chip time measurements of two different time intervals.

The chip characterization was performed using internal test circuits composed of a 6b DAC which generates the voltage Vtest that determines the charge which is injected in the preamplifier input of test-configured pixels by an in-pixel pulser in correspondence of the externally provided Test pulse. Fig. 6 shows an example of time measurements for two different time intervals.

V. Conclusions

tPix is the front-end ASIC for Tixel detector aimed for momentum spectroscopy experiments at LCLS. Table I summarizes the performances of the chip and compares it with the recent works on pixelated time-resolving systems. This work achieves time-measurement performances at the level of current all-digital state-of-the-art combined with an analog front-end necessary for hybrid detectors aimed at momentum spectroscopy and HEP experiments.

Table I: Performance comparison with previous works on pixelated time-resolving systems

Parameter	tPix [this work]	Timepix3 [6]	[2]	[3]	[4]	[5]
System Type	Hybrid	Hybrid	Monolithic (digital SiPM)	Monolithic (SPAD)	Monolithic (digital SiPM)	Monolithic (SPAD)
Technology	0.13µm CMOS	0.13µm CMOS	0.35µm CMOS	0.35µm CMOS	0.13µm CIS	0.13µm CMOS
Array Size [pixels]	48x48	256x256	9x18	32x32	8x16	160x128
Pixel Size [µm²]	100x100	55x55	800x800	150x150	610.5x571.2	50x50
Total # of TDCs	2304 (1 per pixel)	65536 (1 per pixel)	432 (48 per col.)	1024 (1 per pixel)	256 (2 per pixel)	20480 (1 per pixel)
Preamp. Gain [µV/e⁻]	57	53	N/A			
Preamp. Peak Time [ns]	10	25				
ToA Resolution [ps]	100	1562.5	48.5	312	64	55
ToA Range [# of bits]	14 or 18	18	17	10	12	10
ToT Range [# of bits]	8	10	N/A			

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