# LCLS FEMTO-SECOND TIMING AND SYNCHRONIZATION SYSTEM UPDATE* 

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## Abstract

A femtosecond timing and synchronization system has been installed and has been running successfully on LCLS since September 2009. We expanded the system from two channels to a multichannel system. The upgrade includes a 16 channel transmitter, a new implementation of the receiver, and an upgraded Graphical User Interface. The new receivers are installed and operating in five experimental end stations and are supporting experiments.

## INTRODUCTION

Our femtosecond timing and synchronization system was developed in 2007 [1, 2, 3], and the first operational system was installed in LCLS September 2009.[4, 5]

The system modulates an RF reference signal on 1550 nm CW light, and transmits the modulated light over optical fiber. The optical phase delay change through the fiber is measured by a Michelson interferometer and the beat signal is transmitted over another fiber to the receiver side. At the receiver, a synchronization head (sync head) is placed close to the device under control (DUC). The RF reference signal is detected by a photo diode in the sync head and the photo diode is operated at a working point where there is low AM/PM modulation. The RF phase of the reference and DUC are measured by an FPGA-based phase detector [6] in the receiver chassis. The phase variation on the coaxial cables between the receiver chassis and sync head is measured and cancelled by a double side-band suppressed carrier calibration signal. One special receiver is placed next to the beam arrival time monitor (a resonant cavity excited by the electron bunch passing through). The 476 MHz reference signal delivered to the transmitter is shifted such that the received signal follows the average beam arrival time.

As LCLS experiments have developed, more lasers in different hutches require this level of precision timing. Under the collaboration between SLAC and LBNL, we expanded the system to control different kinds of lasers used in LCLS experiments by making the following upgrades:

- upgrade the sender to 16 channels
- upgrade the receiver chassis and sync head RF electronics from connectorized components version to PCB version
- upgrade the EPICS software user interface
- install receivers for 3 end stations in the near-end hall (NEH) and 2 end stations in the far-end hall (FEH)

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## SENDER CHASSIS

The sender amplifies the RF modulated light, and splits it to multiple channels. For each channel, the short arm of the Michelson interferometer and the Faraday rotator mirror are integrated in this chassis. Since the fiber length in the multi-way splitter and the short arm of the interferometer are not actively compensated, we need to maintain good temperature control in the sender chassis.

The new sender is manufactured by Emcore Corporation. This is a 16 channel sender, with 10 mW light power output in each channel.

## RECEIVER CHASSIS AND SYNC HEAD

The PCB version of the RF circuitry in the receiver and sync head has been designed and fabricated to simplify assembly. Figure 1 and Figure 2 show the pictures of the new sync head and receiver chassis. The following boards have been designed,

- Receiver up converter board
- Receiver down converter board
- Receiver LO board
- Receiver beat signal board
- Sync head RF combination board


Figure 1: Receiver chassis.

## Sync Head RF Combination Board

The sync head is installed close to the device under control, because the cable length variation between the sync head and DUC is not actively or passively compensated. The sync head contains the far end of the Michelson interferometer and an optical frequency shifter. The sync head detects the reference signal from the fiber using a highspeed photo diode. The reference RF signal and the DUC RF signal are combined with the double side band suppressed carrier calibration signal and sent to the receiver chassis.


Figure 2: Sync head picture.

The sync head RF combination board can accomplish its basic function, but we measure cross talk of -70 dB between the reference channel and the DUC signal channel. Tests have indicated this adversely affects the timing stability. We will develop a new version of this board to improve cross talk.

In the first delivered system, the RF components used SMA connectorized parts, requiring more tuning during assembly. Together with our SLAC collaborators, we designed PCB boards to implement the same functions. For the receiver chassis, there are 5 kinds of boards that have been developed.

## Up/Down Converter Board

The signals between the sync head and receiver chassis are in the RF/microwave frequency band $(50 \mathrm{MHz}$ to 3 GHz ). The digital processing board processes IF frequency signals. The up/down converter boards are designed to convert the S-band signals down to 50 MHz frequency. Figure 3 shows the pictures of the up/down converter.

The incoming reference and DUC signals from sync head contain the main S-band signals $\left(f_{R F}\right)$ and calibration side bands $f_{R F} \pm 1.75 \mathrm{MHz}$. The reference signal contains another two side bands at $f_{R F} \pm 4.25 M H z$ to be used to correct bucket ambiguity, e.g. allow selection of the right RF cycle corresponding to an optical pulse from the laser. The outgoing signals to the sync head are the AOM (optical frequency shifter) drive signal and calibration signal. The AOM drive signal is a single 50 MHz frequency and the calibration signal has both upper and lower side bands.

The existence of multiple frequencies requires the up/down converter to operate in its linear range. We also require low crosstalk between outgoing calibration signals and incoming signals, and low crosstalk between the reference and DUC signal channels.

The new PCB implementation encloses the boards separately to achieve high isolation between signals. The input signal power level of the up/down converter is limited to remain in the linear range, and high IP3 components are chosen to achieve high linearity.


Figure 3: Down converter (a) and up converter(b).

## Beat Signal Board

The beat signal board contains a photo diode to detect the beat signal from the Michelson interferometer. The phase of the beat signal in the RF band contains phase information about the optical signal. The board also contains RF amplifiers, attenuators and couplers to condition the beat signal to be processed by the LLRF4 board. In this enclosure, an optical isolator is used in front of the photo diode, to prevent interference with the main signal.

## LO and Clock Generation Board

This board takes in the 1400 MHz signal generated by the Wenzel oscillator and frequency multiplier, doubles the frequency to 2800 MHz and fans out to the LO port of each up/down converter. It also distributes the clock signal to the LLRF4 board. The isolation among different LO output ports needs to be high and the VSWR of each port should be optimized to minimize cross talk of different up/down converters through the LO channel.

## SOFTWARE AND USER INTERFACE

The original user interface provided access to all the process variable (PVs) of the input/output controller (IOC) and accessed all the registers of the FPGA, and was not engineered for operator daily use.


Figure 5: LCLS femto second timing system configuration.


Figure 4: Femto second timing system GUI a)system overview b)operator gui c)detail data logging.

The new GUI has three layers of operation. The top layer is integrated with the laser control system reporting the health of each end station, as shown in figure 4 a . The second layer is the operator layer as shown in $4 b$, containing buttons for normal operation, for instance, open/close loop, do bucket correction, add phase shift between reference and DUC. A vector diagram of important signals and the loop status also shown in this level of the GUI. The third layer is a short history of important signals, and some of the signal analysis like rms calculation etc.. This layer helps users quickly locate problems. For long term data recording, the PVs name are changed to follow the LCLS conventions and are archived by EPICs integrated with the LCLS data archiver.

## INSTALLATION ON LCLS

Figure 5 shows the current femtosecond timing system configuration in LCLS. The new sender was installed in the NEH laser room early in 2011. Eight sets of receivers and sync heads were manufactured by Ron Akre's group in SLAC. Four of them have been tested and installed in the SXR, XPP, CXI and MEC experiment hutches. Two original receivers are still running in the undulator hall and AMO station.

## SUMMARY

The timing transmitter in LCLS has been upgraded to 16 output channels. The receiver and sync head have been upgraded to PCB version of RF circuitry. Four sets of receivers and sync heads have been installed.

In order to optimize system performance, we plan to install a modelocked laser oscillator in LBNL together with a new receiver and sync head to further fine tune the laser and control system.

A new software and firmware development platform has been developed and we plan to migrate the LCLS femtosecond timing control firmware and software to the platform.

The crosstalk in the sync head will be reduced by improving the PC board design.

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