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SLAC8's - A DISTRIBUTED ACCELERATOR CONTROL AND MONITORING SYSTEM*

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Summary

The latest addition to our distributed accelerator control and monitoring system is described which achieves parallel control of multilevel functions, multisector access as well as continuous updating of over 800 analog signals. The limitations of the preceding system are compared with the advantages of this larger network. Interface hardware and diagnostic software for the computers is also discussed.

Introduction

Control Room consolidation was first achieved in 1971 using an existing SDS 925 with an operator-machine interface (the touch panel) linked to a PDP9 which interfaced to the accelerator control and monitoring system.[1,2] As the number of beams and the difficulty of running these beams increased, additional beam operator positions were added in Main Control (MCC). In addition, multiple beam guidance devices were added along the accelerator. It was soon obvious that an increase of the number of control channels would be required. The solution that was implemented was to install a communications computer in the Accelerator Control Room (CCR) which communicated with the PDP9-SDS 925 as well as eight new computers (PDP8's) located along the two mile Klystron Gallery (see Fig. 1). Controls thus originating on the touch panel are sent via the SDS 925-PDP9-PDP8/e to the appropriate PDP8/f and then to the device.[3] A status signal, if present, is read by the PDP9 and sent on to the SDS 925 Touch Panel. An analog voltage, if present, is read continuously by the local PDP8 and sent to the touch panel on demand. If a gallery computer fails, the PDP9 takes control in those sectors. This action is automatic and is reasonably transparent. The operator will, however, notice the lack of parallel control (the simultaneous control of multi-level devices) or an analog that is read by the PDP9 instead of a PDP8. If either the SDS 925 or the PDP9 fails, manual operation is still possible at both MCC and CCR.

System Prior to the PDP8's

The PDP9, as interfaced to the accelerator control system, had one output port. This was done (historically) to preserve two-thirds of the manual control in CCR which existed since the accelerator was built. The PDP9 was seen as an aid to the operator and not a funnel through which all controls must flow. Analogs which were sent from the gallery were read by a single ADC in CCR. The long signal runs required heavy line filtering with the attendant slowing of analog response. The status system, by reason of its initial design, could be easily read into the PDP9. Computer patterns (trigger gates) are generated only in the PDP9.

As more simultaneous beams were required (up to 8 at some periods) and the beam requirements became harder to meet (wider energy and current spreads), multilevel pulsed beam guidance devices were added. Thus, instead of controlling one dc focussing magnet, an operator had available up to six adjustable magnet currents which could be assigned to six beams.

Expanded Control System

The computers along the gallery have been situated so that they serve four sectors except for the first computer which serves the injector, sector 1 and sector 2. This was necessary because of the large number of signals to be controlled and read in the injector area. Each computer has been linked to the CCR (PDP8/e) via a wire pair data link. Data speeds of 9600 baud have been sent and received over the various length wire (up to 10,000 feet). EIA levels of ±10 volts are used to drive the wire pairs directly. Receivers are implemented using differential op-amps. Data tests have been run for hundreds of hours in each of these links with no data transmission failures noted.

The gallery PDP8's provide simultaneous access to each level of a multi-level device and in addition to one other selected control in that sector (see Fig. 2). Six level beam guidance devices have been installed at the injector and from the 1/3 point through the remainder of the accelerator. Typical devices are pulsed vertical and horizontal steering, pulsed quadrupoles and pulsed beam loading, as well as a pulsed phase shifter at the injector and a pulsed energy vernier device in sector 27. It is now possible to operate one control in each sector while operating any of these multi-level devices simultaneously.

Analogs are continuously scanned by the local computer. Provisions have been made to read and store up to 32 analog signals from each sector and in CCR (see Fig. 3). The injector analog system is designed to read and store up to 128 analogs. Signal conditioning is provided to accomodate 0 to 1 volt, 0 to 5 volt and ±1 volt signals. The analog multiplexer inputs are high impedance so that signal loading is negligible.

Maintenance switches have been provided so that a sector or a group of sectors can be switched back to PDP9 control and monitoring. Computer or interface repair is, therefore, easily done while the accelerator is operating with a negligible inconvenience to the accelerator operators. Automatic fallback to the PDP9 is initiated if a PDP8's RUN circuit indicates the program has halted or if the program fails to reset a 360 pps synchronization flag.

Diagnostic Programming

A stand-alone program has been written for each interface. These programs have been used to develop the hardware (and vice versa) as well as to checkout and later "certify" the interface after a repair has been made. A paper tape reader, interface card, tapes and program listings have been assembled in one package so that maintenance and checkout can be accomplished at the local computer. Short "quick-check" programs are also provided as well as "scope loop" programs to speed up maintenance of the system.

References

1. K. Breymayer et al, "SLAC Control Room Consolidation Using Linked Computers," SLAC PUB 866, March 1971.

2. W. Struven, "Control and Monitoring of the SLAC Accelerator Utilizing a PDP9 System," SLAC PUB 592, April 1969.

3. W. Struven, "Experience with Touch Panel Control at SLAC," SLAC PUB 1191, March 1973.

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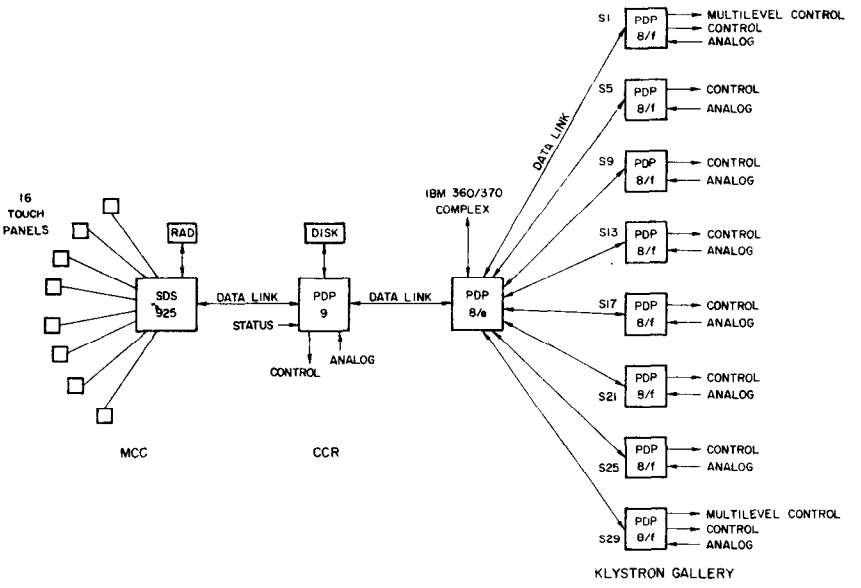
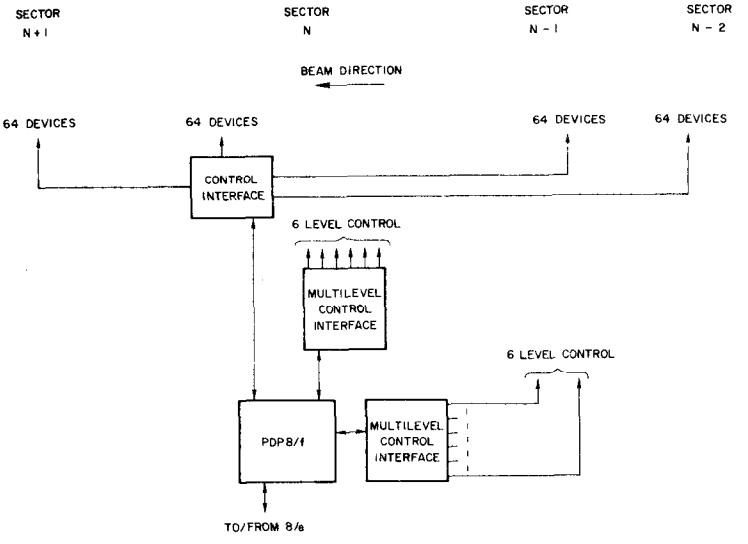


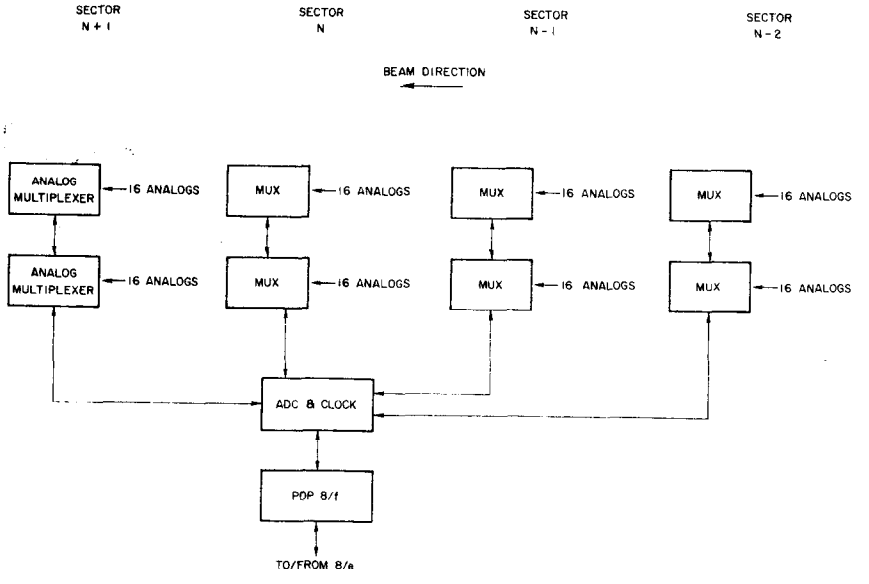
COMPUTER BLOCK DIAGRAM

Fig. 1



COMPUTER CONTROL

Fig. 2



COMPUTER ANALOGS

Fig. 3