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A NEW SINGLE WIRE READOUT SYSTEM FOR SPARK CHAMBERS*

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ABSTRACT

A new, conceptually very simple, single wire readout system for spark chambers in strong magnetic fields is described.

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Introduction

We have designed and built an individual wire readout system for use in a 10,000 wire cylindrical spark chamber assembly. The spark chambers are located around the 1 meter long liquid hydrogen target of LASS, the Large Aperture Solenoid Spectrometer at the Stanford Linear Accelerator Center, in a 25 kG magnetic field, as shown in fig. 1. This location leads to requirements of high reliability and small physical size of the readout electronics. In addition, to insure good multispark efficiency in the region of high spark density close to the target, a narrow spark width, preferably over a wide plateau in high voltage, is required. This has been achieved by limiting the voltage difference between adjacent wires due to a spark on one of them to $\leq$ 100 V. In some readout systems, such a limitation does not exist, and as a consequence, very wide spark phenomena are observed when the voltage is raised much above the onset of the plateau.

Circuit operation

The basic spark detecting circuit is depicted in fig. 2. Apart from the extra capacitor C_2 on the high voltage (anode) wire readout, the ground and high voltage wire readouts are essentially identical. The spark current charge up capacitors C_1 and C_1' to a voltage determined by the voltage drop in the 1Ω resistors, R_0, due to the spark current, typically -40 V. We have chosen to arrange the components of these rectifying circuits, consisting of the 1N3070 diode, R_0, and C_1 or C_1' so that a spark will create a negative signal on both anode and cathode circuits. Rectification eliminates a problem we have observed with some nonrectifying circuits: The sign and magnitude of the final charge on a storage capacitor was dependent on the shape of the high voltage pulse and ringing of the spark current. Notice also that the voltage difference between adjacent wires, one of which has been hit by a spark, is limited to typically ~ 40 V, the voltage drop across R_0 due to the spark current. This is too little to cause breakdown between wires. This is the reason that we observe minimal increase in the spark width over a wide voltage range (fig. 4).

Because of the reverse biasing of the diode, the capacitors C_1 and C_1' stay charged after the high voltage pulse has subsided. In fact, they discharge with a characteristic time of several hundred microseconds, determined by the RC filter which connects the rectifying circuit with the input of the shift registers. The advantage of using shift registers for readout of spark chambers has been pointed out by Nunamaker[1)]. After times of 200 and 450 μs for the cathode and anode readouts respectively, a parallel load pulse is applied to the shift registers. The inputs are biased by V_{bias} to the high state ($V_{input} \geq 2.4$ V), but a spark on a wire will cause the corresponding input to go low ($V_{input} \leq 0.8$ V) with the minimum value occurring at the time of the load pulse. The negative polarity of the input signals allows a large range of signal size, since the input of the shift register is clamped by an internal diode.

With 10,000 wires, we have a 10,000 bit shift register, which in practice has been divided into two independent shift registers, one for the anode wires and one for the cathode wires. After these two shift registers have been parallel loaded, they are shifted out serially at a 4 MHz clock rate, by a "controller" which records the position and width of each "spark" in the chain, identified by one or more bits set to the low (logical 0) state. This information is subsequently transmitted to a PDP-11. In order to check the performance of the long shift register chains, a "fiducial" 8 bit shift register has been introduced between the shift registers of each cylindrical surface and after the last surface. Each 8 bit fiducial is hard-wired to give the bit pattern 01111110, and will thus read out as a spark with fixed position and a width of 6 "wires". Checking that all fiducials are in the right positions certifies that the registers are shifting correctly.

Let us now return to the function of the RC filters in fig. 2. Because of the very long time constants of the filters, it is easy to physically separate the shift register end from the rectifying circuits. In our case, this has been done by separating R_1 and R_2 by 8 meters of unshielded cable. In this way, the "fast" part of the circuit which detects the spark current is placed directly on the spark chamber, while the "slow" part, including the shift register, is placed at a convenient location away from the spark chambers. In doing this, we have traded the disadvantage of having to handle 10,000 8 meter long wires for the greater accessibility of most of the components. Resistor R_1 in the cathode circuit damps the ringing of the 8 meter long cables due to the high voltage pulse, which otherwise is rectified and simulates a spark. The "crosstalk" between adjacent wires over a length of 8 meters due to their mutual capacitance is too small to cause trouble.

Finally, the extra capacitor C_2 on the anode readout is needed to reduce the size of the positive signal at the shift register input arising from the high voltage pulse. The signal at the shift register is $\sim$1 V for a 4 kV high voltage pulse. The full high voltage appears across R_1, a 1/2 watt composition resistor, but there has been no trouble breakdown.

We have arranged it so that the whole anode readout system can float with respect to true ground, which allows us to easily apply a clearing field between anode and cathode wires. In order to accomplish this, the clock, load, and serial data signals of the shift registers pass through optical isolators on their way between shift registers and "controller" [2).

Construction

The spark chamber system is arranged as five cylindrical chambers with diameters ranging from 20 cm to 118 cm, each 90 cm long. Each chamber has two gaps in which both cathode surfaces and one anode surface are read out, thus providing a total of fifteen surfaces. The surfaces are mylar cylinders, on which 0.125 mm diameter Cu coated Al wires have been glued with Scotchcast resin[3]. The wire spacing is 2 mm and the gap between the cylinders is 1 cm. The chambers are built to determine the ϕ angle (the angle in a plane perpendicular to the axis) with good accuracy and the z-coordinate (along the axis) with less accuracy. In order to do this, the first gap of each chamber has the wires in its two surfaces crossed at a small relative angle δ given by $\tan\frac{\delta}{2} = 1/10$, to produce "small angle stereo". This gap thus measures both ϕ and z with, respectively "good" and "bad" resolution, except for the ambiguities resulting from multiple sparks in crossed wire systems. These ambiguities are resolved by the second gap, in which one surface of purely axial wires is read out. The upstream and downstream ends of the system are sets of concentric rings, which determine the position and spacing of the cylinders. The downstream rings are made as a sandwich of mylar and styrofoam, while the upstream rings are lucite. The "rectifying" circuits of the readout are on PC boards, shaped into rings of the right size and mounted on the lucite rings, as shown in fig. 3.

The $\sim$300 nanosecond long, $\sim$4 kV, positive high voltage pulse is applied to the chambers by discharging coaxial cable through a hydrogen thyratron. A standard LBL-Berkeley design gas cart controls and purifies the gas flow. The gas mixture used is 90% Ne, 10% He and 0.25% ethyl alcohol added by bubbling the total gas flow through ethyl alcohol at -25°C. The gas circulates through holes in the mylar cylinders, punched in alternating ends of the chambers.

Performance

Our initial tests of chamber performance in beams at SLAC have shown us two areas of difficulty. First, some of the chambers have variations in the gap size, resulting in azimuthally varying chamber-efficiencies. These are being rebuilt. Second, subjecting the chambers to ~ 2000 sparks/wire has resulted in failure of $\sim 1\%$ of the rectifying circuits. The contributions of each type of component failures are as follows:

Table 1

Component	Anode Circuits	Cathode Circuits
1N 3070 open	.06%	.03%
1N 3070 short	.4%	.2%
C_1 or C_1' open	Not measurable in circuit	.2%
C_1 or C_2 leaky, or C_1' leaky	.2%	.03%

These failures occurred in spite of component tests before assembly. New failures have steadily decreased with time so we do not expect the final failure to be much worse than 1%.

The performance of one chamber, with a uniform gap width is summarized in figs. 4 and 5. Figure 4 shows the average number of bits set per spark. This number is quite low, and remarkably independent of the applied voltage, which is very useful in a region of high spark density. Figure 5 shows the chamber efficiency as a function of high voltage for tracks in a plane perpendicular to the cylinder axis. These tracks cause two sparks in each gap, separated by 180°. Notice the rapid rise of the chamber efficiency to its plateau value.

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References

1. Thomas A. Nunamaker, Rev. Sci. Instr. 42 (1971) 1701.

2. Hewlett Packard HP 5082-4360.

3. Scotchcast 221, manufactured by the 3M Company.

Figures

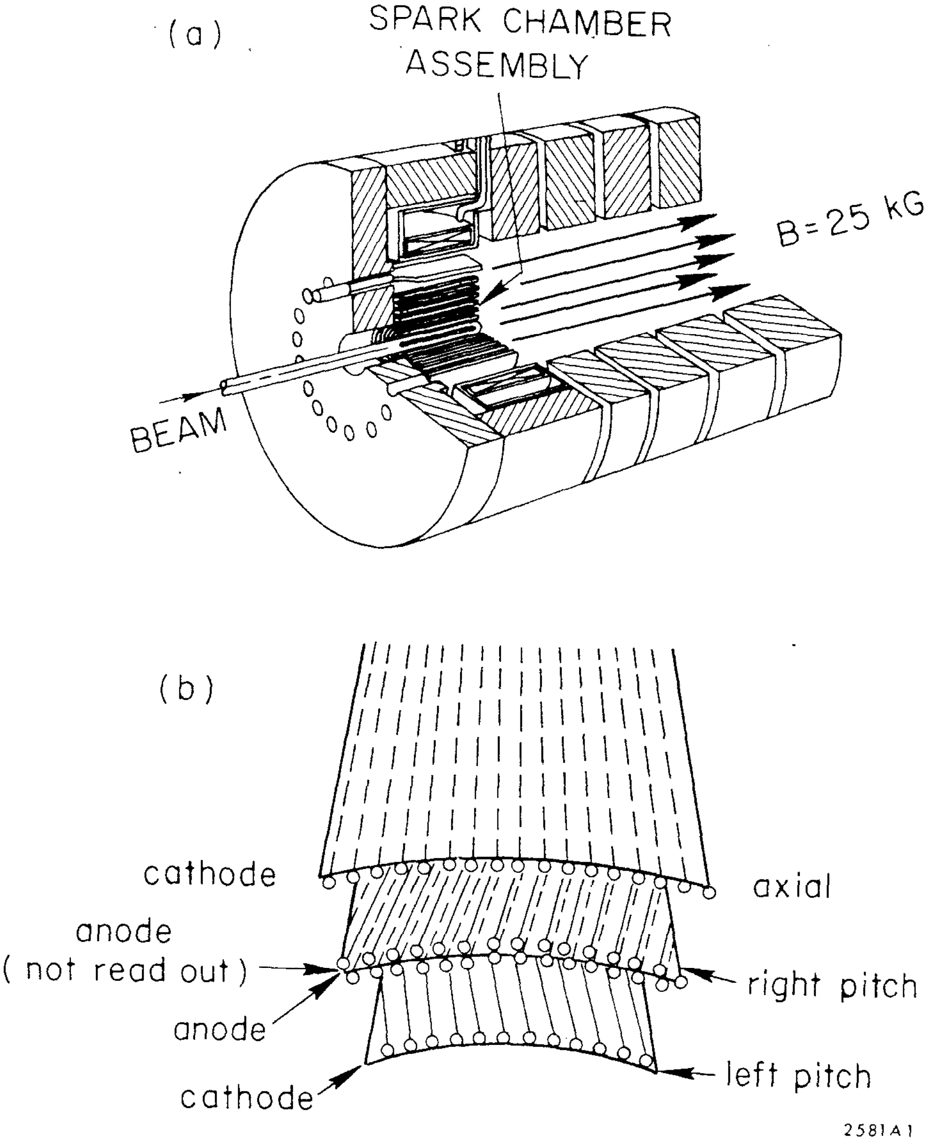

(a)
SPARK CHAMBER
ASSEMBLY
B=25 kG
BEAM
(b)
cathode
axial
anode
(not read out)
right pitch
anode
cathode
left pitch
2581A1

Fig. 1

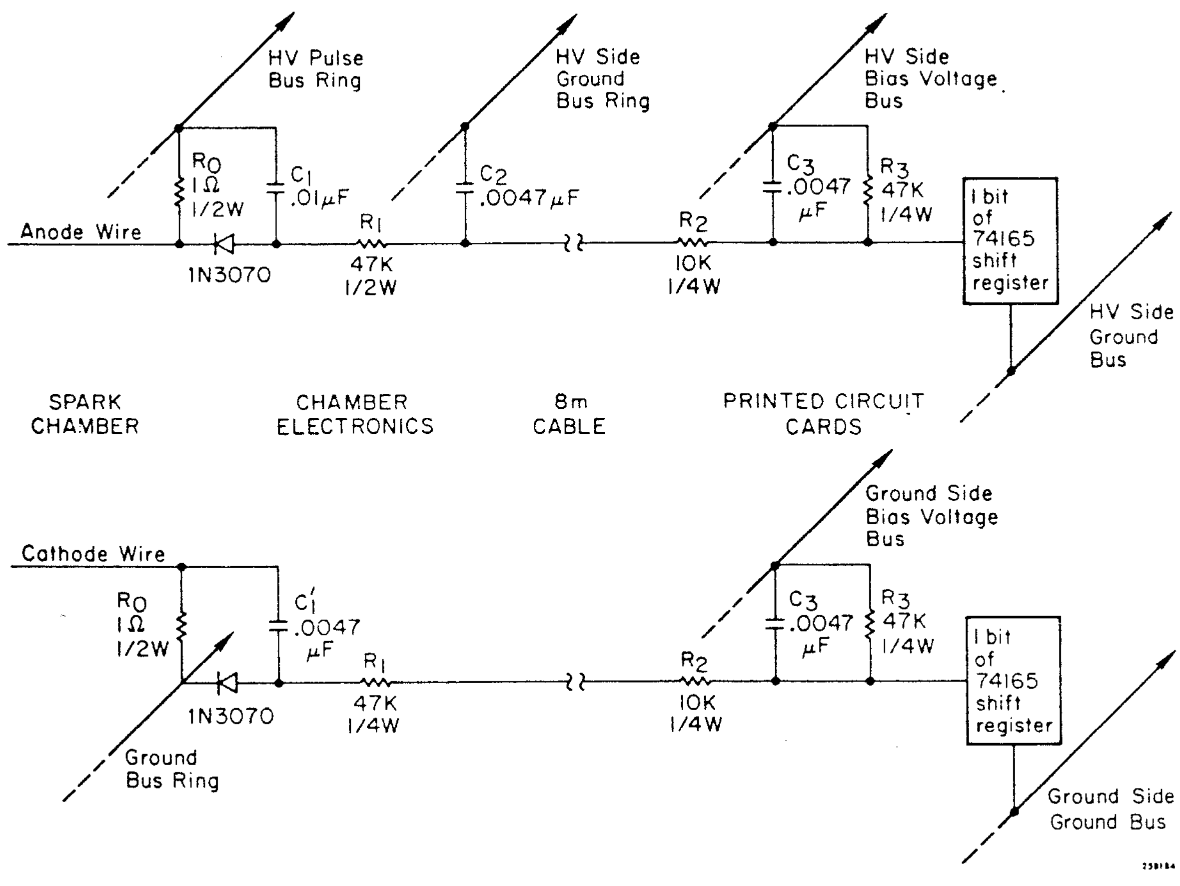
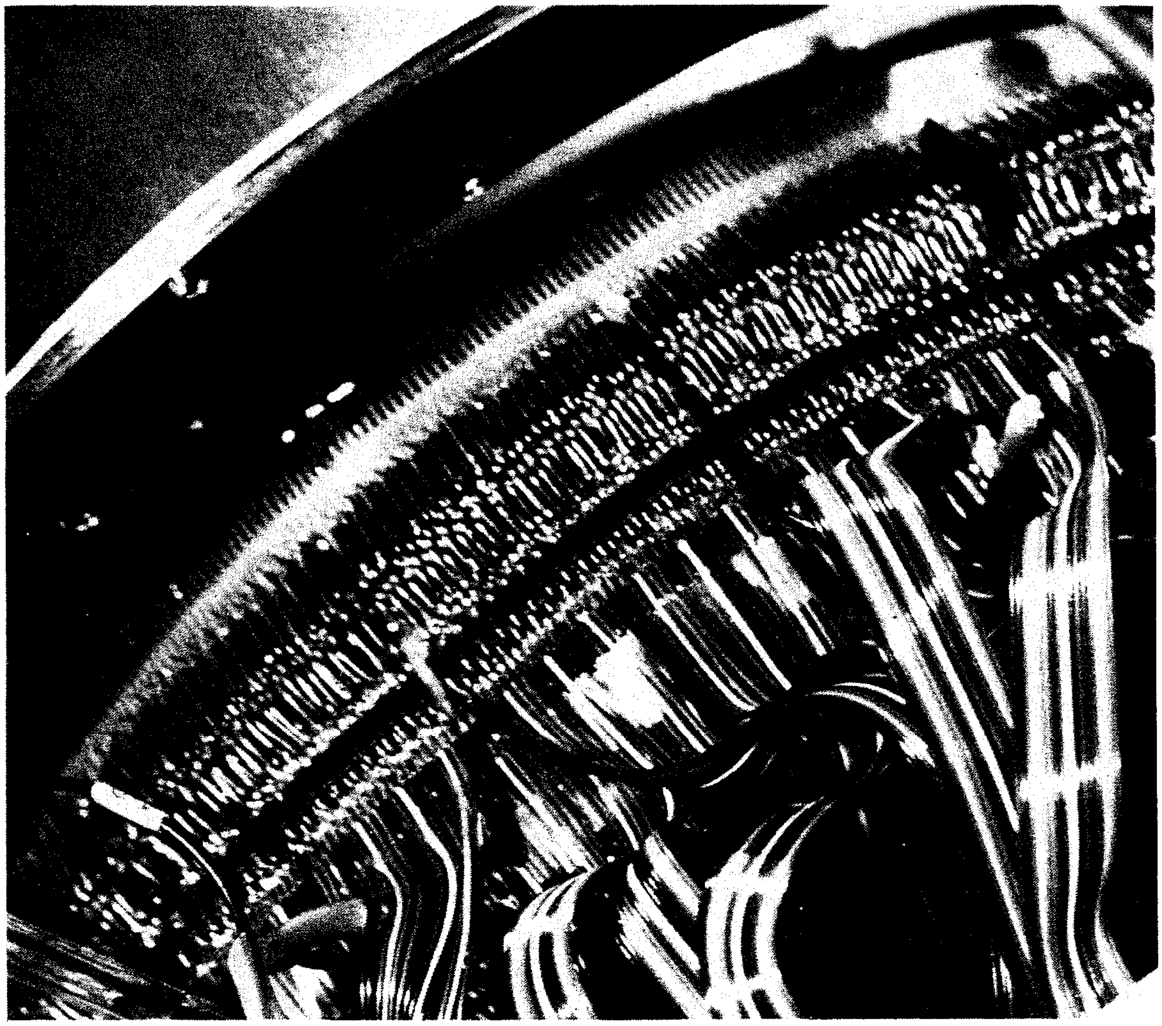
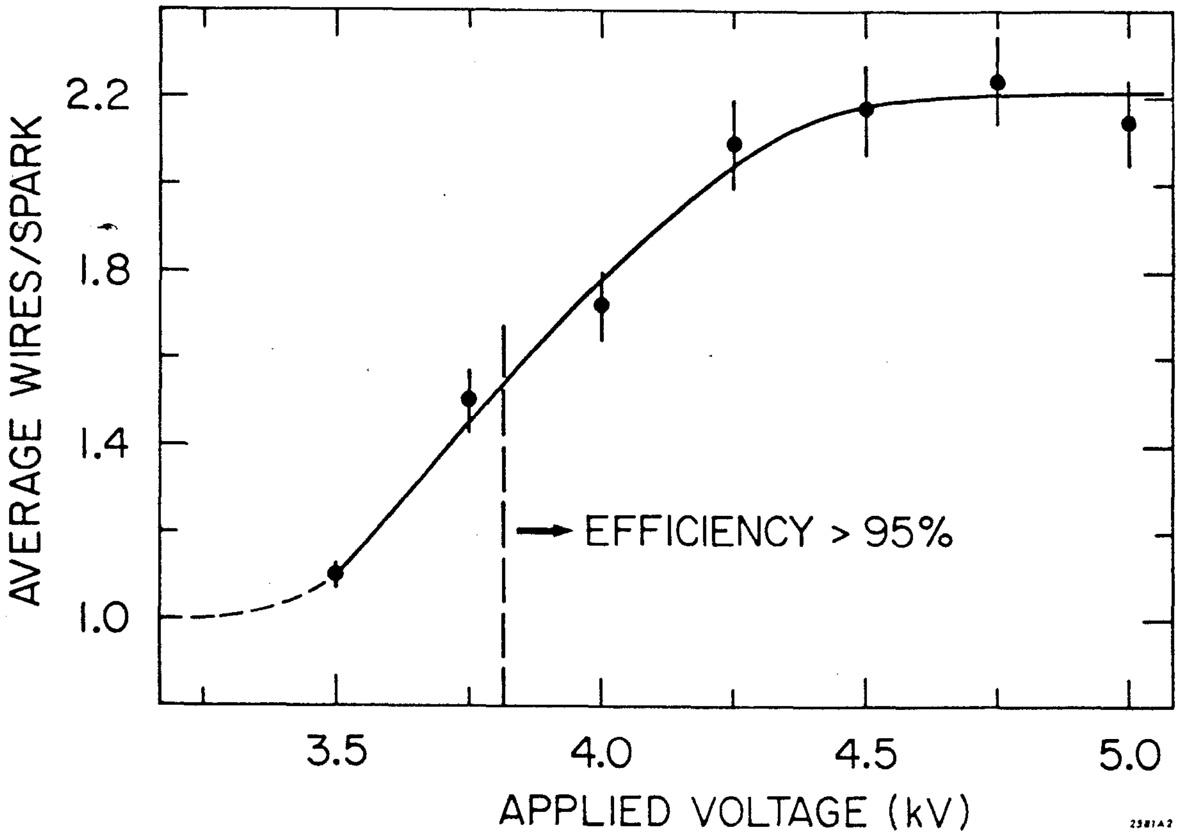

HV Pulse Bus Ring
HV Side Ground Bus Ring
HV Side Bias Voltage Bus
R0 1Ω 1/2W
C1 .01μF
C2 .0047μF
C3 .0047 μF
R3 47K 1/4W
Anode Wire
1N3070
R1 47K 1/2W
R2 10K 1/4W
1 bit of 74165 shift register
HV Side Ground Bus
SPARK CHAMBER
CHAMBER ELECTRONICS
8m CABLE
PRINTED CIRCUIT CARDS
Ground Side Bias Voltage Bus
Cathode Wire
R0 1Ω 1/2W
C1' .0047 μF
R1 47K 1/4W
1N3070
Ground Bus Ring
R2 10K 1/4W
C3 .0047 μF
R3 47K 1/4W
1 bit of 74165 shift register
Ground Side Ground Bus

Fig. 2



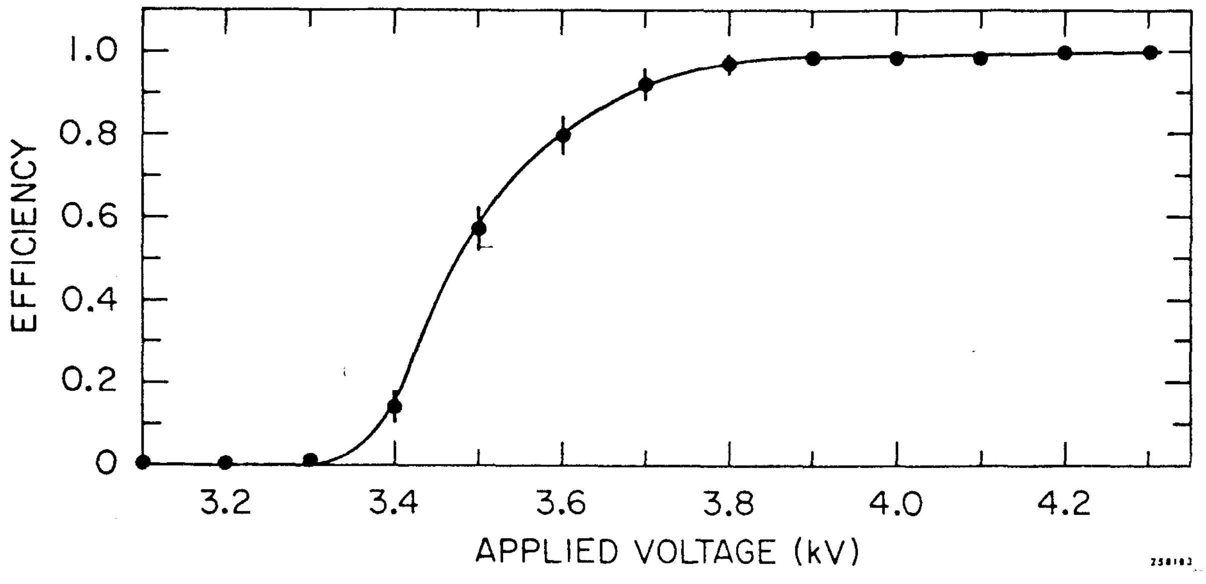
2581A5

Fig. 3



AVERAGE WIRES/SPARK
2.2
1.8
1.4
1.0
EFFICIENCY > 95%
3.5
4.0
4.5
5.0
APPLIED VOLTAGE (kV)

Fig. 4



EFFICIENCY
1.0
0.8
0.6
0.4
0.2
0
3.2
3.4
3.6
3.8
4.0
4.2
APPLIED VOLTAGE (kV)

Fig. 5