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# The FE-I4 Pixel Readout Chip and the IBL Module

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FE-I4 is the new ATLAS pixel readout chip for the upgraded ATLAS pixel detector. Designed in a CMOS 130 nm feature size process, the IC is able to withstand higher radiation levels compared to the present generation of ATLAS pixel Front-End FE-I3, and can also cope with higher hit rate. It is thus suitable for intermediate radii pixel detector layers in the High Luminosity LHC environment, but also for the inserted layer at 3.3 cm known as the "Insertable B-Layer" project (IBL), at a shorter timescale. In this paper, an introduction to the FE-I4 will be given, focusing on test results from the first full size FE-I4A prototype which has been available since fall 2010. The IBL project will be introduced, with particular emphasis on the FE-I4-based module concept.

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## 1. The FE-I4 Project and the ATLAS Pixel Upgrades

ATLAS is one of the 4 main detectors located on the LHC ring in CERN, Geneva. The central element of ATLAS is its pixel detector, crucial not only for the detection of displaced vertices, but also for high quality and efficient track reconstruction. LHC has started operation at a center of mass energy $\sqrt{s} = 7$ TeV, and has already reached in the first half of 2011 a peak luminosity of $2\times10^{33}$ $cm^{-2}s^{-1}$, with the machine performing so far very well. According to the latest machine schedule, a first long shutdown will take place in 2013 to prepare the machine to run at design energy $\sqrt{s} = 14$ TeV and nominal full luminosity of $10^{34}$ $cm^{-2}s^{-1}$. During this shutdown, a fourth pixel layer will be inserted inside the present pixel detector. The "Insertable B-Layer" (IBL) [1] will improve tracking and b-tagging, and could also compensate for degradation of the current pixel system (e.g. radiation induced damage, inefficiencies at increased luminosity, component failures). In 2017-2018, a second long shutdown called LHC Phase-I Upgrade will take place, to prepare the machine for increased luminosity running (L = $2\times10^{34}$ $cm^{-2}s^{-1}$). The scope of the changes that will be brought to the inner tracker at this occasion is still subject to debate. The replacement of the complete pixel detector by a new pixel detector based on IBL experience and technologies is under consideration. The FE-I4 project has to be understood in the context of these 2 upgrades.

The limitations of the current ATLAS pixel Front-End FE-I3 [2] -in particular for what concerns radiation hardness and its ability to cope with high hit rates- have been realized a few years ago [3] and have led to the development of a new IC series in a smaller feature size, the FE-I4. With respect to previous Front-End generations, the FE-I4 shows an increased tolerance to radiation which mainly comes from using only the thinner gate oxide transistors which are offered in the 130 nm CMOS process. In FE-I4, it is also the first time that the new digital pixel architecture based on "4-Pixel Digital Region" has been implemented. This innovative pixel organization is particularly important for high rate applications. A first full scale test IC called FE-I4A has been submitted during the summer 2010, and will be described in Section 2. A description of the Pixel Digital Region will be given in Section 2. FE-I4A's periphery hosts many analog and digital blocks, some used to control communication to the IC or to control the data output from the IC, some to provide extra testing capabilities for the prototype, others related e.g. to the testing of various powering schemes. The periphery will be introduced in Section 2. In Section 3, a few test results will be shown and a few selected results on highly irradiated FE-I4A will be focused on. It is interesting to note that designing a bigger and more complex IC potentially leads to a simplified module concept, and the baseline for the IBL module will be shown in Section 4. Section 5 will finally focus on the development of the production version of the FE-I4 for IBL purposes, FE-I4B.

## 2. Development of the first full scale FE-I4 prototype

The development of the FE-I4 series is based on a rather simple starting point: the need for all future ATLAS pixel upgrades of a Front-End capable of coping with very high radiation

doses (above 250 MRad, which corresponds to approximately 3 years at twice LHC full luminosity for a pixel layer located at a radius r ~ 3.3 cm away from the beam) as well as coping with the high hit rate encountered in such environment. With an intrinsically high radiation hardness, good analog performance and easy access to the process through vendors and MPW brokers, the 130 nm feature size was identified as the technology of choice for this development. After an analysis of the various sources of inefficiency of the present ATLAS pixel IC, new possibilities for the digital architecture of the FE-I4 were compared [3] and the final structure of the digital pixel array was obtained. The new FE-I4 series is based on local in-pixel hit storage in 4-pixel digital regions and trigger propagation inside the array. The first full scale prototype FE-I4A consists of an array of 80×336 pixels with a size of 50×250 $\mu m^2$ organized in double-columns, and a periphery of height approx. 2 mm. It was developed in 5 institutes[1] which collaborate remotely using a commercial design library sharing platform [4]. A picture of the FE-I4A is shown in Figure 1a, together with a picture of the FE-I3 to scale (in Figure 1c) for comparison of the physical sizes of these ICs.

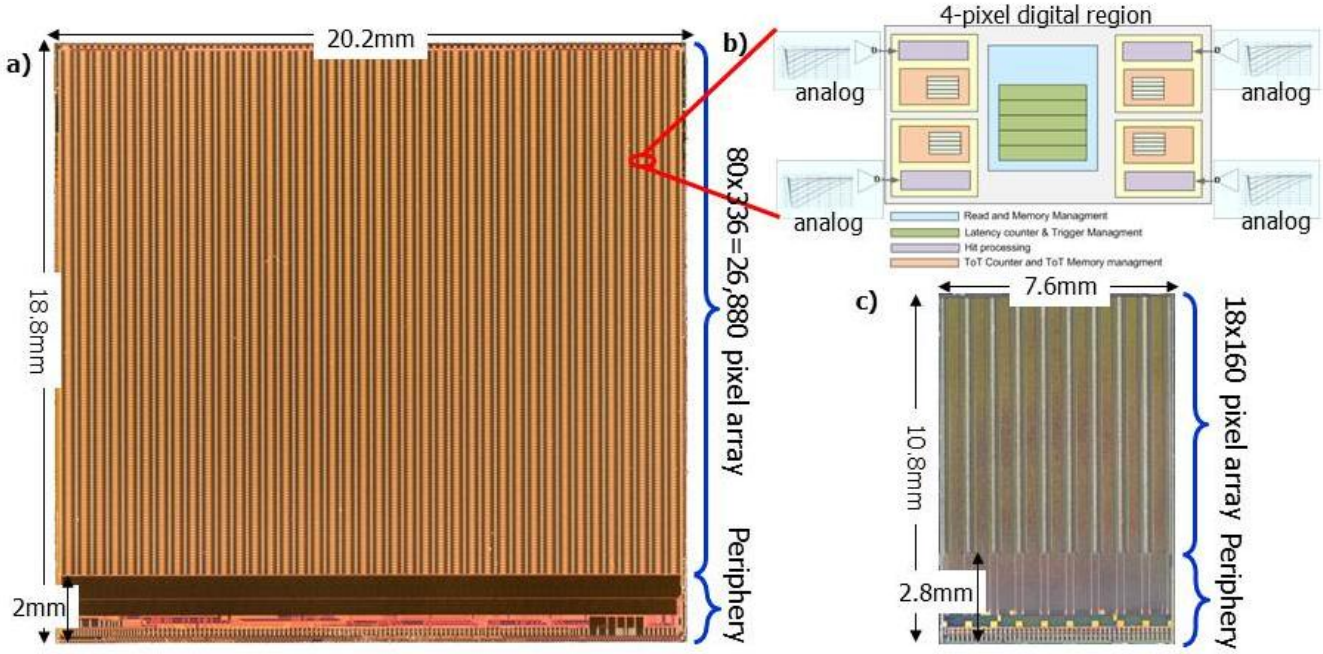


*Figure 1 a) Picture of the 20.2×18.8 $mm^2$ first full scale prototype FE-I4A. b) Zoom into the 4-Pixel Unit with its central 4-Pixel Digital Region (see Section 2.1 for more details). c) Picture of the 7.6×10.8 $mm^2$ FE-I3 currently used in the present pixel ATLAS*

### 2.1 FE-I4A 4-Pixel Unit

Figure 1.b shows a zoom into the 4-pixel unit, underlining the features of the 4-Pixel Digital Region (4-PDR). In this structure, 4 independently working analog pixels share a common digital blocks. The outputs of the 4 discriminators are fed to 4 separate hit processing units (in purple in Figure 1b) in which Time-Stamping and Time over Threshold (ToT, the pixel

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analog information) is processed. An extra level of digital discrimination can also be programmed, to distinguish large recorded charges from small ones. When one (or more) of the four hit processing unit detects a hit, the unit books one of the central latency counter (in green). Regardless of which of the four pixels has initiated the booking of the latency counter, four ToT memories for the four pixels will be associated to the event, thanks to a simple geographical association (1st latency counter corresponds to 4 1st ToT buffer memories, 2nd latency counter to 4 2nd ToT memories, and so on…). This architecture presents several advantages. First, the geographical proximity of the pixels inside the 4-PDR is efficient to record hits, as real hits come clustered. Second, it is advantageous in term of lowering the power used, as the un-triggered hits are not transferred to the periphery, and as some logic inside the 4-PDR is common to several hits at a time. Third, it is efficient in term of time-walk compensation, as one can use the digital discriminator to record a small hit (below digital discriminator threshold) with a big hit (above digital discriminator threshold) occurring in previous bunch-crossing, by simple geographical association. Finally, it also improves the active fraction of the IC as the memory is located at the level of the pixels, not in the periphery.

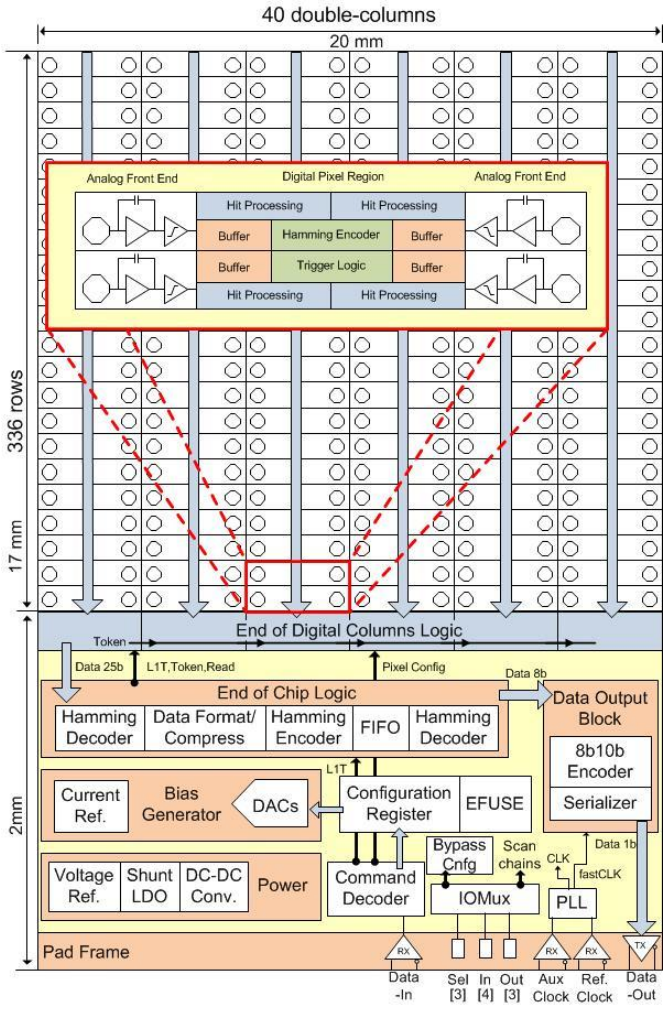


*Figure 2. The FE-I4A IC and its periphery*

The analog pixel is based on a two stage architecture, consisting of a preamplifier with leakage current compensation circuitry AC-coupled to a second stage of amplification. Each analog pixel hosts 13 configuration bits, to locally adjust the pre-amplifier feedback current, the discriminator threshold, and to allow test charge injection. Several pixel flavors were tested in FE-I4A, with variations in the implementation of the pre-amplifier feedback capacity, discriminator and local latch layout. The interested reader will find more information concerning the analog pixel in [5].

### 2.2 FE-I4A periphery

FE-I4A is the first 130 nm CMOS ATLAS pixel prototype full scale chip developed with the generic goal of fitting future ATLAS pixel upgrades. Given the short development time for the IBL project, it was also of prime importance to have in the FE-I4A an IC which requires only minor

modifications to fit the IBL needs. The periphery of the IC (see Figure 2) consists of a mixture of blocks, some needed for IBL operation, others providing extra testing capabilities (e.g. IOMux and bypass cnfg), and some finally that might be of use for a future ATLAS upgrade (e.g. the powering blocks). FE-I4A's periphery consists of an End of Chip Logic block which organizes trigger propagation, pixel hit formatting and does temporary hit storage, a Phase Locked Loop (PLL) Clock Generator block which takes the 40 MHz LHC machine clock and generates the 160 MHz clock necessary for 160 Mb/s data transfer, a Data Output Block which does 8b10b [6] data encoding and 160 Mb/s serialization, a Command Decoder which decodes Level-1 Trigger commands as well as the Global Configuration (then held in Configuration Registers) and the Pixel Local Configuration (held in memories at pixel level), and DACs used to generate biases based on the values stored in the Configuration Registers. For testing of various powering options, FE-I4A contains 2 Shunt-LDO voltage regulators, a device based on a shunt transistor (for serial powering applications) with extra Low Drop-Out regulation capability (see [7]). Integrated in the periphery is also a DC-DC divide by 2 charge pump converter. A more detailed description of FE-I4A's periphery is given in [8].

## 3. Performances of the FE-I4A: test results

FE-I4A was submitted to the foundry in the summer 2010, received in fall 2010 and has been extensively tested since then. Most of the testing done was performed with the use of a portable USB test system called USBpix [9]. The submission has been very successful, in particular for what concerns the performance of the analog pixel, the implementation of the 4-PDR array, the communication to the IC, the handling of the data output, control logic, formatting, buffering and high speed serialization. FE-I4A samples have been bump-bonded to planar silicon sensors, 3D silicon sensors and diamond sensors, and have been successfully operated in the laboratory, in cosmic data test stands and in test beams. In this section, a selection of few important test results is discussed.

The current consumed in the FE-I4A depends in first approximation upon only a few parameters. For the analog power, two main contributors are the biasing of the in-pixel preamplifier and of the discriminator. The digital power is in first order the sum of two contributions, one static and the other depending on hit rate. Typical laboratory or test beam values for operation of the FE-I4A at IBL occupancy are approx. 16 µW / pixel for analog power and 6 µW / pixel for digital power, which amounts to approx. 160 mW / $cm^2$. The typical value for the noise of the bare FE-I4A before irradiation is in the range 110-120 electrons ENC for 3000 electron threshold. For an FE-I4A bump-bonded to a planar silicon sensor or a 3D silicon sensor, the ENC would typically reach of order 150 electrons.

As anticipated, the IC designed in the 130 nm technology node resists well to irradiation. Three bare ICs have been submitted to 800 MeV protons in Los Alamos, USA, to doses of approx. 6, 75 and 200 MRad. Over this range, threshold dispersion is almost unchanged and noise increased by 15-25% in comparison to pre-irradiation values. The value for FE-I4A current reference has shown a maximal change of about 3%, but the trimming of the reference current needs to be shifted for the IBL production chip FE-I4B, as the desired current is at the limit of the FE-I4A trim range. Leakage current due to sub-threshold leakage in the switches

located in front of the in-pixel injection capacitors has increased in particular for the lowest tested dose of approx. 6 MRad, by a factor 4 to 5. The present FE-I4A pulse generator block has shown some limitations and early saturation when it comes to inject in parallel to many pixels at the same time, and this increased leakage current will be detrimental to operation (see Section 5 where a fix to this problem is suggested for the IBL FE-I4B).

It is interesting to note that assemblies with both planar sensors and 3D silicon sensors have also been exposed to high doses and could be operated with success in a test beam. In Figure 3a, low threshold operation is demonstrated, for both planar and 3D silicon assemblies irradiated to $5.10^{15}$ $n_{eq}$ / $cm^2$ proton irradiation in Karlsruhe, with noise occupancy figures around $10^{-8}$ per pixel per 25 ns for a threshold set to 1200 electrons (note that this conversion to electrons is known to a precision of about 10-20%). Figure 3b shows the fraction of noisy pixels after irradiation as a function of discriminator threshold. There is a baseline of pixels that must be masked of 2% for the planar assembly and 0.8% for the 3D assembly. These are pixels that were not flagged as bad before irradiation, but no longer function properly in digital tests. It should be underlined that the purpose of the irradiation was to test the sensor tolerance. A beam of 60 MeV protons was delivered to the sensor with the IC behind it, but with no calibration for the ionizing dose delivered to the IC. Due to expected Bragg peak, the ionizing dose may have exceeded 800 MRad, which is far above the design specifications. The IC was electrically floating during the irradiation. Also, due to time constraints to fit into an aggressive test beam schedule, no attempt for reviving the digitally dead pixels has been made. Nevertheless, it should be underlined that such low threshold operation with the big FE-I4A is one of the major successes of this enterprise, and of major importance for the sensor community, as it would extend the sensor life expectancy in particular for the post-irradiation planar sensors. This is an improvement with respect to the assemblies with FE-I3 used in the present ATLAS pixel detector, where typical lowest operational threshold are of order 2500e-.

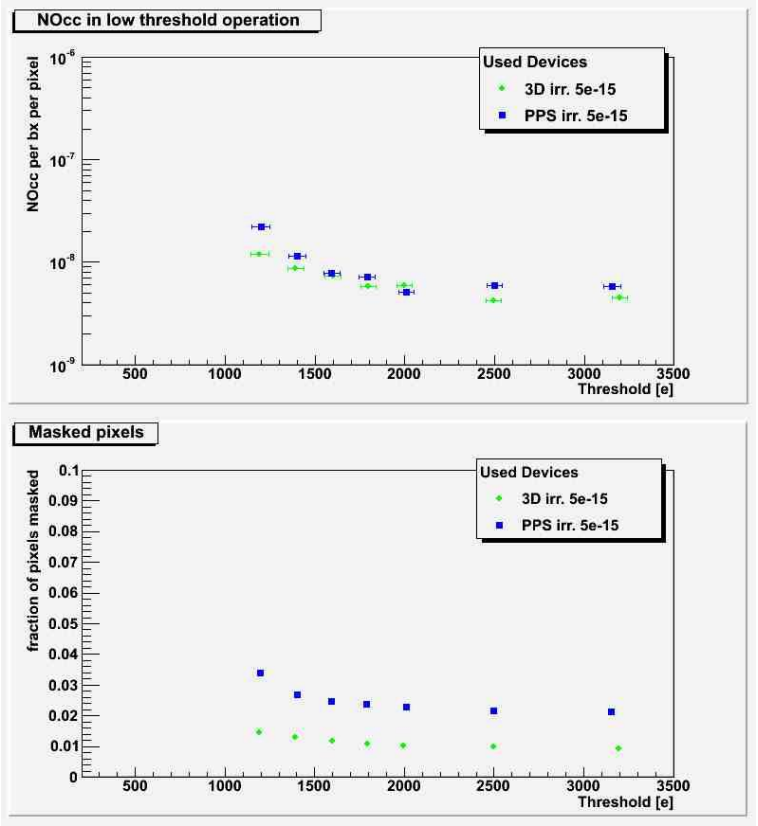


*Figure 3 a) Noise occupancy (per bunch-crossing and pixel) versus threshold (in electrons). b) Fraction of pixels masked versus threshold (in electrons), coming from two contributions: 1- Digitally un-responsive pixels whichever the threshold. 2- Pixels with noise occupancy above $10^{-5}$ per pixel per 25ns which would be masked in real operation. More details are provided in the text.*

For reasons related to the current ATLAS pixel system and the need to provide 160 Mb/s data output from the IBL FE-I4 to fit the high hit rate, a clock multiplier block was designed to cope with a 40 MHz input reference clock and deliver higher frequency clocks. The Clock Generator block is based on a PLL core (top part of Figure 4a) which generates multiple clock frequencies, coupled to a Multiplexer (MUX) section (bottom part of Figure 4a) enabling the selection of two output clocks which are then provided to the FE-I4A. The PLL architecture is that of a classical charge pump PLL, with Phase Frequency Detector (PFD), fed with the LHC bunch crossing nominal 40 MHz reference clock and the regenerated PLL clock, followed by a Charge Pump (CP) which upon detection of a sizable phase difference between the 2 input clocks of the PFD, can then adjust the voltage level of the Voltage Controlled Oscillator (VCO)

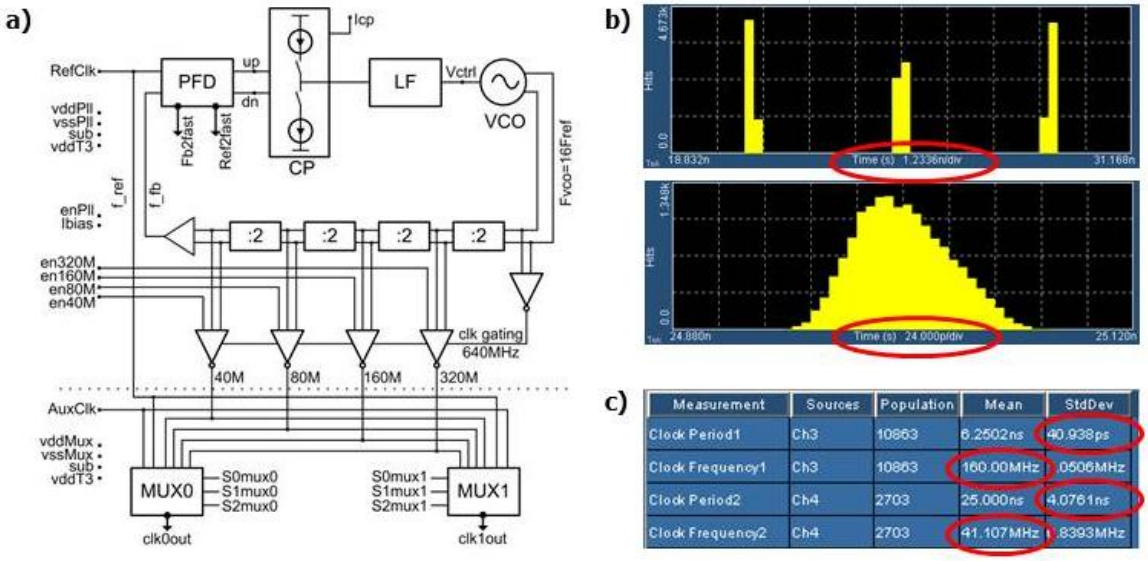


*Figure 4 a) Schematic of the Clock Generator bloc, with the core PLL loop on top and the 2 Multiplexers at bottom. b) Clock recovery from bad reference clock (test result): The top histogram shows the edges of the reference clock provided to the FE-I4A, where every second edge was delayed by 4 ns with respect to the nominal 25 ns bunch-crossing. The bottom histogram shows the Clock Generator output (please note change of scale, 1.23 ns/div for top histogram vs. 24 ps/div for bottom one). c) Screenshot of scope jitter software. More details are provided in the text.*

and hence tune its oscillation frequency (nominally 640 MHz). The fast VCO output clock is then divided down by 4 divider stages and finally fed back to the PFD. The 2 MUXes allow selecting between 6 clocks: Reference Clock, Auxiliary Clock (provided externally), or one of the nominal 40 MHz, 80 MHz, 160 MHz, 320 MHz clocks regenerated by the PLL. The CLK0_OUT is then provided to Data Output Block (DOB), whereas the CLK1_OUT is provided to the End of Chip Logic and the End of Double-Column Logic. The DOB uses a nominal 160 MHz clock single edge to do 8 bit to 10 bit encoding of the data stream and serialization before sending the data out through custom made pseudo-LVDS drivers. The stability of the clock is hence primordial. In Figure 4b, two jitter histograms show the results of testing the reaction of the Clock Generator block to a reference clock that was made purposely very jittery. In this test, the reference clock which was fed to the FE-I4A had every second edges displaced by 4 ns with respect to the nominal 40 MHz (top Figure 4b). The PLL helps recover a much cleaner clock as can be seen qualitatively in the bottom histogram in Figure 4b.

Highlighted in Figure 4c, the reader can see that the standard deviation of the period of the clock, as measured by the scope jitter analysis software, went from 4.1 ns for the reference clock (clock2) down to 41 ps for the 160 MHz cleaned-up clock.

Overall, after now about half a year of experience with the FE-I4A, either standalone in the laboratory, or bump-bonded to various sensors, in cosmic test stands, in test beams, or even under heavy irradiation, it appears that the IC is performing very well. Still, a few changes to the IC are deemed necessary to be able to use the FE as a production IC for the IBL: this topic will be covered in Section 5 devoted to the FE-I4B, after Section 4 devoted to the IBL module.

## 4. FE-I4 -based module for the IBL

The IBL is made of 14 staves, each of them consisting of an arrangement of 32 FE-I4s. The IBL module concept is eased by the use of the large size FE-I4 and a module concept which is indeed simpler than the current FE-I3-based module used in the present ATLAS pixel detector has been agreed on. The benefits of this simpler module concept are several: easier assembly, better testability, reduction of material. The 90% active fraction of the FE-I4 also enables the design of a low radial profile layer, as required for the IBL. The module unit is based on 2 FE-I4s adjacent along the LHC beam direction (z) which share clock and command inputs, but each one having independent data output. The FE-I4s require no extra active element to achieve functionality (no module control chip as is the case for the present FE-I3-based ATLAS pixel module). The building elements of the module are: the FEs, the sensor, the module flex and passive components. A sketch of the half module is shown in Figure 5, together with the preliminary placement for passive components on the half-module flex, with wire-bonds apparent between the flex and the FE-I4 and connection between the flex and the stave flex wing.

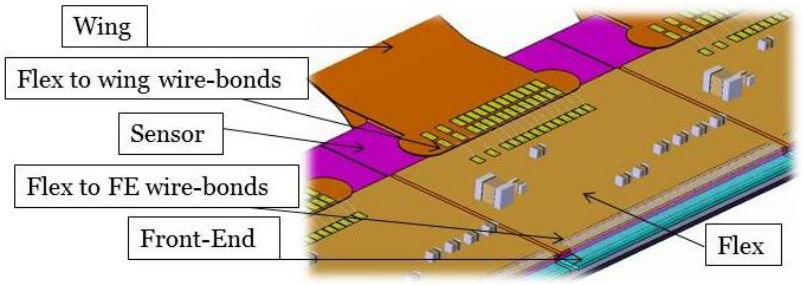


*Figure 5 Sketch of the arrangement of the half-module with flex, underlining tentative placement of passive components, wire-bonds and wing. More details are provided in the text.*

The choice of a sensor technology for the IBL has drawn a lot of R&D activity in the last years. Two technologies of choice have emerged, silicon planar n-in-n 200μm thick with ~200 μm slim edges and silicon 3D double-sided with full passing electrode and slim edges. Silicon planar n-in-n sensors are based on a very mature technology (actually these are sensors very similar to what is used for the current ATLAS pixel detector), with all the associated benefits: many qualified vendors at disposal, high yield foreseen, relatively low cost, experience with design optimization, usage of a mature radiation hardness model. The main challenges facing the planar technology come from the reduced charge collection after irradiation, which requires increasing the high voltage up to 1000 volts, and needs small effective threshold readout electronics. With no shingling in z, the inactive edges on the side of the sensor need to be kept at a minimal. It was recently

demonstrated that in an n-in-n technology, with guard rings on the opposite side from the pixel collecting implant, one can shift the guard rings under the active area, with a slight loss of homogeneity at the edges, which is recovered after heavy irradiation due to the fact that charge collection comes then mainly from just under the pixel implants [10]. In the planar case, one sensor tile corresponds to one module.

3D silicon sensors present advantages with respect to planar sensor that come from having fast charge collection, needing lower high voltage after high irradiation, and being generally more rad-hard. The main challenges facing this technology is the higher capacitance and the loss of efficiency at normal incidence associated to the collecting pillar, as well as manufacturability concerns (limited number of vendor available, difficulty to reach high yield, higher costs). Also for this technology must the edges be kept at a minimum size, and this was shown to be possible with the use of so-called ohmic fences, with finally dead area that could be kept below the 200 μm level as well [11]. In the 3D silicon case, two sensor tiles correspond to one module. With an installation date foreseen for the summer 2013, sensor production needs to be already on-going in fall 2011 in order to meet the schedule. Therefore the production of enough planar sensors to fully cover the IBL has been launched, and in addition a parallel production of enough 3D sensors to cover up to 50% of the IBL (depending on yield). Depending on manufacturing results, up to 25% of the IBL may be covered with 3D sensors. The 3D sensors would then be placed in the high η regions where these sensors are thought to be advantageous for inclined track detection. This possible dual technology IBL is made possible by the fact that most of the other components of the IBL are designed independent from the choice of a specific sensor.

One should mention here that R&D is on-going on other themes related to the IBL module, e.g. development of a module flex, passive components needed, high yield bump-bonding and wire-bonding. To minimize the material introduced by the IBL, a thinning down method for the large FE-I4 has been put in place with ATLAS pixel main bump-bonding partner (Fraunhofer IZM institute Berlin[2]). The challenge is to reliably take care of the handling of a thinned-down FE / sensor assembly during the relatively high temperature bump-bonding process, and the potentially mechanically stressing wire-bonding. For bump-bonding, attachment to a temporary glass handle wafer is done using a polyimide glue, with subsequent handle wafer laser removal. Methods for safe wire-bonding of thinned down assemblies are currently being developed in Bonn. A target thickness between 100 μm and 150 μm seems manageable.

## 5. Outlook: Towards a Production IC for the IBL

The development of an FE-I4B tuned for the needs of the IBL is one of the main focuses of the IBL project for the summer / end of 2011. The changes which need to be brought to the FE-I4A can fit in three categories. First, a few FE-I4A structures were implemented for test or comparison purposes: for example, the pixel array had a few flavors of double-columns, with variations on the implementation of the pre-amp feed-back capacitance, of the discriminator, of

[2] IZM Berlin: http://www.izm.fraunhofer.de/

the in-pixel memories. The FE-I4B array will now be made uniform with a single pixel flavor. Second, few fixes need to be brought to the FE. A few DAC ranges need to be extended or better centered. The effect of leakage current on the pulse generator (calibration pulse injection to the pixel) needs to be addressed. The fix there will be also at pixel level by the choice of switches using low power transistors which should exhibit less sub-threshold leakage current. The Shift Register read back needs to be done in a more reliable way and the skipped trigger counter needs to be properly implemented (both requiring tuning of EoCHL logic), etc. Third, new functions will be added: addition of a global ADC and a temperature sensing circuit, placement of an analog MUX. New functionalities are required by the pixel DAQ (make Bunch-Crossing ID counter 13 bits and Level 1 Trigger ID counter 12 bits, implement user defined event size limiter for optional long event truncation, tune data format). Finally, the powering scheme must be tuned to the final IBL powering implementation, using the Shunt-LDO.

Despite the accelerated schedule that was brought by the decision of going for a "fast track" IBL to fit the updated LHC machine shutdown scenario, and based on the very encouraging results brought by the sensor R&D groups and the successful submission of an FE-I4A, the IBL community is confident that the IBL project will be brought to an on-time completion to be inserted in 2013.

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