PICMG xTCA Standards Extensions for Physics: New Developments and Future Plans

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Abstract– After several years of planning and workshop meetings, a decision was reached in late 2008 to organize PICMG xTCA for Physics Technical Subcommittees to extend the ATCA and MTCA telecom standards for enhanced system performance, availability and interoperability for physics controls and applications hardware and software. Since formation in May-June 2009, the Hardware Technical Subcommittee has developed a number of ATCA, ARTM, AMC, MTCA and RTM extensions to be completed in mid-to-late 2010. The Software Technical Subcommittee is developing guidelines to promote interoperability of modules designed by industry and laboratories, in particular focusing on middleware and generic application interfaces such as Standard Process Model, Standard Device Model and Standard Hardware API. The paper describes the prototype design work completed by the lab-industry partners to date, the timeline for hardware releases to PICMG for approval, and the status of the software guidelines roadmap. The paper also briefly summarizes the program of the 4th xTCA for Physics Workshop immediately preceding the RT2010 Conference.

Acronyms- PICMG - PCI Industrial Computer Manufacturers Group, a consortium of over 250 companies dedicated to the development and maintenance of PICMG open-source specifications including PCI and ATCA platforms; ATCA - Advanced Telecommunications Computing Architecture, the first architecture designed for high availability of 5-nines (0.99999); ARTM - ATCA Rear Transition Module; AMC - Advanced Mezzanine Card, which can reside on an ATCA Carrier board or in a separate MTCA shelf; MTCA - MicroTCA, specifically the chassis or shelf that supports AMC cards in the same manner as an ATCA carrier; μRTM - Micro Rear Transition Module, a feature allowed but not specified nor implemented in current industrial designs; xTCA – the generic ATCA –and TCA family of specifications.

I. Introduction: The Managed Platform

The case for developing ATCA[1] and MicroTCA (xTCA) specification extensions for physics has been covered in several previous papers[2]. Briefly, ATCA and MicroTCA is the first all-serial communication platform available to the physics community to support both massively complex accelerator controls and massively large, high bandwidth and throughput experimental data acquisition systems. The major strength of xTCA is its multi-layer highly scalable *managed platform architecture* designed to achieve the highest possible *system availability*. Physics research imaging technologies have driven industrial applications in a wide range of medical scanners, for example, and in turn continue to evolve to exponentially higher speeds and resolution through new computer, communications industry and analog-to-digital conversion chip developments. The high availability managed platform is an important new tool for the instrumentation and control systems of these most complex scientific machines and instruments ever invented.

Adaptation of the x TCA platforms to physics was undertaken by a collaboration starting in May-June 2009 with the PICMG open specifications industry consortium. The remainder of this paper discusses the results of lab-industry committee work as well as important concomitant prototype developments among participating laboratories and industries.

II. New Features Required for Physics Hardware

To achieve high availability in a complex physics system requires three main features common to xTCA:

1. Modular architecture
2. N+1 or N +M redundancy of single-point-of-failure modules whose malfunction could stop operation of the machine or detector
3. Intelligent platform management for quick isolation of faults and hot-swap

In addition, physics modules need a few extended features not covered by current xTCA specifications:

4. Rear transition modules (RTMs) with standardized interconnects and management features
5. Extended real estate on AMC cards for high performance analog conversion, signal conditioning and calibration circuitry
6. Extended options for backplane distribution of high precision timing, triggering and machine synchronization of modules and groups of modules

The goal is to accomplish the latter features with backward compatibility to existing industry AMC designs of processors, analog modules or carrier cards that use the existing standard backplane interconnect.

III. Summary of Hardware Solutions

The above list of needs and proposed solutions has been tabulated in detail in Ref. 2. The current status summary is as follows:

Work supported by U.S. Department of Energy Contract DE-AC02-76SF00515

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[1] Advanced Telecommunications Computing Architecture, specification developed by the PCI Industrial Computer Manufacturers Group, PICMG, released in June 2004.

[2] See for example IEEE Real Time 2009 Conference Proceedings, Advances in Developing Next Generation Electronics Standards for Physics, May 2009, R.S. Larsen, Beijing China.

A. AdvancedTCA RTM Interface (ARTM)

A physics standard interface has been defined consisting of the following:

1. Up the 3 of the versatile ZD 4-row by 10 channel connectors for IO
2. A newly developed power and management connector[3]
3. The interface description and mechanical keying solution have been detailed except for format of FRU data.
4. See Fig. 1.

This effort has also taken account of the work of another PICMG committee's work on the standard management interface which is under development.[4]

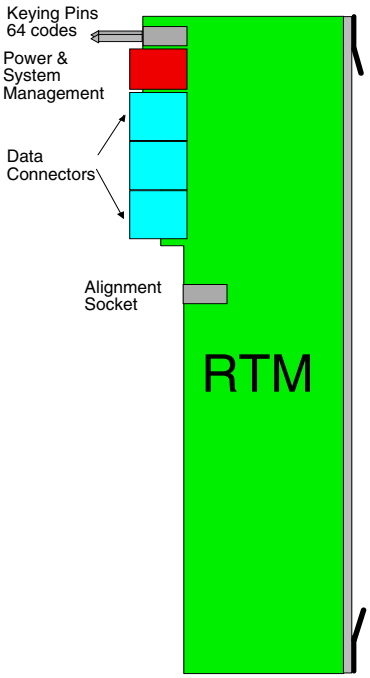

Figure 1: ARTM Mechanical Outline- R. Downing

Status:

1. All mechanical specifications are agreed by the committee.
2. Final details of the power and management connector are being resolved.
3. Prototyping by one or more industrial partners will commence shortly
4. A draft specification[5] is complete except for item 2.
5. The Committee vote followed by circulation to the entire PICMG community for approval is anticipated in summer 2010.

B. ATCA for Physics Precision Timing Distribution

A timing distribution system to use extended option lines or added special lines in the ATCA backplane for higher precision has been proposed by J. Sousa[6] and generally accepted by the committee. The goal is guideline for users in which the specific implementation for most applications with timing precision of <100 psec jitter can be accomplished within the base specification of current backplanes, at the same time pointing out the possibilities for considerably high precision with modifications to the backplane. Table 1 shows a summary of options and Table 2 the line usage for a dual-dual star backplane.

Timing over	Ports	Lines available	Performance	Compatibility
Bussed Clock Interface	CLK1, CLK2 assigned Only CLK3 may be used	6 diff pairs	Fair 100 MHz bussed	Compatible
Fabric star on hub slots	Timing hub in slot 3;4 Ports 3;4 on node cards	All nodes receive/send up to 8 distinct timing signals	Good * ~3 GHz P2P <100 ps jitter	Addition of ATCA 3.6
Base interface	Timing+Data hub in slots 1;2	All nodes receive/send 2 distinct timing signal	Good ~1 GHz? P2P	Changes to ATCA 3.0 required
Shared Fabric port	Timing+Data lines share a fabric port	All nodes receive/send up to 6 distinct timing signals	Good ~3 GHz P2P <100 ps jitter	Changes to ATCA 3.x required
Dedicated backplane lines	Update channel ports redefined for timing	Up to 10 additional, equal length, low crosstalk diff pairs	Excellent Low skew Low jitter	May not be compatible

**Can improve with equal length low crosstalk lines on backplanes*

Table 1: Summary of Options for ATCA Timing – J. Sousa

Logical Slot #		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Con	Fab Ch#											SLOT - CHANNEL					
P20	15	16-1	16-2	16-3	16-4												
P20	14	15-1	15-2	15-3	15-4												
P20	13	14-1	14-2	14-3	14-4												
P21	12	13-1	13-2	13-3	13-4												
P21	11	12-1	12-2	12-3	12-4												
P21	10	11-1	11-2	11-3	11-4												
P21	9	10-1	10-2	10-3	10-4												
P21	8	9-1	9-2	9-3	9-4												
P22	7	8-1	8-2	8-3	8-4												
P22	6	7-1	7-2	7-3	7-4												
P22	5	6-1	6-2	6-3	6-4												
P22	4	5-1	5-2	5-3	5-4	4-4	4-5	4-6	4-7	4-8	4-9	4-10	4-11	4-12	4-13	4-14	4-15
P22	3	4-1	4-2	4-3	3-3	3-4	3-5	3-6	3-7	3-8	3-9	3-10	3-11	3-12	3-13	3-14	3-15
P23	2	3-1	3-2	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15
P23	1	2-1	1-1	1-2	1-3	1-4	1-5	1-6	1-7	1-8	1-9	1-10	1-11	1-12	1-13	1-14	1-15

Table 2: Dual-Dual Star Backplane Routing – J. Sousa

Figures 2 & 3 show the de-jittering circuit proposals for both clocks and triggers using a PLL and local VCO. Triggers need reconstituting by sampling at the domain using a de-jittered clock.

[3] Prototype design developed by Positronix Inc.
[4] PICMG IRTM.0 in development.
[5] Available only to committee members until approved by PICMG general membership.

[6] J. Sousa, *An Overview of the ATCA Timing and Synchronization Resources for Control and Data Acquisition*, presented at IEEE RT2010, Lisbon, May 24, 2010

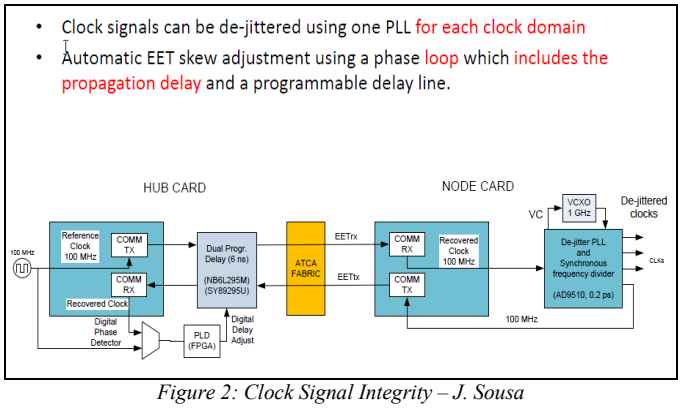

Figure 2: Clock Signal Integrity – J. Sousa

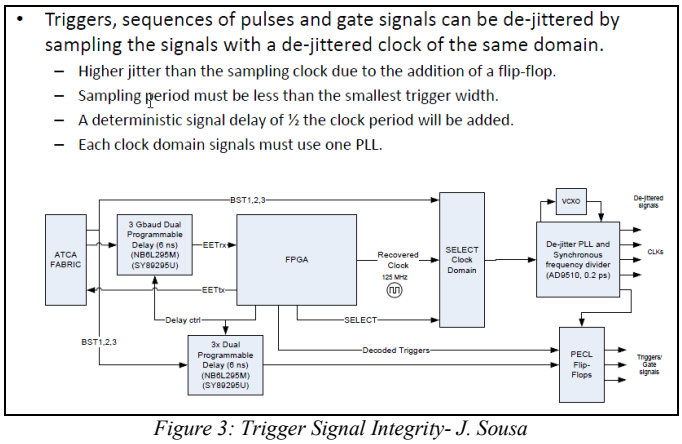

Figure 3: Trigger Signal Integrity- J. Sousa

Status:

1. The overview has been presented and discussed by the Timing and Synchronization Hardware Committee.
2. Contents of a draft of formal guideline are agreed but not yet written.
3. Lab prototyping is in progress at IPFN.
4. The goal is a final document by end of summer 2010.

C. Double Wide AMC with Standard Interface to Double Wide µRTM

Several ongoing controls projects are driving the development of standard specifications based on MicroTCA. This requires the coordinated development of a double-wide AMC, a companion µRTM card and interface, a new 12-slot MTCA shelf, and a new specification of timing and triggering lines and protocols in the backplane. The details and status are as follows:

Figure 4 shows the Double Wide AMC- µRTM concept and interface.[7]

Figure 5 shows the µRTM interface, which includes power, data and IPMI management features as an extension of the host AMC module IPMI.[8]

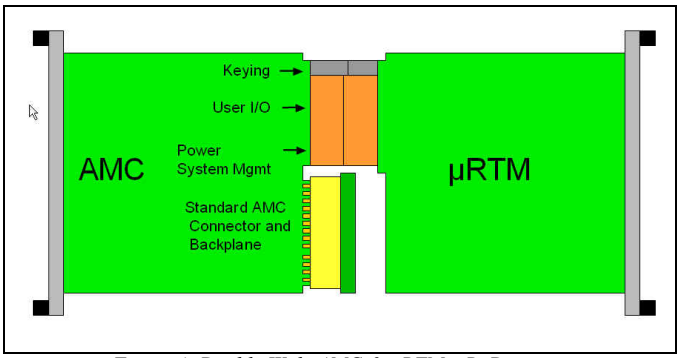

Figure 4: Double Wide AMC & µRTM – R. Downing

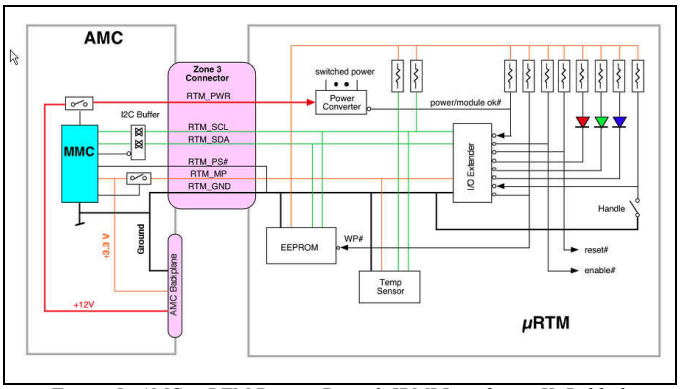

Figure 5: AMC- µRTM Power, Data & IPMI Interface – K. Rehlich

Status:

1. The double-wide mechanics is finalized to the point that shelves have been designed and prototyped by vendors.
2. Double-wide prototype modules are in progress for several applications (DESY, SLAC, Industry)
3. The mechanical-electrical specification is complete including the definitions for IO, power and IPMI for the µRTM
4. µRTM power is limited to 50 Watts and the sum of AMC plus µRTM to the presently specified 80 Watts
5. Details of µRTM communication protocols are still being worked on by the committee but appear near finalization
6. Hardware development can proceed while specifications are being formalized

D. MicroTCA Double Wide 12-Slot Shelf

The original Double Wide Shelf AMC shelf specified by PICMG did not have provision for an RTM, although the module itself allowed a user-defined connector in the RTM area (Zone 3). The needs of the Physics community led to the development of the AMC- µRTM concept developed in (C). DESY along with µTCA shelf manufacturers Schroff and ELMA developed prototype versions of a double-wide proof-of-principle unit. An enormous effort went into achieving the required high precision mechanical details.. Examples of new prototype shelves from industry are shown in Figures 6-9.

[7] Figures courtesy R.W. Downing, *PICMG Physics Hardware Working Group Report & Current Specification Review*, xTCA for Physics Working Group Tutorial Presentation, May 22, 2010, Lisbon RT 2010

[8] IPMI Interface & Timing Figures courtesy K. Rehlich, *µTCA Specification for Physics Timing Distribution & Sum Lines*, xTCA for Physics Workshop Presentation May 23, 2010, Lisbon RT 2010

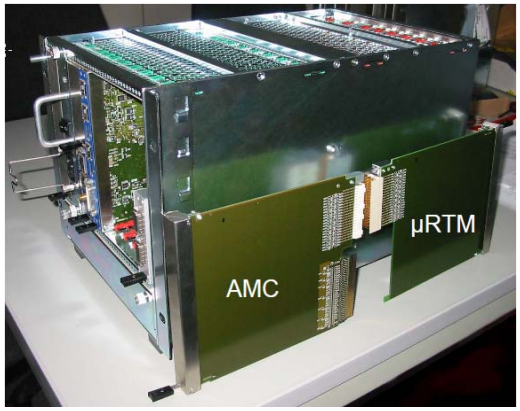

Figure 6: Six Slot Development Shelf with Prototype Cards – K. Rehlich & D. Mann, Schroff

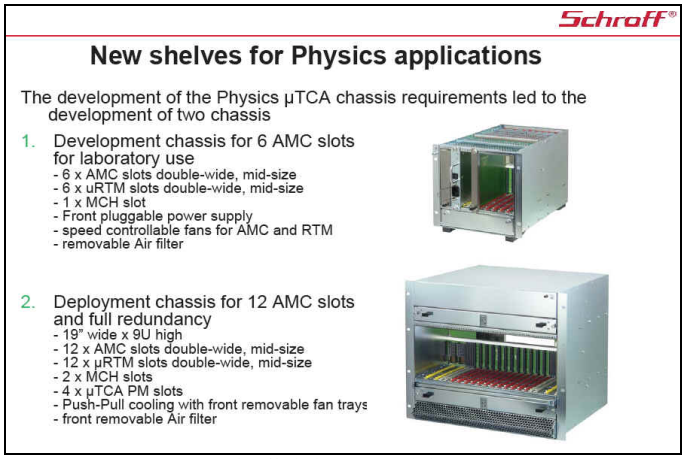

Figure 7: Schroff Shelves at Workshop – D. Mann

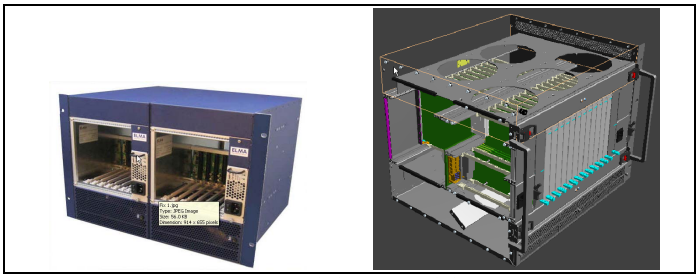

Figure 8: ELMA Shelves at Workshop – F. Fix

Status:

1. Industrial partners Schroff and Elma have collaborated on the µTCA prototype modules and have produced outstanding prototype shelves that the community can use immediately (6-slot version).
2. 12-slot versions are offered by both companies and some orders are already placed.
3. Formal committee approval of the backplane modifications is expected at the next meeting (following Section E on backplane).
4. A protocol for separate fan control of AMC and µRTM areas while staying within present IPMI cooling unit support limitations has been proposed and is expected to be resolved shortly.

E. µTCA Precision Timing & Trigger Distribution

The 12-slot µTCA shelf specified for Physics use includes the capability for distribution of precise timing and triggering thus avoiding a large and expensive external coaxial cable plant. Industry has also produced a 6-slot development shelf that will not provide redundant features but will include support of the timing features. This also requires MCH Controllers that can manage either 6 or 12 slots or both.

The timing concept in which a timing-triggering source in any slot can via the MCH address any other applications slot, is shown in Figures 9-11. Extended Options radial lines are used, managed by the MCH, to provide point-to-point links with separate buffering for good isolation between modules. This is necessary so that removing a module in a hot-swap operation does not perturb timing in adjacent modules.

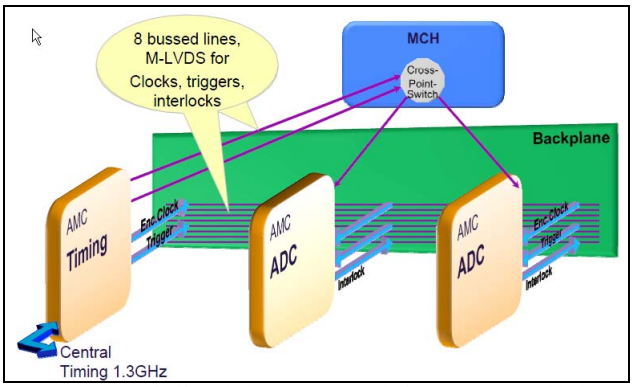

Figure 9: µTCA Shelf Backplane Timing Radial & Buses- K. Rehlich (KR)

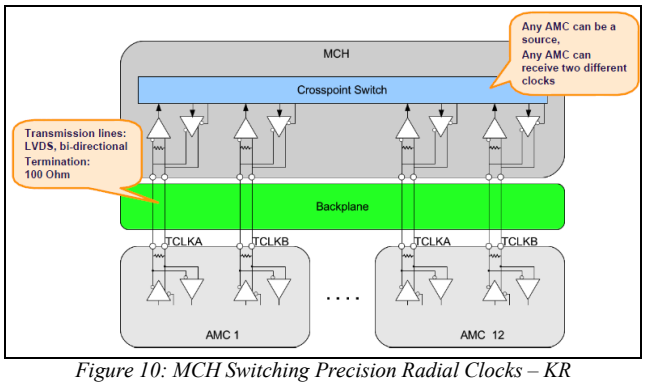

Figure 10: MCH Switching Precision Radial Clocks – KR

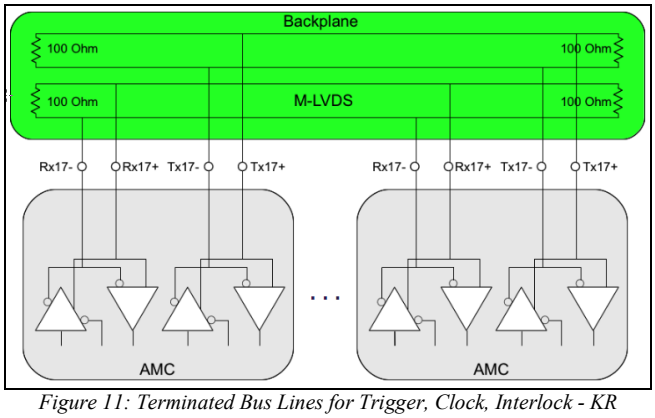

Figure 11: Terminated Bus Lines for Trigger, Clock, Interlock - KR

Additional lines are added on a new backplane layer for the non-precise bus lines as well as special summing and daisy-chain lines for vector summing involving several modules and slow interlocks involving several modules. This is judged to have enough flexibility to cover the most common physics applications while avoiding a large unwieldy external cable plant. The backplane concept incorporating these features is shown in Figure 12.

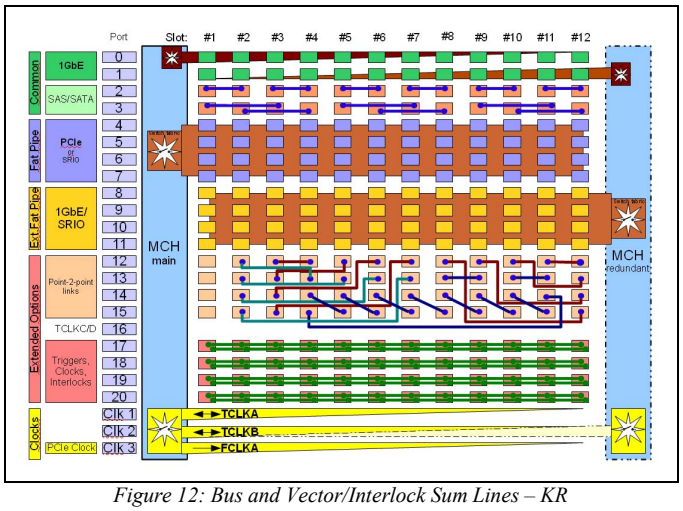

Figure 12: Bus and Vector/Interlock Sum Lines – KR

Status:

1. A comprehensive solution to specification extensions for clocks and trigger distribution on the backplane with minimal changes has been agreed by the committee.
2. The above description has been worked out closely with industry partners and backplane changes confined to a single new layer appear straightforward.
3. Pending final review, the description of timing architecture needs to be added into the draft specification.
4. MCH manufacturers are apprised of the requirements and at least one is preparing modifications to existing products to meet them.

IV. SUMMARY OF SOFTWARE GUIDELINES DEVELOPMENT

The purpose of the Software Technical Subcommittee is to develop guidelines, not specifications. The entire xTCA enterprise is geared toward two key elements:

1. *Interoperability:*

   xTCA modular components claiming to meet PICMG specifications must pass an interoperability test. This is primarily a test to assure that IPMI has been implemented properly and is clean of hidden errors that can cause serious malfunctions in a customer's management system, which itself may be implemented with IPMI from a new design or purchased from a third party vendor.
2. *High availability:*

   The management features of IPMI support high availability through hot-swap of the hardware, but high availability features must be built into software at the same time or all may be for naught. The design of HA software is a strong emphasis of SAF, the Software Availability Forum, which is independent of PICMG and dedicated to advancing standards such as the Hardware Platform Interface (HPI.1) designed to make HA easier to implement in a standard way. The labs are not currently members but have an open invitation to join.

The mechanism for assuring hardware-software interoperability is the PICMG Interoperability Workshop or "Plug Fest" in which a company hosts a group that provides the test hardware, software and PICMG member experts to help test new products. Without submitting to such tests manufacturers cannot claim to be PICMG – compliant. These festivals occur about twice a year.[9]

A. *Software Technical Subcommittee Roadmap*

The Software working group is much smaller than hardware and its members have been heavily loaded so progress has been slow. However the plan is ambitious and as the hardware work diminishes some members will be able to concentrate more on these tasks. The general areas of interest are as follows:[10]

1. Routing and Protocols
   a. Data protocols: Low, medium and high latency; standardized connection, traffic management
   b. Timing & Synchronization Protocols: Clocks, triggers, interlocks, use existing channels as possible; standardized connection, configuration
   c. Command/ Control: Application oriented; Primary via xTCA Base interface (1 GbE); Software support: Standard channel-agnostic protocol
2. System/Rack/Module Management
   a. Remote management functions: identification; health monitoring; redundancy failover management; firmware/software updates
   b. IPMI/HPI standard management from PICMG and SAF: Adapting IPMI/HPI to physics environment; analog signal formats and E-keying
   c. System Management: Common database for infrastructure in physics environments (cable plant, actuators, sensors etc.)
3. Operating Systems & Infrastructure
   a. Virtual Machine environment for software development: Operating independence, insulation from hardware details at application level; standardized components (process thread management via POSIX, EPICS; hierarchical IO communications,

[9] The next Workshop is scheduled at the Schroff Training Center in Straubenhardt, Germany, week of October 18, 2010, open to all PICMG members.

[10] Summary from W. Koprek, *PICMG Software extensions for Physics, Roadmap and Status*, xTCA for Physics Workshop, May 23, 2010, RT2010, Lisbon

timing device API); support local, virtual device in same framework; hardware management API for custom board development.

4. Processing and Operation Libraries
    a. Commonly used device specific APIs -- ADC/DAC/Timing/Power/Actuator/Sensor
    b. Device specific APIs --hardware registers
    c. Standard function libraries --Software, FPGA
    d. Reference designs, templates --Software, FPGA

B. *Working Group Tasks & Status*

1. Data Transport Protocol
    a. Initial protocol selected, under evaluation
2. Synchronization Protocol
    a. Pending final hardware distribution scheme
3. Command Control Protocol
    a. Proposal in development
4. Component Management/failover/update
    a. Proposal in development
5. Common Hardware API
    a. Technical proposal accepted in principle; guideline working
6. Common Process/Thread Model
    a. Technical proposal accepted in principle; guideline working
7. Common IO Device Model
    a. Technical proposal accepted in principle; guideline working
8. Common Communication Model
    a. Combined with (7)

Status:

1. The Software Technical Committee has made good progress despite very limited manpower availability.[11]
2. Task groups are defined and the drafts of the first guidelines are ready for review by a wider group.
3. More input is needed from lab software experts working in both controls and data acquisition fields, for both ATCA and MicroTCA.

V. REPORT ON 4TH XTCA FOR PHYSICS WORKSHOP

At the 3rd workshop in Beijing in June 2009 the formation of the xTCA for Physics Committees was announced, and at the 4th meeting in Lisbon the Committees reported major progress, especially toward completing the Hardware goals for Timing, Synchronization and I/O. This 4th meeting was designed to stress some of the issues of getting started with xTCA design, particularly the IPMI features necessary to achieving any of the advertised high availability benefits of a system. It also preserved the previous themes of invited industry speakers and invited demonstrations of hardware and software tutorials. Table 3 is an ordered summary of presentations by type.

No.	Title	Speaker	Type
1-1.1	xTCA HW Potential for Physics Apps	R. Larsen	Stds HW
1-1.2	HW Platform Management Design	P. Hawkins	Stds IPMI
1-1.3	Building High Availability Systems	Q. Yang	Stds SW
1-1.4	HW-SW Best Practices	H. Bruning	App SYS
1-2.1	HW PICMG Working Group Progress	R. Downing	Stds HW
1-2.2	SW PICMG Working Group Progress	W. Koprek	Stds SW
1-2.3	µTCA New Shelf-AMC-µRTM HW	D. Mann	Stds HW
1-3.1	ATCA Global System Mgr Demo	J. Bruning	Sys IPMI
2-1.1	ATCA System Std Timing-Triggering	J. Sousa	Stds HW
2-1.2	µTCA System Std Timing-Triggering	K. Rehlich	Stds HW
2-1.3	µTCA Timing-Triggering Module	A. Hidvégi	App HW
2-2.1	ATCA Fusion Plasma Control	B. Gonçalves	App CTL
2-1.2	ATCA Fast Control & Timing ITER	P. Makijarvi	App CTL
2-2.3	IPMI Development DESY LLRF	D. Makowski	App IPMI
2-2.4	ATCA Lessons Learned DAQ-IPMI	M. Huffer	App DAQ
2-3.1	µTCA New Shelf-AMC-µRTM HW	F. Fix	Stds HW
2-3.2	µTCA Application Ready Systems	P. Hawkins	App SYS
2-4.1	xTCA Architectures for Controls	T. Jezynski	App CTL
2-4.2	µTCA Versatile FPGA AMC for Ctl	P. Vetrov	App CTL

Table 3: Summary of Workshop Program Presentations (not including discussion sessions)

All presentation slides will be posted to IPFN and CERN websites and will also be included in the conference record DVD.[12]

Among the highlights of the conference were:

1. Presentation of new shelf and module hardware built to the µTCA physics standards by both Schroff and ELMA
2. Presentation of excellent tutorial materials by lab and industry members of the committee including hardware, software, IPMI and timing for both ATCA and µTCA
3. An excellent airing of IPMI challenges and solutions from four different speaker perspectives
4. Presentation of a new timing module prototype designed to the µTCA precise timing and trigger specification
5. Real physics hardware and software prototypes for fast Plasma control and for a massively parallel data acquisition generic module for high energy and astrophysics applications.
6. Reports on the broad range of initiatives underway for the DESY XFEL project.

VI. SUMMARY CONCLUSIONS

The PICMG xTCA Committees for Physics have made excellent progress in the year that they have been operational. Particularly the Hardware Working Group, formally known as the Timing, Synchronization and I/O Technical Subcommittee, is closing in on achieving all the goals on its current Statement of Work. The Software Working group also has a good roadmap and in the coming year should execute all

[11] Leadership credit for developing the roadmap and much of the progress to date is due to Augustus (Gus) Lowell of TripleRing Technologies, Fremont CA, who also serves as Secretary of the Technical Committee.

[12] See ATCA tab at: http://portal.ipfn.ist.utl.pt/rt2010/

of the tasks to first order at least. Software however can be predicted to take longer to master and to make real gains in demonstrating higher levels of robustness and interoperability.

When the current roadmap specifications and guidelines are complete the present working groups will formally disband, although the Physics Coordinating Committee will continue to make sure that maintenance as well as new needs is addressed. This will happen naturally through continuing laboratory membership in PICMG.

The Committees also have requested feedback on future meetings or special workshops that will address issues people face in implementing the standards in their own laboratories. This could include tutorial sessions of short duration as well as longer workshops at the request of a specific lab. Much like the recent workshop, small workshops can be arranged on location rather than having a much larger number traveling across country or internationally.

Hopefully additional labs will join so more hardware and software engineers and physicists will become active in serving the physics community in this important ongoing enterprise. To make any standard a success, the labs have to make a commitment for the future. Hopefully the success of this venture will continue to prove its value to the community at large.

VII. ACKNOWLEDGMENTS

For this 4th Workshop we gratefully acknowledge the outstanding support of the following: Workshop Co-Chair Dr. Bruno Soares Gonçalves and Dr. Maria Fernanda Pinto and her capable staff at IPFN Lisbon; all of the speakers listed in Table 3 who gave their valuable expertise most generously; and all the contributing members the two very hard-working committees who meet every week, headed by Robert Downing of SLAC/R.W. Downing Inc., who also proofed the manuscript; and Dr. Stefan Simrock of ITER. We especially acknowledge the extremely generous contributions of our PICMG industry members to the physics community by their support of this effort; these world-class experts have been unstinting in helping our mutual collaboration. We are deeply indebted to all of them.