ANALYSIS OF THE ULTRA-FAST SWITCHING DYNAMICS IN A HYBRID MOSFET/DRIVER*

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Abstract

The turn-on dynamics of a power MOSFET during ultra-fast, ~ ns, switching are discussed in this paper. The testing was performed using a custom hybrid MOSFET/Driver module, which was fabricated by directly assembling die-form components, power MOSFET and drivers, on a printed circuit board. By using die-form components, the hybrid approach substantially reduces parasitic inductance, which facilitates ultra-fast switching. The measured turn on time of the hybrid module with a resistive load is 1.2 ns with an applied voltage of 1000 V and drain current of 33 A. Detailed analysis of the switching waveforms reveals that switching behavior must be interpreted differently in the ultra-fast regime. For example, the gate threshold voltage to turn on the device is observed to increase as the switching time decreases. Further analysis and simulation of MOSFET switching behavior shows that the minimum turn on time scales with the product of the drain-source on resistance and drain-source capacitance, $R_{DS(on)}C_{OSS}$. This information will be useful in power MOSFET selection and gate driver design for ultra-fast switching applications.

I. INTRODUCTION

The flip chip assembly technique has been used to directly mount die-form devices on a printed circuit board. This method is capable of significantly reducing the parasitic elements; especially inductance in the package, bonding wire and PCB traces, and is widely used in high speed digital circuit assembly. This technique has been applied to a power MOSFET/driver circuit to develop a Hybrid Switch Module (HSM) [1]. The HSM not only reduces the MOSFET switching time, but also improves the accuracy of the gate voltage measurement. This makes the HSM an ideal platform for investigating the fast switching dynamics of power MOSFETs.

Experiments using the HSM reveal clear differences in MOSFET ultra-fast switching states as compared with low speed operation. In this paper, the experimental findings are presented with analysis and simulation.

II. HYBRID MOSFET/DRIVER SWITCH

The power MOSFET is intrinsically capable of switching in about 1 ns [2]. However, parasitic inductance in the commercial packages of both the power MOSFET and its driver prevent the MOSFET from achieving this switching speed. A die form power MOSFET and driver are assembled on a PCB using the low inductance flip-chip method in the HSM to minimize parasitic inductance.

The HSMs incorporate four function blocks; energy storage capacitor, power MOSFET, totem pole driver and input buffer as shown in Figure 1. To minimize the impedance of the gate drive circuit, a pair of totem pole drivers (and associated input buffers) are used, as can be seen in the photograph of the HSM shown in Figure 2.

The energy storage is formed from a low inductance array of 1 kV, 1812 SMD ceramic capacitors in parallel (five, 1 nF, C0G and two, 47 nF, X7R), for a total capacitance of 0.1 µF. The power MOSFET, M0, is an APT1201R2 (1200V, 1.2 Ω). The die is prepped for flip chip assembly by depositing solder bumpers on the source, gate, and drain pads. The source and gate terminals are attached to corresponding pads on the PCB using conductive epoxy. The drain (back side of the die) is connected to a copper foil, which is soldered to the PCB, using sliver paste. The totem pole drivers incorporate a 100V P/N MOSFET pair (IRFC120/9120).

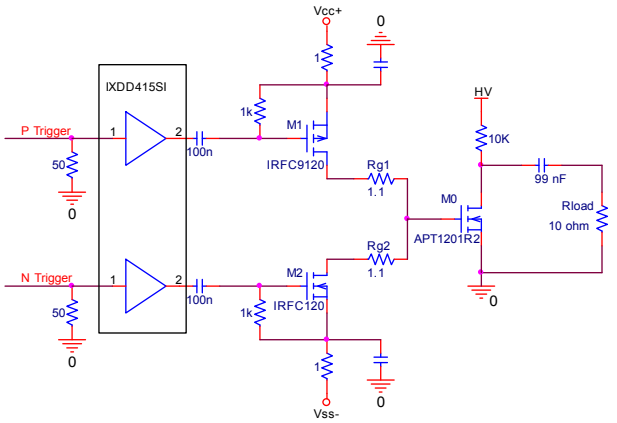

Figure 1. Schematic diagram of a Hybrid Switching Module (HSM

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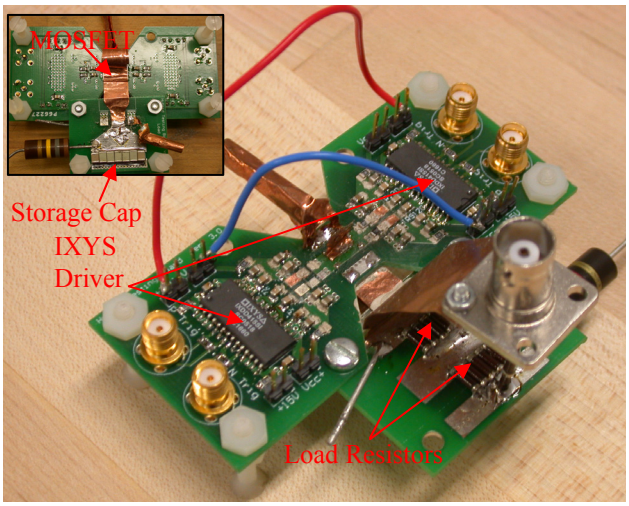

Figure 2. A photo of an HSM. Inset: bottom view of the board (MOSFET is under the copper foil).

These bare die MOSFETs are installed using the same flip-chip assembly technique. The input buffers, IXDD415SI, translate the TTL level trigger signals to high voltage to effectively drive the totem pole gates. The input buffers are capacitively coupled to the totem pole gates, as the drivers are referenced to Vcc+ and Vss- up to ±100 V.

III. TEST RESULT AND ANALYSIS

Figure 3 shows typical switching waveforms for the HSM. Because of the low inductance construction of the HSM, the oscillatory behavior that is normally seen at the gate terminal of MOSFETs during fast switching (a product of package inductance and gate capacitance) is eliminated. The ability to cleanly measure the gate voltage (V_{GS}) is very beneficial for the investigation of power MOSFET switching dynamics.

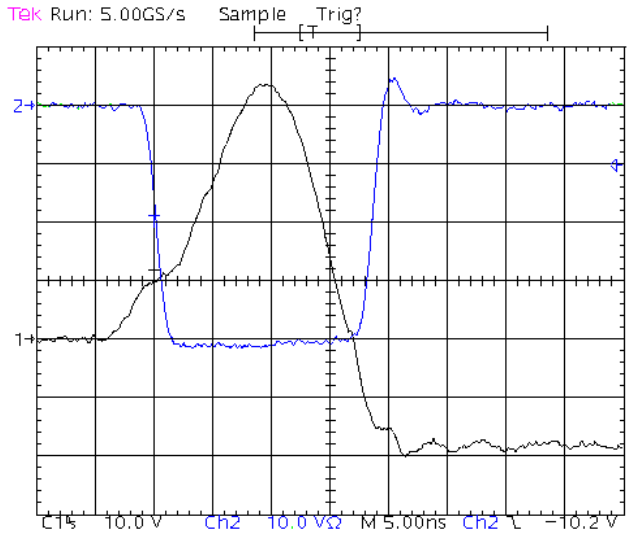

Figure 3. Typical HSM waveforms during fast switching, t(90-10) = 2 ns (Charge voltage: 1000 V, Load resistance: 10.6 Ω). CH1: Gate voltage, CH2: Output (load) voltage (attenuation ratio: 17.1:1).

A. MOSFET effective gate threshold shift during ultra-fast switching

An apparent increase in the gate threshold voltage to switch the MOSFET ($V_{GS(th)}$), is observed as the (turn-on) switching time decreases. The totem pole gate driver is a current source (|Vcc+| and |Vss-| >> V_{GS}), increasing the driver current decreases the MOSFET switching time. The driver current is controlled by varying the resistance of the series gate resistor (Rg). When the MOSFET transfer curves (I_D verses V_{GS}) are plotted for a range of Rg, Figure 4, a significant increase in $V_{GS(th)}$ is seen for small values of Rg (fast switching). During slow switching, 25 ns, $V_{GS(th)}$ is about 5 V, which rises to about 8.5 V when the MOSFET is switched in 1.5 ns. The change of $V_{GS(th)}$ is roughly proportional to the inverse of switching time as shown in Figure 5.

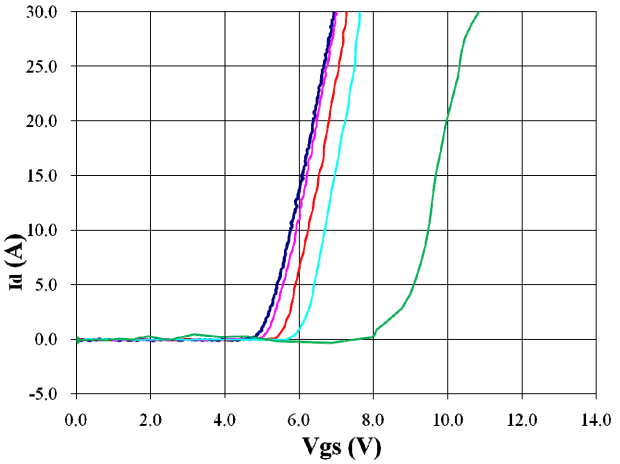

Figure 4. MOSFET transfer curve (I_D vs V_{GS}) at different values of gate resistance (switching speed): 75Ω (25 ns), 43Ω (15 ns), 20Ω (7.3 ns), 10Ω (4.1 ns), 0Ω (1.46 ns). (Charge voltage: 1000V, Rload: 27 Ω)

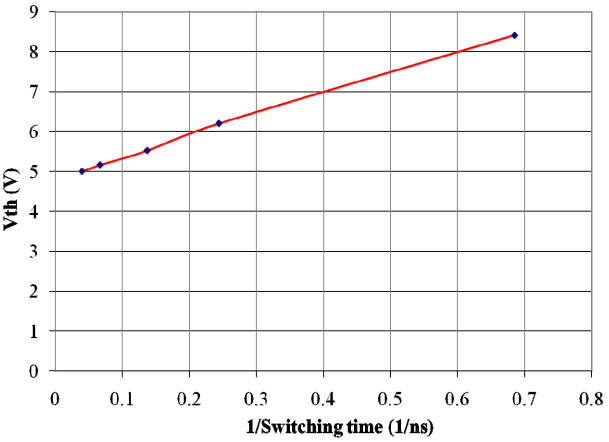

Figure 5. Gate threshold voltage verses inverse of switching time.

The observed shift in the gate threshold voltage can be attributed to the discharge current of the intrinsic MOSFET drain-source (output) capacitance (C_{OSS}). The drain current plotted in Figure 4 is the external current that flows through the drain terminal. However, during switching, the current flowing through the MOSFET channel also includes the internal discharge/charge current of the C_{OSS}. The amount of charge that must be removed from this capacitance during switching is almost independent of switching time. Therefore, as the switching time decreases, this internal current increases.

The charge required to discharge the MOSFET output capacitance is estimated by integrating the C_{OSS} versus V_{DS} curves from the manufacturer's datasheet; this value is 0.24 µC for the HSM. It is important to note that the externally measured V_{DS} includes the resistive drop across the substrate, $I_D R_{DS(on)}$, which is ~100 V at 33 A. However, the internal voltage across the junction goes to zero as the carrier distribution reaches equilibrium, and so the capacitance curves must be integrated to ~0 V to evaluate the switching charge. If the switching speed is moderate, 24 ns, the internal current that is added to the load current (~33 A) is ~10 A. However, for ultra-fast switching, 1.2 ns, the internal current is ~200 A. Hence, the total channel current (internal plus external load) must increase by more than 5 times, which requires a larger V_{GS}.

A SPICE simulation of ultra-fast (0.8 ns) MOSFET turn on using the manufacturer's device model, Figure 6, shows this effect. Here I_D is the external current flow into drain terminal, $I_{D\text{-}S}$ is current through the drain-source diode (the major source of internal drain-source capacitance), I_{CH} is the total current through the MOSFET channel ($I_D + I_{D\text{-}S}$), and V_{DS} is the drain-source voltage. It is clear that during switching, the total channel current (cyan curve) is much larger than the measured current at the external drain terminal (blue curve), due to this large internal current (magenta curve).

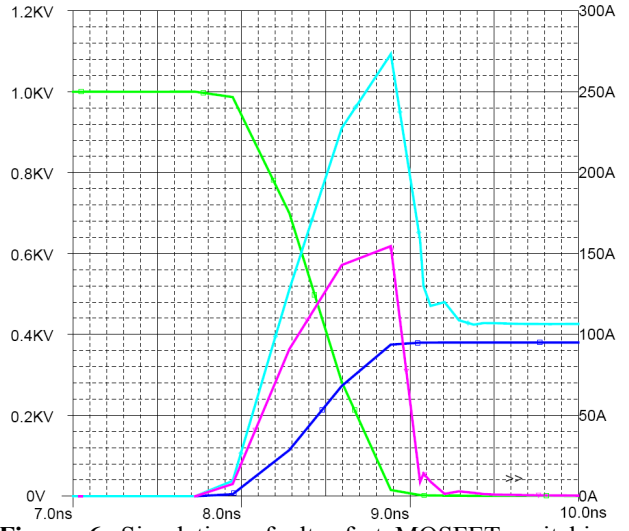

Figure 6. Simulation of ultra-fast MOSFET switching, drain-source voltage (V_{DS}), external drain current (I_D), drain-source diode current ($I_{D\text{-}S}$) and total channel current (I_{CH}). (Charge voltage: 1000V, Rload : 10 Ω)

In addition to causing this apparent $V_{GS(th)}$ shift, discharge of the output capacitance sets a minimum turn on time for the device. Although this is a voltage dependent capacitance, the effective capacitance ($\Delta Q/\Delta V$) is approximately proportional to the C_{OSS} given on the datasheet. The rate at which this charge can be removed is proportional to the channel resistance. Although this is dependent on gate voltage and channel current, it will scale with the stated $R_{DS(on)}$. Therefore, the intrinsic minimum turn on time for a device will scale as the product $R_{DS(on)}C_{OSS}$.

B. Gate charge and MOSFET turn on

Figure 7 shows the gate and drain voltage verses the injected gate charge for the HSM with an initial charge of 1000 V and a 27 Ω load. To minimize the $V_{GS(th)}$ shift discussed in previous section, a value of 43 Ω is used for Rg1. Initially, the gate voltage is independent of the HSM charge voltage. However, once threshold is reached and the slope of gate voltage plot flattens into the Miller plateau, the four plots diverge. Higher voltage charge of the HSM results in a larger I_D, which requires a higher V_{GS}. After the Miller charge has been injected, all four plots follow the same slope but they are offset by the difference in the Miller charge from their initial voltages.

An interesting feature is how little gate charge is required to effectively switch the HSM when initially charged to 1000 V. Integrating the reverse transfer (Miller) capacitance (C_{RSS}), yields ~80 nC for an initial voltage of 1000 V. Of that, approximately half is after the V_{DS} drops below 50 V, or 5% of the initial charge voltage. Therefore, a relatively small amount of charge is needed to drop the drain voltage to 10% of the initial value. The remainder of the Miller charge (over 50%) has little impact on the load voltage. This information is very important for short pulse generation: it is possible to inject a small package of charge into the power MOSFET gate to effectively turn it on.

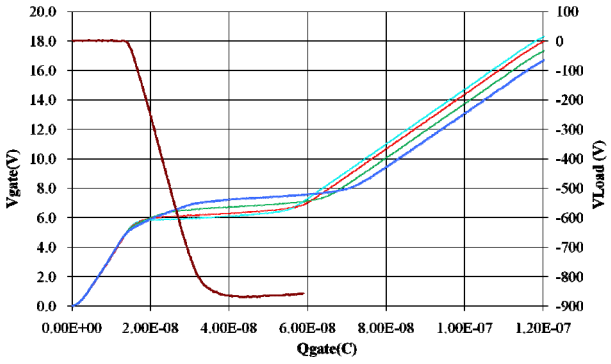

Figure 7. Gate voltage and output voltage verses gate charge at different values of the initial HSM charge voltage; gate voltage at 100V, 200V, 500V, 1000V and load voltage at 1000V charge. (Rload: 27 Ω, Rg1: 43 Ω)

IV. SUMMARY

The turn on dynamics of the power MOSFET during ultra-fast switching (t ~ 1 ns) have been investigated, using the hybrid switching module. The MOSFET switching properties vary compared to normal turn on (t ~ 10 ns or more). The threshold voltage increases during ultra-fast switching due to the added internal current required to discharge the parasitic drain-source capacitor. The Miller capacitance only needs to be partially charged to effectively switch the power MOSFET on. The minimum turn on time for any device scales with the product $R_{DS(on)}C_{OSS}$. Further analysis is needed to fully understand the behavior of the power MOSFET under ultra-fast switching.

V. ACKNOWLEDGEMENT

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VI. REFERENCES

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