SLAC-PUB-13708
June 2009

A Fusing Switch for Fault Suppression in the SNS High Voltage Converter Modulators*

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Abstract

The High Voltage Converter Modulators (HVCMs) at the Spallation Neutron Source (SNS) have operated in excess of a combined 250,000 hours. Performance and reliability improvements to the HVCM are ongoing to increase modulator availability as accelerator system demands increase. There is a relatively large amount of energy storage in the HVCMs, ~180 kJ. This energy has the potential to dump into unsuppressed faults, cause damage, and increase the time to repair. The "fusing switch" concept involves isolation of this stored energy from the location of the most common faults. This paper introduces this concept and its application to the HVCMs.

I. HVCM DESCRIPTION

There are several HVCM configurations with up to 1 MW average power, 120 kV output voltage, and 11 MW peak power. Output pulses are ~1.3 ms with a pulse repetition frequency of up to 60 Hz. There are several advantages to this topology including a relatively high efficiency, >93%, and zero-voltage switching [1]. A simplified system diagram of the HVCMs is shown in Fig. 1.

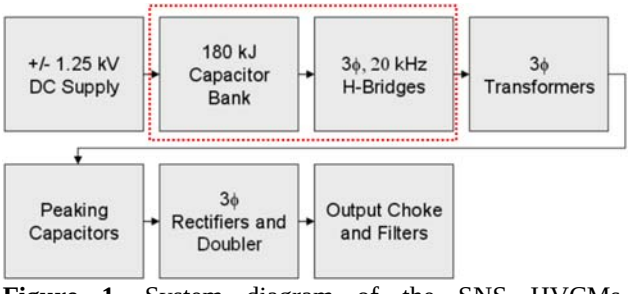

Figure 1. System diagram of the SNS HVCMs. Highlighted in red is the area of interest for the fusing switch.

An area of interest is the link between the high-energy capacitor bank and the three H-bridges. The H-bridges have been identified as a component which is particularly sensitive to failures. This has been an area of ongoing development at SLAC National Accelerator Laboratory [2, 3]. An advanced gate drive system was developed for fault suppression. In addition, higher voltage, press-pack IGBTs were incorporated into the H-bridge. Both of these additions will contribute to a lower susceptibility to faults on and after the H-bridge (ex. transformer saturation, transformer arcs, etc.).

II. FUSING SWITCH PHILOSOPHY

The fusing switch (FS) will act as an additional level of protection for the HVCMs. Figure 2 illustrates the location, highlighted in blue, of the fusing switches in the HVCM circuit. As shown, each connection from the high-energy capacitor banks to an H-bridge is now through a series switch. These switches are *not* in parallel, and therefore, current sharing schemes are unnecessary. The

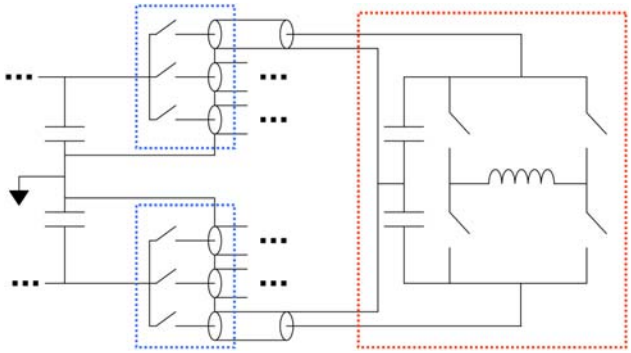

Figure 2. Simple circuit diagram of the placement of the fusing switches (highlighted in blue). Only one (highlighted ion red) of three H-bridges is shown. The capacitors at the left of the figure represent the 180 kJ capacitor banks.

* Work the Department of Energy under contract No. DE-AC05-00OR22725.
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current through a given switch is determined by the voltage on the high-energy capacitors and the effective impedance of the H-bridge. If a high-current fault occurs on one H-bridge, the current increases only through two (one on each capacitor bank) of the six total switches.

The design is such that, similar to a fuse, if a high-enough current flows through a single FS, it will open. The open switch prevents additional stored energy from flowing to the location of the fault. During normal operation, the switch remains closed. Ideally, operation with a closed FS is identical to operation with the existing capacitor bus structure. A solid-state switch, an IGBT, was chosen for the fusing component because it is not sacrificed during a fault and it offers gate control of current.

Another advantage of utilizing an IGBT is that, for a given gate-emitter voltage, there is a maximum current that will flow through the device. These are typically given in the datasheet "output characteristic" curves. Complicating interpretation of these curves are transient effects due to the Miller capacitance. A large collector-emitter dv/dt will temporarily raise the gate-emitter voltage and, therefore, conduct a higher collector current. Increased external gate capacitance can partially mitigate this effect. Nevertheless, even if the IGBT is not opened, the current during a fault can be limited to some value with an appropriate bias of the gate-emitter. Design of the gate capacitance, turn-off resistance, and voltage level are best determined empirically; experiments are currently underway at SLAC to determine the appropriate values.

In addition to self-limiting the current to an H-bridge, it is possible for sensors to be incorporated with the FS gate drives to detect the onset of a fault and signal the IGBT to open. Potential sensors include $V_{ce,sat}$, I_c, dI_c/dt, and over-temperature detection. Selection of the proper sensor complement depends on the nature of the expected faults and the associated waveforms at the location of the fusing switches.

There are many potential communication options between the fusing switches, H-bridges, and the modulator control system. Two example schemes are outlined in Fig. 3. These two schemes highlight a low and high amount of FS interaction with the HVCM control system respectively. Choice of the proper scheme to utilize will be determined by the nature of the expected faults, the ease of integration with the existing control system, and the amount of desired interaction with the control system. These issues are still being evaluated.

Scheme 1

Detection

-FS gate drive detects fault based on FS parameters (I_c,$V_{ce,sat}$, dI_c/dt, etc.); FS opens

Communication

-none

Global HVCM Fault Generation

-Through some "external" means such as low modulator output voltage, HVCM faults

Scheme 2

Detection

-FS gate drive detects fault based on IGBT parameters (I_c,$V_{ce,sat}$, dI_c/dt, etc.); FS opens

-Any HVCM fault opens the FS

Communication

-FS gate drive status signals are ORed and sent to HVCM control chassis.

-HVCM fault signals are sent to FS gate drives

Global HVCM Fault Generation

-An open FS sends a signal to fault the HVCM.

Figure 3. Two possible schemes for fusing switch fault handling.

III. MECHANICAL LAYOUT

A photograph of the existing capacitor bus plates is shown in Fig. 4. Each bank is seven capacitors in parallel. The capacitor banks connect to the H-bridges via bundles of forty parallel coaxial cables. Cable headers clamp the bundles to the capacitor buses. A major consideration when designing the FS is ensuring limited modification of existing hardware. In addition, there is limited room around these capacitor buses. Therefore, rather than constructing a new bus structure for mounting the fusing

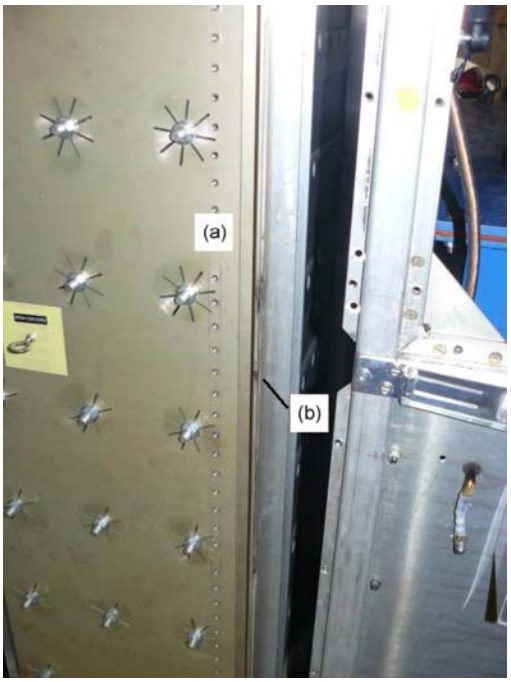

Figure 4. Photograph of an existing SNS HVCM capacitor bus. Shown is the bus for one polarity; another capacitor bank and bus structure is behind. Cable bundle headers are omitted. Highlighted are the (a) high voltage bus and the (b) ground bus.

switches, the bus structure was modified by cutting the existing bus plate.

Limited alteration of the existing bus plates places a constraint on the IGBT packages which can easily fit in the structure. Shown in Fig. 4, the high voltage leads from the capacitors periodically protrude from the bus structure. If the switch were too large, it would interfere with these connections. However, an IGBT with a 130 mm x 140 mm package was found with electrical ratings appropriate for this application. This is small enough to easily fit on the capacitor bus. A drawing of the resulting mechanical layout is shown in Fig. 5.

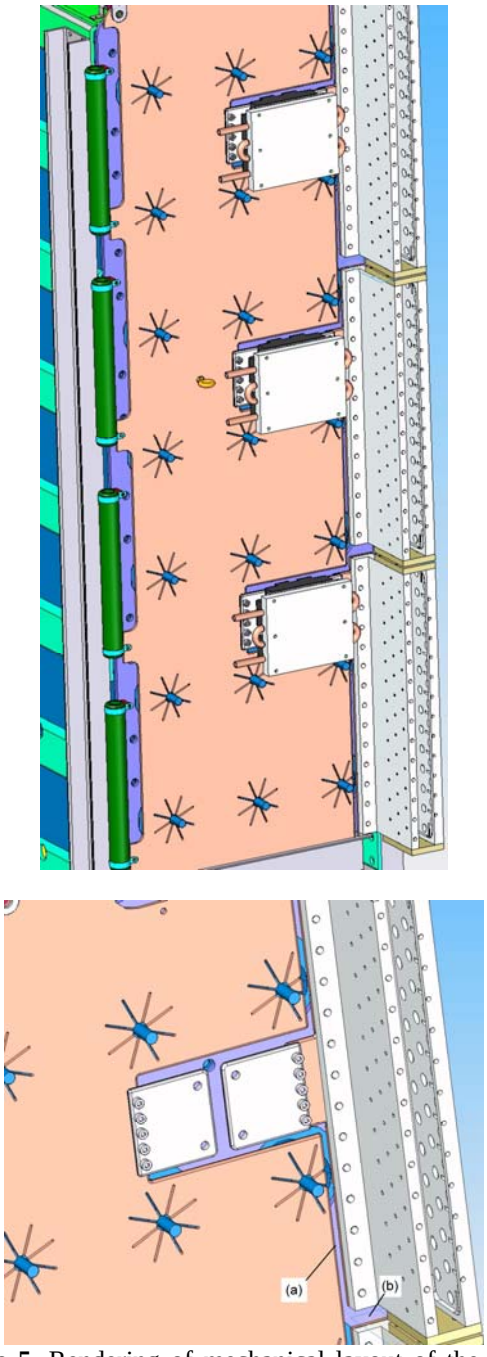

Figure 5. Rendering of mechanical layout of the fusing switch IGBTs and cold plates. Also shown are the cable bundle headers. (top) overview, (bottom) zoom-in with IGBT omitted.

There is a cut (Fig. 5, bottom, a) the vertical length of the bus which separates the capacitors from the cable bundle headers. In addition, there is a cut (Fig. 5, bottom, b) between each of the cable headers. Two small buses are made for each IGBT such that the IGBT can be removed from the modulator without removing the entire capacitor bus.

The capacitor buses were originally designed to provide a very low inductance connection from the high-energy capacitors to the H-bridges. To quantify the increase in inductance associated with the addition of the fusing switches, finite element modeling using FastHenry was performed [4]. It was found that the existing bus plates have an effective inductance of ~15 nH between the capacitor leads and the cable bundles. Addition of the fusing switches increased this value to ~25 nH. This inductance is in series with the total inductance of the cables connecting to the H-bridges which is calculated to be 70-150 nH. Therefore, the net effect of the fusing switches on increasing the total capacitor bank to H-bridge inductance is minimal.

IV. IGBT PARAMETERS

One parameter in selecting the appropriate IGBT is the peak pulse current. Figure 6 shows measured current through the existing high-energy capacitor banks with a charge of ±2.2 kV. This current is split evenly between each of the three H-bridges. Therefore, each FS would be expected to conduct ~1.5 kA during the pulse. The Eupec FZ800R33KL2C is one appropriate device. This device has a maximum collector-emitter voltage of 3.3 kV, a maximum repetitive peak collector current of 1.6 kA, a turn-off delay time of ~4 µs, and a fall time of ~350 ns.

From the transfer curves on the IGBT data sheet, with a conduction current of 1.5 kA and a gate-emitter voltage of 15 V, the collector-emitter voltage drop is ~5.5V. At

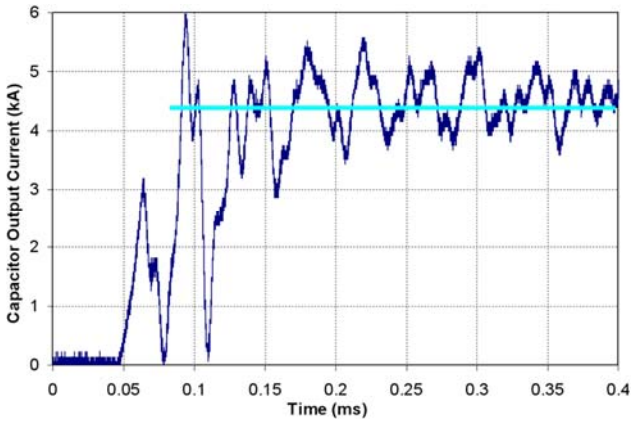

Figure 6. Measured current from the capacitor bank to the H-bridges. Shown is the start of the pulse.

full HVCM average power, the estimated conduction power losses per IGBT are (5.5 V)(1.5 kA)(60 Hz)(1.6 ms) = 800 W. The total FS power consumption per HVCM is (800 W)(6 IGBTs) = 4.8 kW. For a 1 MW average power modulator, this is 0.5% of the total power output. It is anticipated that the majority of power consumption is due to conduction losses. The only "switching" loss would occur during the beginning of the HVCM pulse when the resistance of the fusing switches is still large as the IGBT drift region is not yet populated with carriers. True characterization is best done experimentally.

A cooling water distribution system already exists on each HVCM. Because there is limited space around the capacitor buses, water cooling was chosen for heat management for the IGBTs. A commercial off the shelf, 4-pass liquid cold plate was chosen. With 800 W power dissipation per device, the junction temperature of each IGBT is calculated to be ~70 ^{o}C.

On each H-bridge, there are bypass capacitors closely coupled across the IGBTs. The energy stored in these capacitors is 170 J. The fusing switch scheme provides no prevention for this energy to dump into a fault. If current through a single fusing switch rose to 2800 A during a fault, with ±2400 V on the high energy capacitors, it would take 10 μs for ~70 J would flow into the fault. This is a relatively slow turn-off time for this IGBT. Therefore, emphasis on a fast turn-off time is likely not necessary for ensuring low energy transfer from the high energy capacitor banks during a fault.

V. SUMMARY

A preliminary design for a fusing switch in the SNS HVCMs has been completed. An appropriate IGBT was selected and the mechanical layout was sketched. The next step in the design process will be to experimentally characterize the appropriate gate drive parameters in a scaled-down test setup. Of particular interest are the effects of the Miller capacitance during an induced fault. In addition, the appropriate IGBT protection scheme (parallel MOVs, snubbers, etc.) will be determined. After a communication and fault detection scheme is chosen, the design will be complete and the options for implementation on existing HVCMs will be evaluated.

VI. REFERENCES

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