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Advances in Developing Next-Generation Electronics Standards for Physics

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***Abstract*– The Advanced Telecom Computing Architecture (ATCA) open standard developed by an industry consortium is beginning to find new applications in non-telecom fields including accelerators, HEP detectors, medical physics, astrophysics, fusion and similar applications. At the same time the broad physics community needs to modernize the capabilities of standard platforms for the future. This paper describes the formation of a lab-industry collaborative effort to extend ATCA specifications into the physics field for greater reliability and availability of next-generation machines and detectors, to improve the interoperability of instruments developed at different laboratories, and to take advantage of the potentially broad base of ATCA industry support for physics products.**

I. INTRODUCTION: NEW INDUSTRY STANDARDS

The newest modular electronics platform on the market is the Advanced Telecommunications Computing Architecture (ATCA) developed by well established industry consortium PICMG[1], released in mid-2004, the first to be developed jointly by industry from a Design for High Availability (HA) perspective. The $100B per year Telecom industry concluded that a new standard platform would on the one hand permit customers to purchase a range of interoperable components from different manufacturers to assemble systems, reducing dependence on a single large vertically integrated supplier; and on the other would enable industries to achieve the coveted "minimum time-to-market" for new technology products. Since the electronics chip technologies are famous for rapid turnover causing many products to become obsolete every few years, a successful platform has to accommodate such rapid change gracefully over at least a decade or longer, and must be open to technology improvements without major disruption to legacy installed systems, i.e. both upgradeable and scalable. Achieving a viable standard is critical to advancing the entire telecom and related consumer industries which in turn produce the chip technologies that are critical to data gathering, signal processing and data analysis and storage for physics instruments and systems.

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[1] Advanced Telecommunications Computing Architecture, specification developed by the PCI Industrial Computer Manufacturers Group, PICMG, released in June 2004.

II. GOALS FOR NEXT GENERATION PHYSICS STANDARDS

Very large long-lived accelerator and detector systems have made use of several generations of modular instrument standards starting in the 1960s though 1980s with three standards, NIM, CAMAC and FASTBUS, developed by the community and processed as open industry standards with IEEE and ANSI in the U.S. and the IEC globally. Many detector systems and some accelerator control systems were built with these standards. Meanwhile VME gained traction as an instrument standard, primarily by demand from military markets; today most newer accelerator control systems are built on VME with some instruments on VXI, a version of VME invented by instrument companies Tektronix, Hewlett Packard and others because of a desire for better shielding and additional timing and triggering features for high speed instruments. All of these later systems have similar very high pin count backplanes to accommodate parallel data transfers between data collection and processing modules with the time-multiplexed results sent upward through a single crate controller by serial link to a central control computer. In the 1980's serial links were custom-designed for physics because high speed commercial products were unavailable. System bandwidth was a function of the width of the bus which kept growing as chip speeds increased. Although current VME systems are very reliable, production physics machines such as accelerators and light sources are becoming ever more complex and demanding to keep online 24/7, so the interruption of operation by a single-point-failure of a data line in a crate backplane may become unacceptable especially for very large machines.

For large machines on the drawing boards of the scale of the International Linear Collider, total machine availability simulations have shown that the reliability of existing systems is completely inadequate, and "Design for Availability" of controls and power systems is mandatory to have any hope of achieving the target up-time.

A decade ago it was realized that the multiplexed parallel bus architecture would become obsolete as the base technologies for data communications moved ever more strongly toward high speed serial communications, even between devices within a module. The new preferred architecture became conceptually a stand-alone functional module accepting a single voltage power input, analog and digital data inputs, and a timing/trigger signal, that sends out its processed results digitally on a single high speed serial link. Such modules would easily adapt to both the sparse population of a large machine as well as the high-density clusters of a large detector. The modules could be sealed and conduction cooled,

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to handle the very high powers of emerging processor chips, and hot- swapped as a single rugged unit. This design was considered for the ILC, and the VME-VSO standards organization reportedly conceived of such a design for military customers. Around 2000-2001, PICMG started its new design, embodying many of these same principles, and with the completion of ATCA in mid 2004 announced a set of building blocks that accomplished many of the desired concepts, such as the independence of a single module from the data bus of its neighbors, hot-swappable units (which the physics community was never able to achieve in prior standards despite many attempts), and the use of a single relatively high voltage power bus to make distribution more efficient and to insulate system design from new chip technologies demanding ever-different lower voltages and higher currents. ATCA has accomplished these goals in a chassis (shelf) cluster concept that is air-cooled, N+1 redundant for all infrastructure functions (power, network and controller, hub switch and diagnostic control layer) scalable to large or small clusters down to a very small payload module, and hot-swap capable at both the large ATCA board level and a smaller Advanced Mezzanine Card (AMC) level. The suite also includes a Rear Transition Module (RTM) for IO on ATCA, and separate shelf options for the AMC card called MTCA (MicroTCA). Figure 1 shows ATCA standard shelf options; Figure 2 shows a normal card with RTM; and Figure 3 shows an ATCA Carrier card with four AMC's.

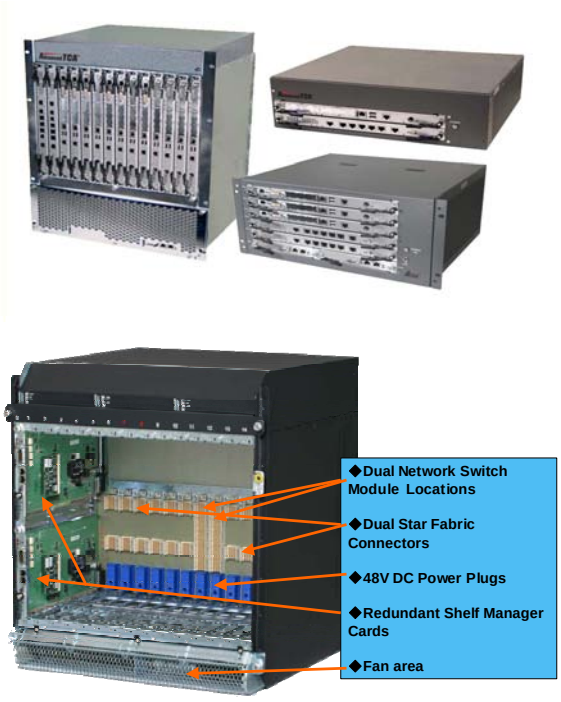

Figure 1: ATCA Basic Shelf Options (RTM standard but not shown)

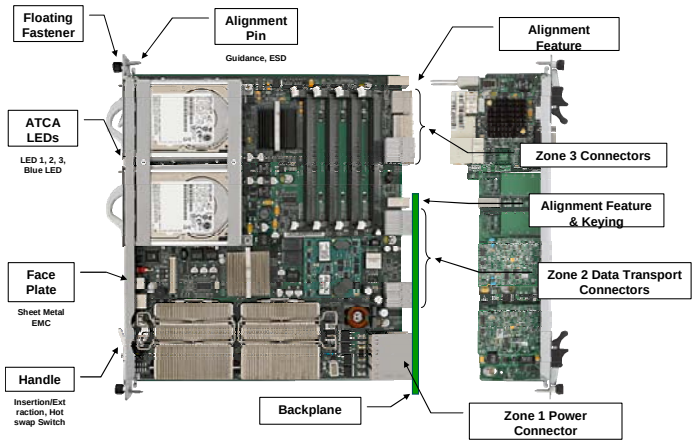

Figure 2: ATCA Module with Rear Transition (RTM) for IO (Courtesy C. Engels, Emerson)

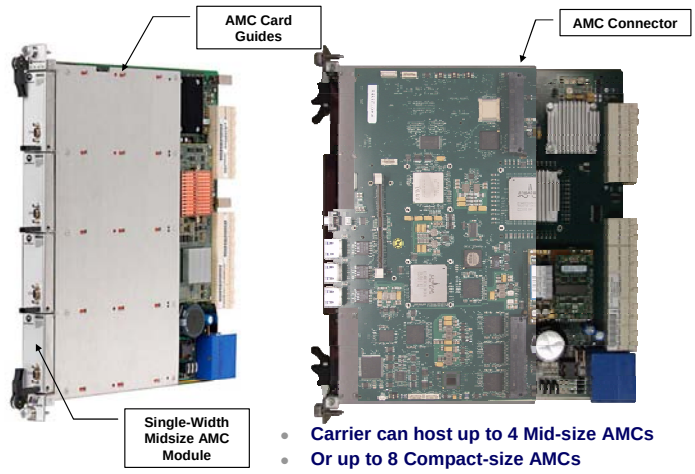

Figure3: ATCA Carrier with AMC's (Courtesy C. Engels, Emerson)

After specification of the ATCA board, shelf and AMC modules, the MTCA shelf was developed to take advantage of the small board size and predicted lower cost. The migration concept is shown in Figure 4.

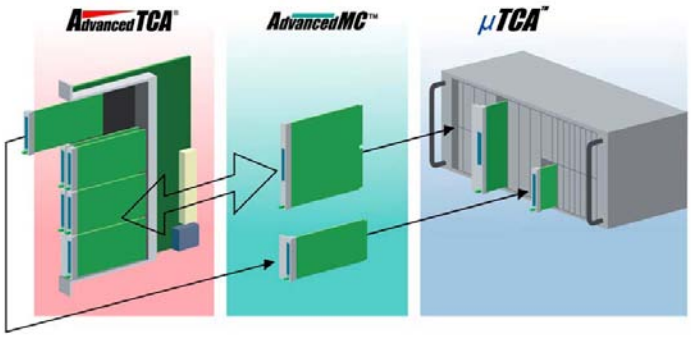

Figure4: AMC to MTCA Package Concept (Courtesy C. Engels, Emerson)

Non-Telecom users also quickly began adapting this package to industrial controls and similar uses, resulting in a variety of packages which are still emerging, these range from a fully redundant 12-payload module feature set based on a modular MTCA Carrier Hub (MCH) comprising stacked AMC boards in a single control, shelf management and switching module; all the way to non-redundant controlled blade-like packages with an embedded hub-shelf-manager mother board and only six AMC payload slots, one of which must be used for a controller. MTCA packages are still being developed with the recent release of Rugged Air Cooled MTCA[1], while conduction cooled MTCA modules and shelves still under development. Figures 5 through 7 illustrate the basic AMC and MTCA elements.

All of these features are highly desirable for next generation physics machines. However, not all physics requirements are met in the present incarnation of ATCA so desired extensions to the specifications will now be addressed.

Figure 5: Processor AMC Modules and MCH (Courtesy C. Engels, Emerson)

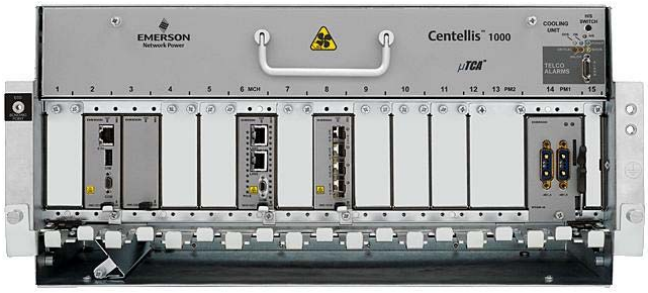

Figure 6: Fully redundant 12-AMC Payload MTCA Shelf (C. Engels, Emerson)

Figure 7: Top to Bottom: 8 AMC Payload 1U Shelf; 6 AMC Payload Non-Redundant Controller 1U Shelf; Left, Rugged Air Cooled 4-AMC Payload Shelf; Right, Conduction Cooled AMC Module (Courtesy C. Engels, Emerson)

III. PHYSICS REQUIREMENTS & SOLUTIONS FOR ATCA & MICROTCA EXTENSIONS

The computer blade-size ATCA board in its present form is well suited to new physics experiments and controls because of its very high bandwidth and throughput architecture, generous size, and RTM (Rear Transition Module) options for both expanding Input-Output (IO) connectivity and avoiding disconnecting cables when hot swapping. Several experimental physics groups have already purchased products and/or designed applications boards in order to mount experiments and learn to design future high performance systems. However further standardization for physics is needed as follows:

1. ATCA Carrier IO

The ATCA board has already proven useful when used as a carrier for AMC modules in physics controls applications[2]. In this case, however, connecting high speed low noise analog signals between ACTA carrier board and its AMC modules required a custom solution[2]. While the ATCA-RTM IO connector area (called Zone 3) is completely user-defined, the AMC itself specifies no signals for IO use. The first idea considered was to specify some unused pins on the AMC 170 pin edge-card connector for analog use, but this was unacceptable because (1) the COTS AMC ADC board being used would have to be completely redesigned for rear IO, and (2) performance would suffer with analog signals colliding

[2] This example courtesy S. Simrock et al, DESY XFEL prototype LLRF fast feedback system under development.

with the fast digital processing and gigabit serial interface areas of the board. The alternative choice adopted was to add a second connector and board stacked atop the AMC board in a sandwich arrangement, creating an entirely separate board area and path for the analog signals and conditioning circuits. The two boards are interconnected by a high density 2 piece connector. The arrangement is shown in Figures 8 for the ATCA carrier.

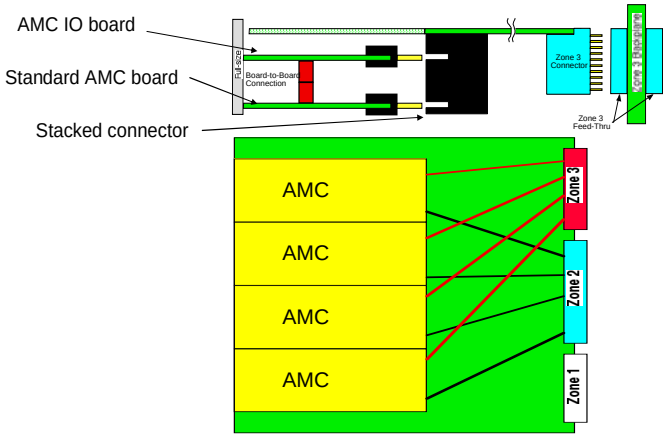

Figure 8: ATCA Carrier & Stacked AMC's for IO (Courtesy R. Downing, SLAC)

2. MicroTCA & MicroRTM IO

The same AMC stacked solution can be adapted to an MTCA shelf with a MicroRTM. Figure 9 shows the same stacked AMC board plugged into a (to be designed) MTCA shelf in which every other connector is designated as an IO connector, and the backplane has feedthrough connectors on the rear for mating with a MicroRTM (µRTM, also to be designed).

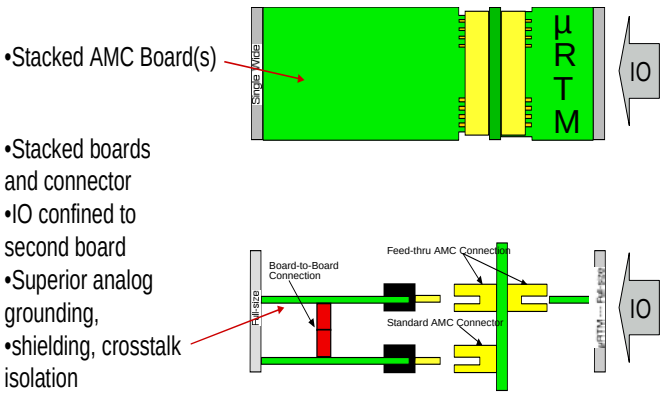

Figure 9: Stacked AMC Board in MTCA Shelf with µRTM (Courtesy R. Downing, SLAC)

Stacked AMC connectors and feedthroughs have been already developed by at least two vendors for use in both standard MTCA modules (e.g. MCH) and MTCA shelf backplanes. This version of a stacked module with separate connector seems a perfectly acceptable IO option for either ATCA or MTCA carriers.

3. Timing & Synchronization

Another physics requirement for the above examples is the need to distribute to every data acquisition card slot precise timing clock and triggering references, phase-locked to the machine clock and RF system to very high precision. In the above examples it was first proposed to solve this by adding a second section of backplane into the RTM zone for clock ad trigger distribution; however a preferred solution is to use excess existing backplane lines in a dual star or mesh configuration from a control slot in the backplane. It is highly desirable to define a timing distribution standard for physics use to achieve as wide interoperability of designs as possible. The most recent proposal to use existing lines has many advantages, including superior isolation of timing disturbances of a module being swapped from impacting timing in other payload locations.

4. Communication Protocols

Another important requirement is to specify the communication protocols allowable in physics systems between ATCA modules and between AMC modules on carrier boards, and to minimize the number of options. There is a need for very low latency protocols in real-time fast machine feedback systems as well as the predominant GbE and PCIe between AMCs and GbE between ATCA modules and external to the shelf. It will also be necessary to employ simple custom protocols at the lowest levels of fast real-time response in feedback control systems. Multiple protocols can are already accommodated within xTCA designs by an E-Keying strategy in which every unique module has a profile known to the system manager and will be prevented from interfering with other dissimilar modules in the same shelf.

IV. HIGH AVAILABILITY SYSTEM DESIGN & INTRLLIGENT PLATFORM MANAGEMENT (IPMI)

Physics machines are some of the most complex machines ever built and are often the most difficult to keep running efficiently in the face of potentially tens of thousands of single points of failure. Ideally, once brought into full operation, physics machines should run flawlessly until the end of their designed schedule or "mission period." Some accelerators are planned to run 24/7 for 9 months of the year, for a mission time of 6000 hours. If HA design strategies are employed in all subsystems of the machine, including controls, magnet and RF power systems, vacuum, plant water and power etc., then machine availability during the mission period of 99% or better is realizable[3]. The larger the machine, the more difficult this becomes [3].

In large accelerator systems, single points of failure can be mitigated through N+1 redundant design in which the load of a failed power supply module, for example, is immediately assumed by its N neighbors and operation continues

[3] N+1 design principles are applicable to all physics machine subsystems such as magnet power, RF power, vacuum, cryogenics, plant power and water. See Ref. [3]. For purposes of this paper, we assume the principles are understood and focus on additional ATCA requirements for physics instrumentation and control applications and proposals for meeting them.

uninterrupted. For another example, in a linac N+1 redundant RF stations are always provided so that if one trips off, even momentarily due to a klystron or waveguide arc, a hot standby station is automatically switched in (by changing the trigger time from "standby" to "on-beam") to compensate for the loss beam energy. Again, machine operation is uninterrupted while the faulty unit is reset or failed components are replaced as necessary.

Many accelerator and detector subsystems already employ monitoring diagnostics to aid in the detection and repair of malfunctions, constantly reading out the health of the system and its environment. However these are often designed by independent collaborator subsystem groups with no enforced module or platform interoperability requirements and generally not designed for auto-failover. Aside from needless duplication of infrastructure engineering design, operating performance is compromised and commissioning, system tester design and long-term maintenance effort multiplied in direct proportion to the number of different subsystems.

ATCA has incorporated an imbedded management sub-layer known as IPMI (Intelligent Platform Management Interface)[4] into the standard. Figure 10 shows the concept. A shelf manager communicates with a local controller (IPMC) on the carrier module or MCH (MCMC), which in turn communicates with the AMC modules under local control. Each AMC has an imbedded Module Management Controller (MMC) which gathers information determined by the designer Environmental information for power and cooling control is also gathered into a local Sensor Data Register (SDR). IPMI can also be extended to remote "non-managed FRU's" (Field Replaceable Units) as depicted in Figure 11.

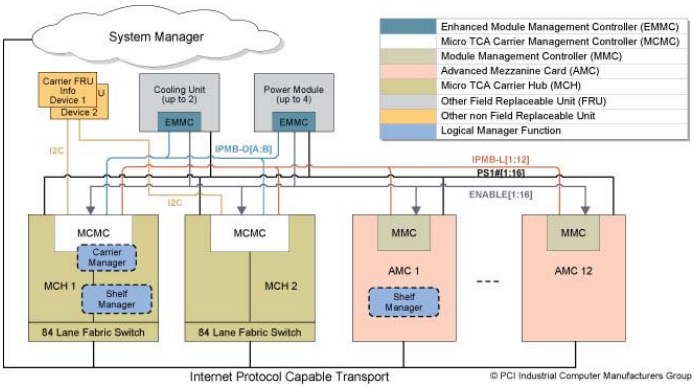

Figure 10: Intelligent Platform Management Architecture (Courtesy C. Engels, Emerson)

The IPM system offers one of the most important possibilities for major performance improvements in the large machines. The IPMI is a tool to monitor all critical operating information and warn of signs of abnormality, take evasive action, and isolate a module for hot-swap. The IPMI used by PICMG has a decade of operational experience and can be either imbedded into customer designs or purchased with integrated systems, as for example in all xTCA shelf products. IPMI is mandatory for managing physics design interoperability.

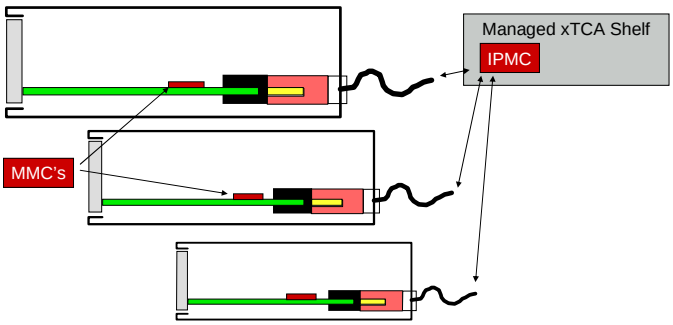

Figure 11: Remote FRU's under IPMI Management (Courtesy R. Downing)

Clearly xTCA IPMI reference designs will have broad application in both machine controls and DAQ systems, with extensions to non-managed devices providing an enterprise-wide intelligent platform management capability. The physics community should collaborate on IPMI reference designs that can be shared and made readily available through industry. Examples of some non-managed implementations for power systems have been prototyped [4, 5].

V. XTCA FOR PHYSICS GOALS SUMMARY

The foregoing discussion suggests a list of goals for physics xTCA specification collaboration. The committee should develop the following *Reference Designs* as an integrated toolset for the community:

1. ATCA board including IPMI, power architecture, scalable data fabric interface and scalable FPGA logic section to receive serial or parallel data inputs.
2. ATCA Zone 3 RTM with high performance connector, IPMI and managed power extension from ATCA board to RTM. Note that Zone 3 connector options may be needed by users but IPMI and power should be standard on the RTM
3. ATCA timing and synchronization distribution to all module slots. Options are (i) distribute over existing star fabric lines designated optional use; or (ii) add extension to backplane in RTM Zone 3
4. MTCA AMC reference design with provision for rear IO (as well as front panel IO). Options are (i) single wide with re-allocated lines in fabric backplane; (ii) stacked single board and connector with every other slot available for IO and timing; (iii) double wide board with additional connector for IO and timing
5. MTCA shelf and backplane design including rear IO option plus timing and synchronization distribution
6. IPMC embeddable controller and software for extension to non-managed devices.

[4] IPMI was developed by a consortium of Intel, HP, NEC and Dell. IPMI Specification and licensing agreements are available from Intel Corporation at: http://www.intel.com/design/servers/ipmi/index.htm.

7. SOFTWARE structure and protocol selection to demonstrate operation under real test conditions in typical applications. Ideally merged with hardware demonstration of prototypes

These goals should be developed in close collaboration with the PICMG industry partners who will provide prototypes for physics evaluation. This will require coordinated parallel prototype development effort in mechanics, electronics and software design.

VI. XTCA EARLY PHYSICS EXPERIENCE

Physics applications are currently being prototyped on both ATCA and MTCA platforms. The ATCA IO prototype solution is shown in Figure 12. Proposed concepts for MTCA AMC modules and shelf are shown in Figures 13 and 14.

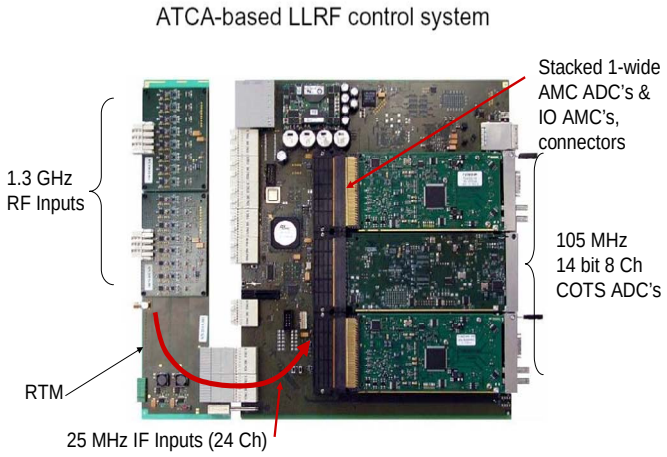

Figure 12: Physics Implementation of AMC Stacked Board Carrier (Courtesy W. Koprek & T. Jezynski, DESY)

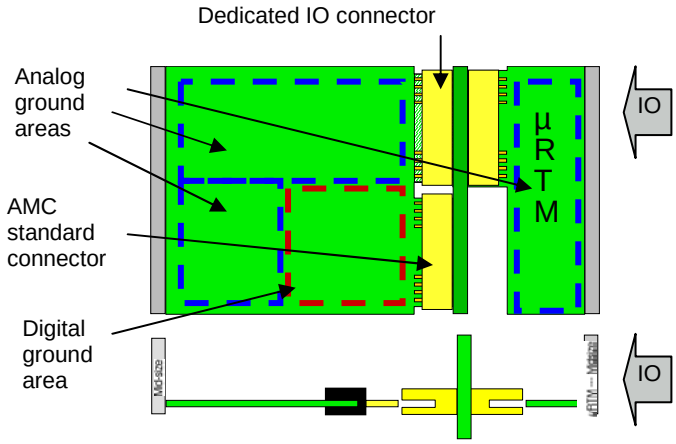

Figure 13: Double Wide AMC with IO via µRTM (Courtesy R. Downing)

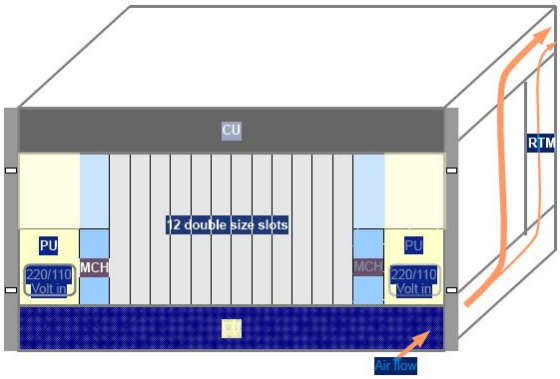

Figure 14: MTCA Shelf 12 AMC Payload Slots Rear IO µRTM (Courtesy K. Rehlich, DESY)

Figure 13 shows the proposal for MTCA rear IO, namely a double wide AMC card with an added IO connector in Zone 3. This provides a larger payload design space for the analog section and avoids conflicts between analog and digital lines and ground planes. The corresponding shelf concept is shown in Figure 14.

Several machine control applications are exploring the use of AMCs in an MTCA chassis for interlocks and controls including RF fast feedback control. RTM, IO and timing distribution must be incorporated beyond the existing standard specifications. The main reason for RTM is to avoid handling cables while exchanging modules, especially for RF, clock synchronization or precise sampling trigger signals where mere flexing of cables changes delays enough to require recalibration, aside from potentially damaging a flexed RF cable.

VII. ACHIEVING PHYSICS XTCA INTEROPERABILITY

The goal of all standards efforts from the commercial user point of view is "interoperability," The entire reason for the invention of ATCA was the realization by competing telecom providers that they could no longer afford the development costs of unique proprietary products and that both providers and customers would benefit by adopting a common interoperable architecture and infrastructure. Thus providers can concentrate on unique developments within that infrastructure to bring new economical products to market in the shortest possible time, responding to new-technology advances quickly without having to constantly reinvent infrastructure. For the physics community to achieve similar benefits for its relatively small niche market it needs to adopt as many of the existing standards as possible, and collaborate on developing standard extensions where no standards exist.

Besides benefits on the engineering and "time-to-market" sides, the benefits to service and maintenance operations are even greater in minimizing total life-cycle costs of machine subsystems.

VIII. INTEROPERABILITY TESTING WITHIN PICMG

Physics standards of the past achieved a high degree of hardware compatibility but limited success in driver and diagnostics software compatibility. Adopting the xTCA standard for physics offers a new opportunity to reach much further than before into both hardware and software interoperability. Industry has defined interoperability standards for compatibility of products and independent consortia have been set up both for software and middleware development, and for testing against benchmarks before a new product can claim to be ATCA or AMC compliant. A number of such independent consortia collaborate both to extend the open standards to include hardware and applications interfaces that all systems need at some level, to maintain these standards, and to evaluate the products that use them. Consortia collaborating with PICMG include the Service Availability Forum (SAF) for software and middleware, Linux Foundation, Scope Alliance and Communications Platforms Trade Association (CP-TA). CP-TA organizes "Interoperability Fests" where new products are brought together and evaluated by a group of engineers from the represented companies. The physics community has been invited to join these efforts at the appropriate future time when it (or providers building physic products) have new products to test. The organization relationships are depicted in Figure 15.

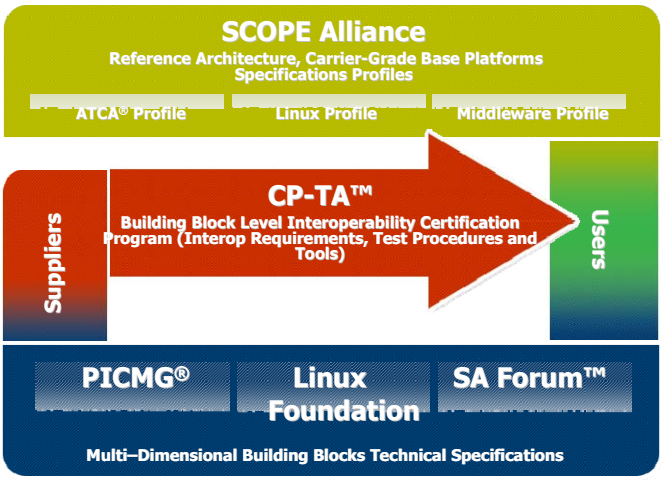

Figure 15: Inter-relationships of PICMG Supporting Consortia (Courtesy J. Fryer, President SAF, Emerson)

IX. PICMG XTCA FOR PHYSICS COORDINATING COMMITTEE

After discussions of special physics needs at two ATCA workshops in 2007 and 2008, the community was encouraged to form a Technical Subcommittee under PICMG to further its interests. This committee, sponsored initially by four labs[5] that joined PICMG as Executive Members and two companies[6], became approved and held its first organizing meeting on March 10, 2009. PICMG The organization, shown in Figure 16, includes two separate PICMG Technical Subcommittees.

[5] SLAC, DESY, IHEP and FNAL
[6] Performance Technologies, Cypress Point Research

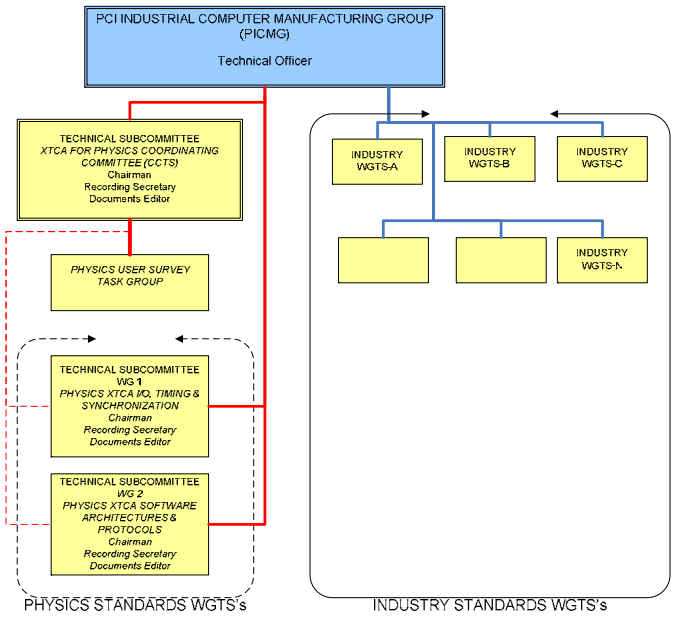

Figure 16: PICMG Physics Coordinating Committee Technical Subcommittee and Working Groups 1&2 Technical Subcommittees

The CCTS and all Technical Subcommittees report directly to the PICMG Technical Officer as shown.

Technical Subcommittees are open to any corporate member that wants to join through a Call for Participation (CFP). PICMG Technical Subcommittees are established based on a specific Statement of Work (SOW) and timeline; when their work is completed they are disbanded until a new need arises. However, the Physics Coordinating Committee (CCTS) will have a continuing role to help establish new Working Group Technical Subcommittees (WGTS's) for physics and to monitor their work products prior to submittal to PICMG for formal vote. The CCTS now has 44 corporate members with 71 individuals authorized to attend the web-based meetings; attendance for the CCTS is typically 20-25 members.

After several weeks of discussing the issues mentioned above, the CCTS has moved to sponsor the two Working Groups, one for hardware and one for software issues. The Preliminary SOW's with the CFP's for both were issued, applications closed May 7, 2009, officers were elected and regular weekly meetings began in late May-early June 2009.

The preliminary SOW's for WG's 1&2 read as follows:

WG1: Physics xTCA I/O, Timing and Synchronization Working Group

A. Introduction

This Working Group's main task is to define Rear I/O for AMC modules. The task has many side affects. The ATCA carrier and the µTCA shelf have to accommodate these AMC's. A new component, the µRTM has to be defined. Additions will have to be made to the µTCA Shelf specification to accommodate the µRTM. The AMC Rear I/O will impact the design of the ATCA carrier RTM. Lastly, lines will need to be identified for clocks, gates, and triggers that are commonly used in Physics data acquisition systems. The complication for this Working Group will be how to mesh all the requirements into a coherent design and specification(s).

B. Tasks:

- Specify AMC's with Rear I/O (AMC-IO) and an associated µRTM
- Consider the potential need for Mezzanine Cards..
- Specify the ATCA carrier for the AMC-IO.
- Specify an ATCA RTM module that will accommodate the AMC-IO along with support features such as power, management, JTAG, etc.
- Specify e-keying code extensions to the Shelf Management Section to accommodate the additions to the AMC, RTM, µRTM and the µTCA shelf specifications.
- Specify lines, both bussed and radial, that are in both ATCA and µTCA backplanes that could be used for Physics clocks, gates and triggers. If necessary, specify lines that are not in the ATCA and µTCA backplanes but could be added to the RTM and/or µRTM for such use.

C. Requirements & Constraints:

- The Working Group will strive for maximum compatibility with current ATCA, AMC and µTCA hardware. If some incompatibility is necessary it will be documented and its impact on other specifications clearly noted.
- The AMC-IO must fit within the envelope of the current ATCA Carrier or the µTCA shelf, except for increased shelf rear depth and hardware to accommodate the µRTMs. Only the layout of the backplane(s) in the shelf will be impacted by the Rear I/O specification. If a connector different from the AMC is chosen it should not require a change in the envelope.
- The proposed specification shall be tested against real physics implementations.
- The Working Group will deliver proposed specifications to the xTCA for Physics Coordinating Committee for pre-approval before submitting to PICMG for ballot.

WG2: Physics xTCA Software Architectures and Protocols Working Group

D. Introduction

This working group is chartered to define a common set of software architectures and supporting infrastructure that will facilitate inter-operability and portability of both hardware and software modules among the various applications developed for the Physics xTCA platform and that will minimize the development effort and time required to construct experiments and systems using that platform.

E. Tasks

- Define protocols and APIs for management and control of real-time data acquisition and machine-control components, to include calibration, synchronization, and triggering mechanisms.
- Define protocols and APIs for high-rate and low-latency distribution of data among the various data acquisition, machine-control, data processing, data storage, and data transmission components, including use of the backplane fabrics within shelves and use of external links between shelves.
- Define the mechanisms and techniques within the ATCA/µTCA infrastructure to manage component-, shelf-, subsystem-, experiment-, and facility-level redundancy and automated failover.
- Define protocols and APIs for management of resources within an xTCA network, including identification and allocation of common functional modules among subsystems and experiments, management of active module disposition and status, and auditing of component usage and maintenance.
- Define a common set of APIs and functional blocks at the software and FPGA firmware levels to be provided as a standard development library for xTCA application development, including standard operating system and thread management functions, module identification and data routing functions, standard I/O management functions, and standard data processing blocks.

F. Requirements and Constraints

- The working group shall strive for maximum compatibility with existing ATCA, µTCA and AMC specifications.
- Wherever possible the working groups shall make use of existing and well-supported standards and/or fielded implementations as the basis for guidelines and specifications.
- Prior to release for balloting proposed specifications and guidelines shall be validated against real-world physics implementations and applications through use of architecture-level paper designs and/or analyses.
- The working group shall deliver proposed specifications and guidelines to the xTCA for Physics Coordinating Committee for pre-approval before submission to PICMG for balloting.

X. FUTURE PLANS

The deliverables for the WG's will be specification documents that will be published as an extension to the three main existing standards for ATCA, AMC and MTCA. The specifications will be tested through collaboration with industry participants to product example prototypes for testing by interested laboratory potential customers.

In addition to establishing the Working Groups, the CCTS will conduct a survey of requirements of major laboratories and users known to be interested in participating in standards development.

A web page will be posted shortly in a public area of the PICMG site (www.picmg.org) to provide background information as well as instructions on how to participate in the CCTS, WG's or both. The quality of WG results will depend directly on the quality and level of effort of the participants. T

Schedules will be set for task results by each WG, but the CCTS goal is to complete the most urgent tasks of MTCA with IO, Timing and Synchronization, and AMC physics options by end of calendar 2009 with prototypes being developed in parallel. The CCTS will conduct the user survey, monitor results and review WG work products once they are ready to be submitted to PICMG

Although we can anticipate fairly rapid progress on hardware, it can be expected that the software WG will need to collaborate with some of the existing affiliated consortia mentioned above, in particular the very active Software Availability Forum and the Scope Alliance, in developing standards or best-practice guidelines for protocols as well as enterprise wide Intelligent Platform Management systems.

XI. CONCLUSIONS

Since many labs are already beginning to apply the standards, collaboration is urgent if the physics community is to successfully develop requirements and specifications for inter-operable hardware-software products that become broadly available through industry. Since the standards exist and the organization is amenable to extensions for physics, there is a

unique opportunity to achieve interoperability of hardware, software and systems-level intelligent platform management. This cooperation at this critical time will make possible future systems where infrastructure is supported by the collaboration and lab efforts can concentrate on the unique problems of bringing new technologies into payload designs.

The process of advancing standards extensions for physics is now well underway with the formation of the new xTCA for Physics Coordinating Committee and the two major working groups for Hardware and Software. There is very large group from both labs and industry in the hardware WG but representation from the labs for Software has still not developed broadly.

The formal Requirements Survey has filed a general plan but has not yet developed an action plan. It will rely on contacts within the various labs to help gather information on requirements as well as individual lab action plans. Meanwhile because several labs, most notably DESY with its new approved accelerator XFEL and SLAC with an impending major controls upgrade, are pushing hard for early solutions, we do have the necessary critical mass to keep both Working Groups moving rapidly.

For success in reaching not just quick solutions but quality results supported by a strong collaboration of both labs and industry, it is imperative that more labs and lab development groups join the effort. There is little doubt that xTCA will be a major player in future lab controls, instrumentation and data acquisition systems, and the new system provides an opportunity to create a major leap in high performance and high availability for next-generation machines and experimental detectors.

The PICMG specifications development structure is designed for organizing quickly, setting clear goals and driving to useful goals in a timely fashion. This is proving to be of tremendous value to the physics community. xTCA is the culmination of efforts by the consortium that includes all the key industry players of existing standards such as VME, VXI, PCI, PMC, IP, etc. The collaboration of lab and industry is expediting progress in that answers to many questions about the existing vast capabilities if xTCA and Intelligent Platform Management systems are quickly answered by knowledgeable industry partners, leading to very rapid progress in identification and convergence of options.

The Committee feels confident it will meet its early goals and chart a fruitful course for the future.

XII. REFERENCES

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