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DEVELOPMENT OF AN ADDER-TOPOLOGY ILC DAMPING RING KICKER MODULATOR*

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Abstract

The ILC damping ring injection and extraction kickers will require high availability modulators that can deliver ±5 kV pulses into 50 Ω with a 2 ns flattop (~1 ns rise and fall time) at up to 6 MHz. An effort is underway at SLAC National Accelerator Laboratory to meet these requirements using a transmission line adder topology to combine the output of an array of ~1 kV modules. The modules employ an ultra-fast hybrid MOSFET/driver that can switch 33 A in 1.2 ns. Experimental results for a scale adder structure are presented.

INTRODUCTION

ILC damping ring kickers will require ±5 kV, 2 ns flattop (~1 ns rise and fall time) pulses at up to 6 MHz repetition rate [1]. However the switching time for the fastest commercially available power MOSFETs is about 3 ns [2]. An ultra-fast hybrid MOSFET/driver, recently developed at SLAC, has achieved 1.2 ns switching of 33 A at 1000 V with a single power MOSFET die [3]. By combining the output from an array of these switches in an adder topology, it may be possible to build a modulator to meet the ILC damping ring kicker requirement.

The minimum rise time of the output of a standard inductive adder is twice the transit time through the structure, which would limit the structure length to less than 15 cm to achieve ~ns rise time. A transmission line adder topology can be used to overcome this geometric limitation. Preliminary measurements of a transmission line adder demonstrate that it is capable of adding outputs from several of these ultra-fast switching modules without significantly degrading the switching performance.

DESIGN

The schematic of the transmission line adder is shown in Fig. 1. The adder incorporates four Hybrid MOSFET/driver Switching Modules (HSM). Each HSM is connected to a 4.17 meter long (20 ns delay) RG-402/U 50 ohm coaxial cable. The other end of the cable is connected to an adder PCB. The PCBs are stacked together to create a series connection of the four input cables. The combined output is matched to a 200 ohm load.

The design and assembly of the HSM, transmission line adder and load is discussed in more detail in the following sections.

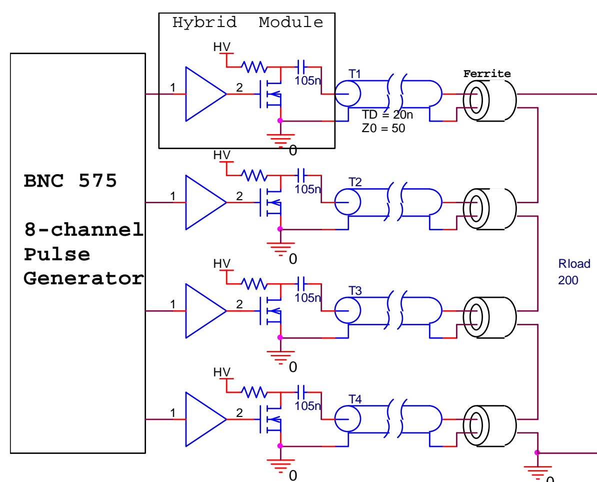

Figure 1: Schematic of transmission line adder.

Hybrid MOSFET/Driver Switch Module

The power MOSFET is intrinsically capable of switching in about 1 ns. But the parasitic inductances in the commercial packages of both the power MOSFET and its driver limit the switching time. In order to make an ultra-fast switching module, a die form power MOSFET and driver are assembled on a low inductance PCB using the low inductance flip-chip method.

The HSMs incorporate four function blocks; energy storage capacitor, power MOSFET, totem pole driver and input buffer as shown in Fig. 2.

The capacitor bank combines five, 2.2 nF, 3kV, C0G capacitors and two, 47 nF, 1000V, X7R capacitors (all 1812 SMD), for a total capacitance of 105 nF. The power MOSFET, M0, is a 1200V die form MOSFET (APT1201R2). Solder bumpers were deposited on the source and gate pad of the MOSFET die. Then the chip was flipped front down, and the source and gate terminals were connected to corresponding pads on the PCB using conductive epoxy. The drain connection was made using sliver paste to the back side of the die (now facing up). The totem pole driver incorporates a 100V P/N MOSFET pair (IRFC120/9120). These bare die MOSFETs were installed using the same flip-chip assembly technique. An IXDD415SI is used as the input buffer to translate the function generator TTL level trigger to high voltage to effectively drive the totem pole gates. The input buffer is capacitively coupled to the totem pole gates, so that the totem pole can be referenced to Vss+ and Vss-.

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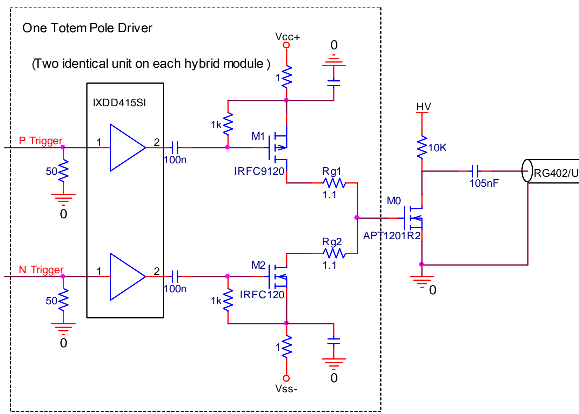

Figure 2: Circuit diagram of an HSM.

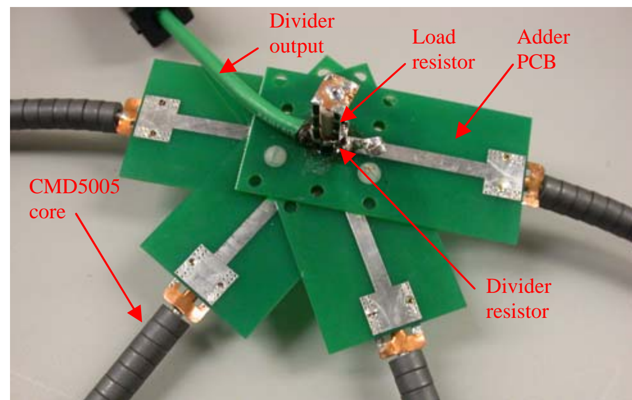

Figure 4: Photo of adder and load.

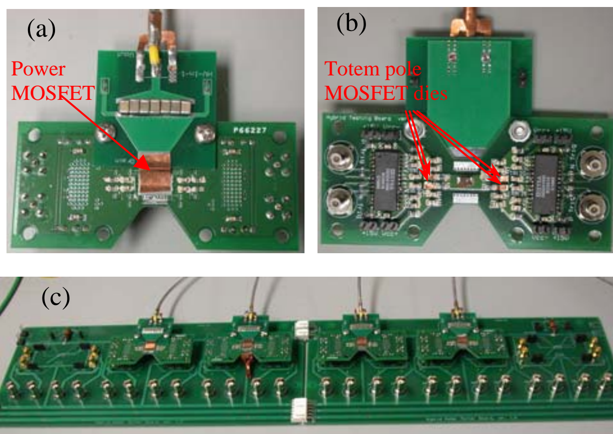

Figure 3: Photos of the HSM. (a) Back side; (b) Front side; (c) 4 HSMs on the motherboard.

Transmission line adder

The output from each HSM is transmitted to the adder by a 4.17 meter long (20 ns) RG402/U coaxial cable. The long cables are used to transit-time isolate any reflections, to simplify analysis of the added waveform. Each cable is inductively isolated at the adder PCB with ferrite cores, 25 pieces of T371818T-CMD5005 (ID:0.187" OD:0.376" H:0.187"), as shown in Fig. 4. These cores isolate each HSM when the high voltage pulse is combined at the adder.

The adder PCB matches the coaxial cable to a 50 Ω strip line formed by the top and bottom layer of the PCB. The PCBs are stacked together so that the top layer trace of one board is connected to the bottom layer of the next board, to achieve a series connection of the HSMs. The adder was designed for up to 6 HSMs, but only 4 were used for these experiments.

A high voltage silicone wire threaded through the 6 mm hole in the adder PCBs forms a coaxial line of ~60 Ω that connects to the resistive load. Although this does not match the 200 Ω load impedance, the transit time of this line, ~40 ps, is so short compared to the risetime of the HSM pulse, ~ 1.4 ns, that it has no effect on the risetime of the adder.

Load and Measurement

The 200 Ω, matched resistive load is formed from an array of cylindrical thick film resistor without trim cut. Twelve 270 Ω HSF-1 resistors in a 4 parallel by 3 series array yield a total measured resistance of 197 Ω.

A resistive divider, formed by placing an ~1 Ω resistor in series with the load (ground side), was used for measurement of the output waveform. The divider drives a 50 Ω cable. The dividing resistor is formed from seven parallel 6.8 Ω HSF-1 resistors. The measured resistance is 0.948 Ω. The overall dividing ratio is 208:1.

RESULTS

The switching characteristic of the HSM was measured at the load end of the 20 ns coaxial cable using a Barth (142-NMFP-26B) attenuator and TDS7154 oscilloscope (1.5 GHz bandwidth, 20 GS/s). A typical switching waveform is shown in Fig. 5. The measured switching time is 1.5 ns into a 50 Ohm load at 1000V charging voltage (faster switching has been obtained using the dual totem pole driver, but only one driver was utilized in these experiments due to the failure of a driver on one of the HSMs). The measured load voltage was 920 V.

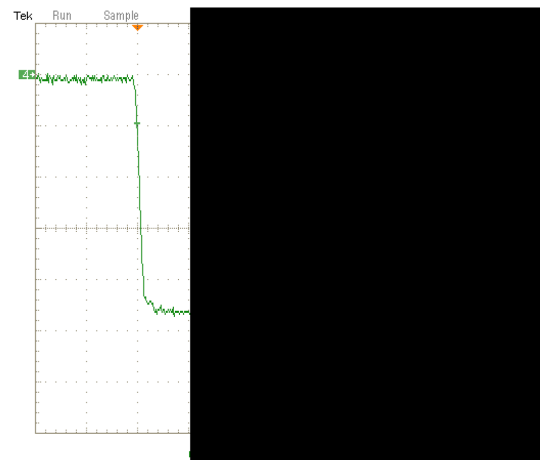

Figure 5: Output of a single HSM into 50 ohm.

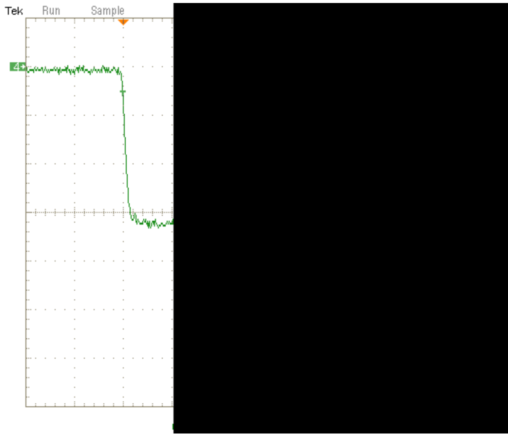

Figure 6: Output of the adder with 4 HSMs combined, 1040 V/div (attenuation ratio: 2080:1).

The calibration of the resistive divider was confirmed against the Barth attenuator by operating the adder with a single HSM.

An 8-channel BNC-575 pulse generator was used to trigger all 4 HSMs. The HSM requires 2 triggers for each of its totem pole drivers; one for turn on and the other for turn off. Each HSM was first tuned by adjusted the relative trigger delay so that the pulse from each individual HSM will arrive at the adder at the same time. Then, all the HSMs were triggered simultaneously to generate the combined pulse shown in Fig. 6. The measured switching time is 1.4 ns.

CONCLUSION

A transmission line adder was designed based on the ultra-fast hybrid MOSFET/driver switching module. The initial test demonstrated the adder can combine pulses with 1.4 ns switching time without any degradation of the switching time.

By operating the HSM with the dual totem pole drivers, the switching time of the HSM can be reduced to 1.2 ns. Further experiment will be conducted to test the adder with these faster pulses.

ACCKNOWLEDGEMENT

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REFERENCES

[1] ILC Reference Design Report, http://www.linearcollider.org/cms/?pid=1000437
[2] G. J. Krausse, “DE-Series Fast Power MOSFET”, Direct Energy Inc. Technical Note, 2002.
[3] T. Tang, C. Burkhart, “Hybrid MOSFET/Driver for ultra-fast switching”, IEEE Trans. on Dielectrics and Electrical Insulation, Aug. 2009, in press.