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RESONANT KICKER SYSTEM DEVELOPMENT AT SLAC*

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Abstract

The design and installation of the Linear Coherent Light Source [1] at SLAC National Accelerator Laboratory has included the development of a kicker system for selective beam bunch dumping. The kicker is based on an LC resonant topology formed by the 50 uF energy storage capacitor and the 64 uH air core magnet load which has a sinusoidal pulse period of 400us. The maximum magnet current is 500 A. The circuit is weakly damped, allowing most of the magnet energy to be recovered in the energy storage capacitor. The kicker runs at a repetition rate of 120Hz. A PLC-based control system provides remote control and monitoring of the kicker via EPICS protocol. Fast timing and interlock signals are converted by discrete peak-detect and sample-hold circuits into DC signals that can be processed by the PLC. The design and experimental characterization of the system are presented.

INTRODUCTION

A 0.85kG-m length integrated magnetic field is the original field required to prevent undesired beam bunches from entering the LCLS (Linear Coherent Light Source) undulator by deflecting them into the beam dump. Given the magnet parameters, generating this field requires a maximum current of 398A. It is necessary to selectively dump LCLS beam on a bunch by bunch basis requiring a pulsed system operable at 120Hz. This is a relatively low repetition rate in comparison with most storage ring kickers easily allowing for a pulse width as long as several milliseconds. The long pulse width accommodates a compact LC resonant design with low charging voltage and low energy storage.

THEORY OF OPERATION

Referring to Fig. 1, capacitor bank *C* is initially charged to the capacitor charging power supply voltage. Although the maximum repetition rate is 120 Hz, the power supply must have enough current capacity to recharge the capacitor bank between consecutive current pulses yielding a maximum allowed charging time of 7.83ms.

A trigger pulse generates the start of a single-cycle sinusoidal current pulse to the magnet. From this initial trigger, two one-shots will be generated: the first to turn IGBT (insulated gate bipolar transistor) S_1 off for the duration of the single-cycle output current pulse providing isolation from the power supply. The second one-shot will turn transistor S_2 on for a time slightly longer than the positive half cycle of the current pulse produced by the resonance of *C* with inductance *L*. At the end of the positive half cycle, *C* will have a negative polarity. The anti-parallel diode in *S2* provides a path for the remaining energy in the capacitor to be recovered through the magnet. In Fig. 1, *Rp* and *L* represent the series resistance and inductance of the cabling and the magnet. Neglecting parasitic resistance, the peak current of the magnet is given by:

$$I_{peak} = V_{charge}\sqrt{\frac{C}{L}} \tag{1}$$

The full sine wave pulse period is given by:

$$\tau = 2\pi\sqrt{LC} \tag{2}$$

The kicker is operated at the LCLS beam rate. This provides confirmation that the kicker is operable and maintains thermal equilibrium for maximum pulse repetition stability. When beam is to be transported to the undulator (not aborted to the dump) the pulser triggers are adjusted to move the pulse "off beam," so that the pulsed magnetic field does not interact with the beam bunches.

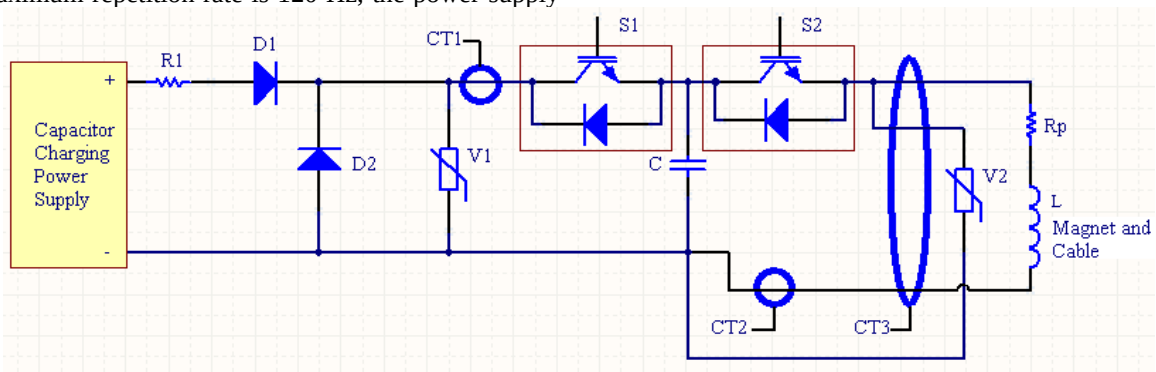

Figure 1: Kicker Schematic

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CIRCUIT BEHAVIOR

The circuit component parameters include a 50uF capacitor, a 64uH magnet, and a ~29uH cable. Using equations (1) and (2) the kicker should provide a 323A peak magnet current in a 428us sinusoidal pulse. As shown in fig. 2, the actual pulse width is 400us and the peak current is 303A. The decrease in peak current relative to calculated values can be attributed to the parasitic resistance. Fig. 2 also shows the decrease in capacitor voltage from 440V to 255V. This corresponds to a 66% energy loss over the duration of the pulse. This loss in energy can be attributed to parasitic resistive heating.

Fig. 3 displays the pulser firing 303A at the maximum repetition rate of 120Hz. CH2 displays the output current of the capacitor charging power supply. The charging current is composed of multiple charge packets. As these packets charge the energy storage capacitor the result is an incremental change in capacitor voltage as evidenced by the linear slope of CH1 during the charging period.

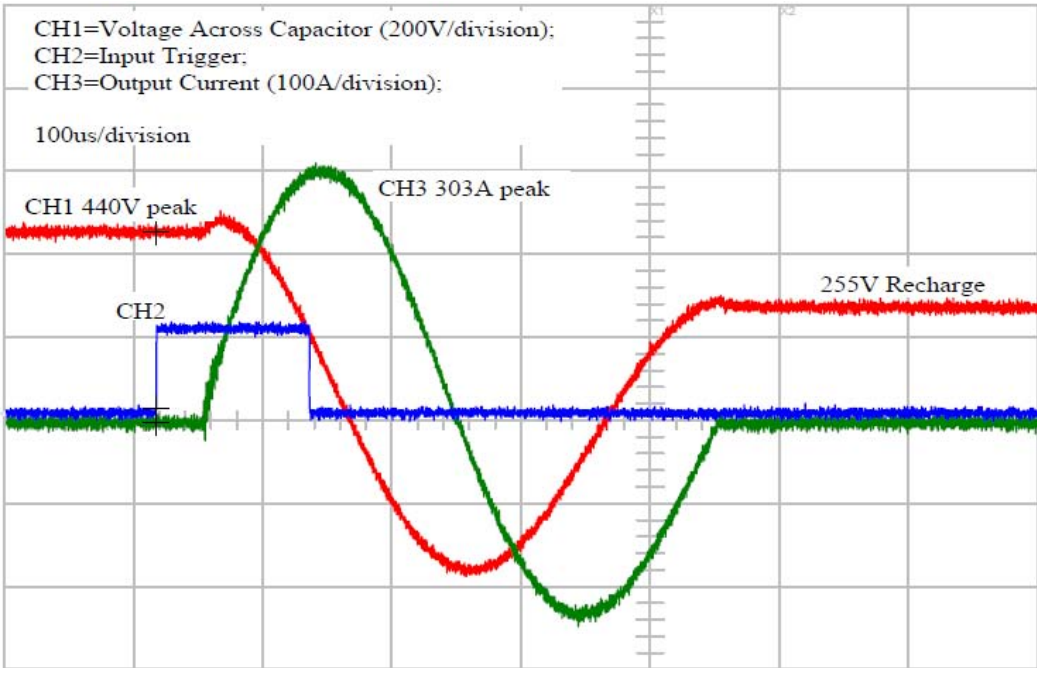

Figure 2: Single Pulse Waveform

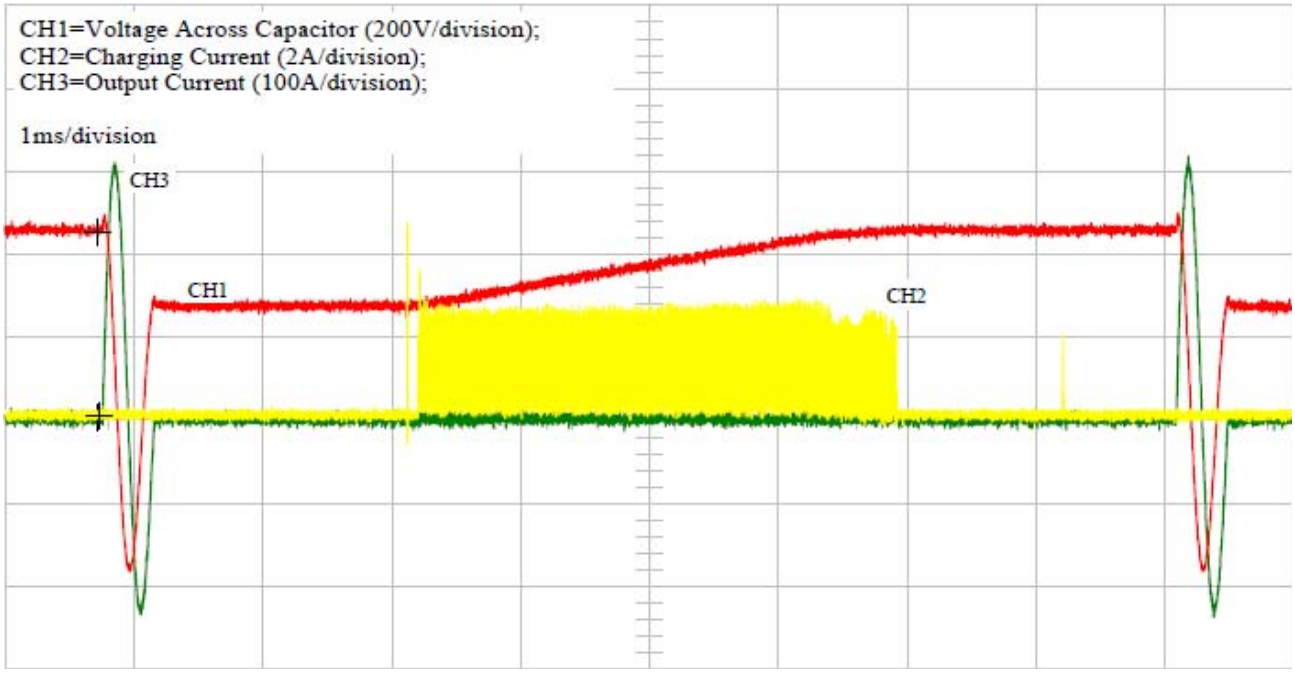

Figure 3: Multi-pulse waveform

PROTECTION CIRCUITS

Several protection circuits have been integrated into the design to mitigate over voltage and over current fault conditions. To maintain a constant impedance load necessary for circuit operation it is important that the current path does not include parasitic ground returns. Referencing Fig. 1, current transformer *CT3* senses any ground current faults by measuring the differential current between the output and return cable. Additionally, *CT3* measures any current shunted by varistor *V2* due to a *S2* overvoltage condition. Upon *CT3* sensing significant differential current, the pulser shuts down mid-pulse. Similarly, the output pulse is terminated in the event of excessive load current, as measured by current transducer *CT2.*

The capacitor charging power supply is isolated from high voltage transients in the pulser by diode *D1*. Diode *D2* provides a path for high current flow in case *S1* were to close mid-pulse. *R1* has been added to inhibit current flow through the power supply during this fault mode. *CT1* measures this fault current and shuts off the pulser. Varistor *V1* is added to prevent an overvoltage failure of *S1* if the switch were to open while conducting high fault currents.

CONTROLS

The kicker system is divided into three enclosures; the charging supply, pulser, and PLC (programmable logic controller) chassis. Fast kicker signals, generated by the LCLS timing system, are processed by a discrete analog control board located within the pulser chassis. Trigger signals are processed by this control board and fed to the IGBT gate drivers. Capacitor voltage, charging current, output current, and differential current are measured and fed into the control board. Over current conditions of any current signal inhibits the pulser mid-pulse. This inhibit signal is also converted to a 2 second pulse and sent to the PLC which then shuts down the kicker system and catalogues the fault. Peak current and voltage values are sampled by the control board and sent to the PLC providing easily accessible voltage and current monitoring.

The PLC controls the capacitor charging supply with the ability to enable the power supply, control the set-point voltage, monitor the output voltage, and monitor power supply faults. Additionally the PLC monitors temperature sensor faults within the pulser and magnets. Upon fault conditions the PLC inhibits the pulser, disables the power supply, and catalogues the fault information. The PLC can be controlled via touch screen or the SLAC control system using EPICS (Experimental Physics and Industrial Control System) protocol.

DESIGN CONSIDERATIONS

The relatively low voltage and energy storage of the system allow for a compact pulser chassis (10.5’’x20”x19”) as shown in Fig. 4. Because the high current IGBT and anti-parallel diode switch under either zero voltage or zero current conditions the switching losses are very small allowing for air cooling of the pulser.

Figure 4: Pulser Chassis

A four conductor 2AWG cable was used to connect to the magnet. The supply and return path each use 2 parallel conductors. This arrangement allows for high average current while minimizing the inductance of the cable. The cable has an aluminum shield that is grounded at the pulser allowing for control of stray capacitance.

REFERENCES

[1] http://ssrl.slac.stanford.edu/lcls/