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# Summary

This paper describes the design, fabrication and test results of a modulator for the 220 kW S-Band klystrons which are part of the proposed beam recirculating system at the Stanford Linear Accelerator Center.

The unit consists of a conventional three-phasebridge power supply, an energy storage bank and a series modulator, with hard switch tube and associated driver circuitry.

Modulator parameters are as follows:

Pulse Voltage	32 to 37 kV Peak
Pulse Current	15 A Peak
Repetition Rate	0 to 44,000 pps
Pulse Width	2.5 µs Flat Top
Duty Cycle	13% max.

The driver circuitry floats at the switch tube cathode potential of 41 kVdc. The paper details the difficulties encountered in designing the pulse coupling, driver stages and protective circuitry. Test results are presented with pictures of pulse shapes.

Final consideration is given the latest proposal of powering 500 kW S-Band klystrons at the same repetition rate and duty cycle and adaptation of the existing modulator with minimal changes to its circuitry.

## Introduction

One of the proposals for increasing the energy of the Stanford Linear Accelerator calls for recirculating the electron beam through the accelerator structure before reinjecting it for a second accelerating pass. During the storage time of 2.8 ms (which is the full interpulse period based on operation at 360 pulses per second), the beam would be completing 122 revolutions. Beam losses due to synchrotron radiation were to be compensated for by 16 klystrons operating at the accelerator frequency of 2856 MHz and pulsed at a repetition rate of 43500 pulses per second (corresponding to the recirculating period of about 23  $\mu$ s).

In order to prove the feasibility of the loss compensation system we decided to build one working prototype RF amplifier. Budgetary considerations forced us to use many parts available around the SLAC site which were not optimally suited for the task at hand: for example, the cabinet was too small for the number and size of components and assemblies and the main capacitor was too low in voltage and too high in inductance necessitating series connection of two units and adding a high frequency one in parallel (which did not help the size limitation of the cabinet and was not fully effective in removing the beam voltage pulse top ringing).

## General Considerations

The proposed klystrons were to have the following characteristics:

Peak RF Output	220 kW
RF Pulse Width (Flat Top)	2.5 µs
Repetition Rate	43,500 pps
RF Duty Cycle	11%
Peak Beam Voltage	37 kV
Peak Beam Current	14.8 A

An existing low duty cycle klystron was redesigned and modified to take the higher average power and repetition rate. The amplifier used during system tests had its cathode structure submersed in a small oil container to minimize corona discharge around the ceramic insulator (which did not particularly help the total load capacitance).

The high repetition rate coupled with the available recovery time of less than 20  $\mu$ s all but dictated the use of a hard tube switching circuit and since voltage and current requirements were moderate, we circumvented the problems associated with pulse transformers at high duty cycles by choosing a series switch arrangement. (Fig. 1)

Since the dc supply has to provide not only the klystron current but also the charging current for all the capacitances in the switch tube plate and klystron, cathode circuits, the modulator pulse has to be wider than the RF pulse. A further increase seemed necessary to exclude a period of anticipated ringing at the beginning of the flat top from getting into the RF pulse. Assuming a voltage pulse flat top of 2.6  $\mu s$  and a total (load and stray) capacitance of 300 pF, the average load current and modulator duty came out to be approximately 2 A and 13% respectively. Therefore the switch tube had to hold off at least the klystron voltage plus its own drop and pass 15 A of plate current with reasonable drive requirements.

We selected an Eimac Y499 tetrode which is a specially processed 4CX35000C with a voltage hold-off capability of 55 kVdc. At 2 kV drop this tube delivers more than 20 A of plate current with zero volts at the control grid and 1000 V at the screen grid. The constant current characteristics are such that any dc voltage changes, including those due to line voltage fluctuations, are attenuated by a factor of two. By setting the nominal tube drop at 4 kV it was possible to absorb - 2 kV of dc voltage changes and still operate at full load current and within the tube dissipation rating. As a consequence we built a power supply with an output rating of 41 kV at 2 Adc.

The ac power at 530 V is stepped up to 31 kV line to line in the main power supply transformer. The input voltage was chosen to facilitate use of the unit at various locations and from different sources: during modulator tests at 530 V from a variable transformer, during production tests at 480 V using an auxiliary boost transformer, and finally in our klystron gallery at 590 V from the existing induction voltage regulators using the auxiliary transformer in a bucking arrangement. The high voltage from the

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Published in the IEEE Conference Record of the 1973 Eleventh Modulator Symposium, pp. 47-55. 73-CHO773-2 ED. Symposium held in New York City, September 18-19, 1973. wye connected secondary is rectified in a conventional three phase bridge circuit resulting in a dc output of 41 kV at 2 A.

A single section filter composed of a 20 H choke and two 2.7 µF, 25 kVdc capacitors in series reduces the 360 Hz ripple to about 35 V peak to peak. The filter capacitor also supplies the load current of 15 A resulting in a droop of 25 V during each pulse. The stored energy is approximately 1200 joules. A 13 **G** resistor was added in series between switch tube and klystron to keep the energy dissipated in the load below a safe level of 10 joules in the event of simultaneous arcs in both tubes.

# Modulator

The grid driver shown in Fig. 1 is of the floating deck type. We chose this circuit because of its inherent high speed capability and good efficiency even though it is more dangerous to service on a routine basis. The driver has to supply all the control and screen grid voltages necessary to hold the switch tube at cutoff during the interpulse period, drive it into conduction for the pulse time and return it to cutoff after the pulse. As a screen supply we used two available regulated supplies of 450 V each in series. Since the grid did not have to be driven positive, the driver could be relatively small and simple, or so we thought.

Our first driver circuit is shown in Fig. 2. It consists of bootstrap amplifier V1, cathode follower V2 and tail biter tubes V4 and V5. All tubes are normally biased at or near cutoff. A full width pulse, generated at ground level, is fed through a pulse transformer with high voltage isolation to the grid of V1. V1 conducts, thereby turning on V2 which raises its cathode and the switch tube grid potential from -700V to approximately zero volts. The pulse transformer fall time is sampled and differentiated by the tail biter circuit, and fed to V4 and V5. Both tubes conduct and discharge V2 and V3 grid circuits respectively.

In testing we found the driver to work very satisfactorily without the isolation pulse transformer. Rise and fall times of 80 ns were realized at the switch tube grid with very good flat top characteristics and little change in pulse shape between low and full repetition rates. Even with a pulse transformer the drive pulse was quite acceptable as long as primary and secondary were at the same reference level and as long as the repetition rate was below approximately 20,000 pps. At the higher rates the transformer would not reset sufficiently. Changing to a light link coupling, the necessary high level amplifier circuitry turned out to be quite bulky and the bootstrap was not capable of supplying the required charging current.

A new circuit was tried using the existing cathode follower and most of the bias and plate supplies but replacing the full width transformer coupling system with one employing separate start and stop triggers and substituting a multivibrator for the bootstrap stage. (Fig. 3)

Briefly, this circuit works as follows: a trigger is fed to the low level pulser (at ground potential). This pulser produces two output triggers, the time separation of which determines the modulator pulse width. The voltage isolating system we used to couple the triggers from ground level to the driver deck, which sits at 41 kVdc nominally, employes small low cost components and provides enough common mode rejection to eliminate feedback from "deck bounce". Start and stop channels each consist of two low voltage pulse transformers and four TV type 500 pF, 30 kV capacitors for high voltage isolation, each leg having two capacitors in series. The transformer center taps are tied to their respective reference levels, giving us a balanced system with inherent common mode rejection. The first trigger passes through the "start" channel and turns off V2-V5 which are normally conducting. The multivibrator changes state, Vl turns on, and a positive pulse is fed to cathode follower V7. The V2-V5 plate resistor was selected to be lk ${oldsymbol Q}$  in order to obtain a good rise time, even though it has to dissipate nearly 1 kW. The cathode follower is used to rapidly charge the 500 pF input capacitance of the main switch tube.

The stop trigger resets the flip flop to its original condition by turning off Vl, thus terminating the output pulse. The stop trigger also momentarily turns on tail biter tube V6 which rapidly discharges the main switch tube input capacitance by driving the grid more negative than its normal -700 V bias level, resulting in a measured drive pulse fall time of 80 ns. Since we utilized dc coupling throughout the driver there was no change visible in the drive pulse shape when the repetition rate was varied between 10 and 44,000 pps.

This circuit was used to check out the klystron for hundreds of hours, yet we were not completely satisfied with the output voltage waveform. At the grid of the switch tube the measured rise time was 80 ns from the 10% to 90% points, but due to the l k $\Omega$  driving impedance into the cathode follower grid, it took an additional 400 ns to reach the steady state value. Peaking in the plates of V2 through V5 helped, but was abandoned because it introduced some ringing on the pulse top.

The klystron beam voltage pulse (inverted) is shown in Fig. 5. Rise and fall times are about 0.5 and 1.5 µs respectively. The long fall time results from the load and stray capacitances being discharged through the klystron's rising resistance with decreasing voltage while the switch tube is cutoff. To compensate for the additional time required to reach pulse steady state voltage, the modulator pulse width was increased by approximately 500 ns and the RF pulse was delayed to fall within the flat top. As a consequence the modulator efficiency suffered. Therefore, we decided to modify the driver circuit to obtain better rise time and efficiency. Again we utilized as many of the existing power supplies and other components as possible (Fig. 4). The new circuit (Model 3) works as follows:

VI-V8 are 8 parallel tubes (6LQ6's) bootstrapped to the grid of switch tube V9. They are cutoff during the interpulse time. A low level pulse generator at ground level drives a light emitting diode (LED) for 0.3  $\mu$ s. The light is transmitted through a fiber optics bundle to the deck illuminating a photo transistor. The fiber optics bundle provides the necessary high voltage isolation between ground and deck. The photo transistor triggers an IC type monostable multivibrator programmed to generate the necessary pulse width of 2.6  $\mu$ s. The 5 V output pulse from the multivibrator is stepped up to a positive 100 V pulse by a low level tube type amplifier, fed into the grids of V1-V8 which in turn deliver a drive pulse to the grid of switch tube V9. Clipper tube V10 holds the V9 grid drive at approximately zero volts. At the end of the pulse VI-V8 turn off and the grid of V9 returns to cutoff bias.

To minimize klystron voltage changes caused by power supply variations, we included a regulator circuit as part of the grid driver. At our operating voltages, 600 V of bias is sufficient to cut-off the Y499 tube. The output pulse from the bootstrap stage rides on top of the bias supply. Therefore by changing the bias voltage it is possible to vary the switch tube grid voltage and thereby its drop. The regulator circuit works as follows: A decrease in the dc voltage is sampled by a voltage divider connected across the storage capacitor and is fed to the regulator circuit. Its output increases the drive to the transistor shunting a 100 V bias supply which is connected in series with the main 600 V bias supply. The total bias is reduced and the V9 grid drive increases, resulting in a decrease in switch tube drop which compensates for the lower power supply voltage.

#### Test Results

Figs. 6-10 show pertinent modulator waveforms. It should be noted that our viewing circuits are not perfect and introduced some ringing. These photographs were taken at the final klystron operating conditions. Because of higher RF gain, the klystron voltage was set at 33 kV rather than the design value of 37 kV. Comparing voltage (Fig. 6) and current (Fig. 8) waveforms, the effect of load capacitance charging can be clearly observed. At the present, phase measurements are being performed and therefore no attempt has yet been made to compensate for droop or otherwise shape the pulse flat top.

## Conclusion

The modulator has worked satisfactorily for over 450 hours. Its reliability has been very good even though two magnetic components (filter choke and filament isolation transformer) experienced voltage breakdown and were redesigned and replaced by the vendor. There has been talk about increasing the peak klystron RF power to 500 kW, requiring 50 kV and 20 A out of the modulator. We are planning to accomplish this using a new HV transformer, a larger rectifier, a higher voltage filter network and a new switch tube (Eimac Y676 rated at 75 kV). We should be able to use the same driver with no modifications because the Y676 has higher gain and lower input capacitance.

## Acknowledgements

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Fig. 1 RLA Modulator Simplified Diagram

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Fig. 2 RLA Modulator Switch Tube Driver Model 1

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Fig. 3 RLA Modulator Switch Tube Driver Model 2



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Fig. 5 Model 2 Driver. Klystron Pulse (shown inverted). Vertical 10 kV/div Horizontal 0.5 µs/div



Fig. 6 Model 3 Driver. Klystron Pulse. Vertical 10 kV/div Horizontal 0.5 µs/div



Fig. 7 Model 3 Driver. Klystron Pulse Rise Time. Vertical 10 kV/div Horizontal 0.2 µs/div



Fig. 8 Model 3 Driver. Klystron Current. Vertical 5 A/div Horizontal 0.5  $\mu s/div$ 



Fig. 9 Model 3 Driver. Switch Tube Grid Voltage. Vertical 200 V/div Horizontal 0.5 µs/div



Fig. 10 Model 3 Driver. Klystron Pulse. Vertical 10 kV/div Horizontal 10  $\mu s/div$ 

NOTE: ALL PHOTOS TAKEN AT 43,500 PULSES PER SECOND.





Fig. 11 Modulator Cabinet

Fig. 12 Switch Tube and Driver



Fig. 13 Klystron Under Test