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CAMAC DATAWAY AND BRANCH HIGHWAY SIGNAL STANDARDS*

R. S. Larsen

Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

Introduction

A CAMAC dataway command operation involves the use of Address, Function, Read or Write, Response, Command Accepted, Timing and Busy lines. Other lines which may be involved are Clear, Inhibit, Initialize and Look-at-me. The dataway signals are as follows:

Read	(R)	Generated in the module
Response	(Q)	
Look-at-me	(L)	
Command Accepted	(X)	
Station	(N)	Generated in the controller
Subaddress	(A)	
Function	(F)	
Write	(W)	
Strobe 1	(S1)	
Strobe 2	(S2)	
Busy	(B)*	*B or I could be generated in the module if desired
Initialize	(Z)	
Inhibit	(I)*	
Clear	(C)	

All lines except L and N are bussed to all normal module stations. An individual L and N line connects each module to the control station.

Signals Z and I can be generated both under program control and manually. The inhibit signal can be generated either by program control or through a separate front-panel input.

Patch pins and free bus lines are available for making non-standard connections. Details of usage of these lines will not be discussed except to note that standard dataway signal standards must be followed.

The basic dataway operation will be described to briefly review the use of the various lines.

Dataway Operations

The Initialize (Z), Inhibit (I) and Clear (C) signals can be used in a variety of ways at the discretion of the designer or programmer. Initialize, which is used to set all registers to a predetermined state, has priority over other status signals such as Busy and Clear. The use of these lines will not be described further, except to note that each line normally carries a signal which originates in the crate controller, simultaneously to a receiver in each module attached to the dataway.

The Look-at-me (L) line similarly can be used in a variety of ways, and may or may not be a part of every dataway command operation. The basic function of L is to enable a module to request service from the controller. Thus an L signal originating in any module is sent along a single line to a receiver in the controller.

A dataway read operation proceeds as follows:

a. The addressed crate controller activates the A and F lines, together with the N line of a particular module. (For a read operation, the function code is F(16), F(8) = 0.) B is also activated.

b. On receipt of these signals, the addressed module puts its data on the dataway R lines, and in addition generates a response on the X and Q lines to indicate that the command is accepted and that data are present.

c. After the read lines are settled, S1 strobes the data into the controller.

d. A second strobe S2, if specified in the function code, removes the data in preparation for the next dataway cycle.

A write operation is similar to steps a) through d), except that write data is set up in the controller for transfer to an addressed module, and S1 strobes the data into that module.

The following facts are apparent:

a. R, X and Q signals can originate in as many as 23 separate modules (assuming 2 slots for the controller); therefore intrinsic OR outputs are required to combine these data sources into a common receiver in the controller.

b. The L signal from each module does not strictly have to be generated through an intrinsic OR, but it is specified as such in case it is desired to combine two or more L signals into a common load.

c. All other lines (N, A, F, W, Z, B, I, C, S1, S2) which originate in the controller simply drive multiple receivers in the modules and again technically do not have to be intrinsic OR outputs. However, the use of intrinsic OR's may lend additional flexibility and is specified.

d. All pullup terminations for any intrinsic OR circuits must be located in the crate controller, not in the module. In the case of the L lines, the pullup may be in a receiver other than the crate controller, for example a separate L-grader.

Dataway Voltage and Current Standards

In general, dataway signal standards are designed to be compatible with TTL (transistor-transistor logic) and DTL (diode-transistor logic) integrated circuits. Inverted logic levels are specified (0 volts = logic 1, +V volts = logic 0). Since the zero or off state of an intrinsic OR corresponds to +V on the open collector, absent modules will always read zero. Further discussion will assume the above convention.

The dataway standard voltages and currents are given in Fig. 1.

The voltage graph is self-explanatory. In the table of current standards, c) provides a guide to calculation of pullup terminations. The supply voltage must of course be taken into account. Note that if W, A, F, S, B, Z, I or C signals can originate in a module other than the controller, additional current sink capability is necessary. This case is unusual and will not be discussed in detail.

For comparison, the characteristics of the Model 7401 TTL quad 2-input NAND[1] (open collector output) are given in Fig. 2. The circuit is shown in Fig. 3. The voltage and current specifications for the 7401 are essentially compatible with the dataway standards. The maximum reverse current of the open collector is specified at 250 μA at +5.5 volts, compared with the dataway specification of 100 μA at +3.5 volts. This current consists of collector leakage current I_{CO}, in addition to any turn-on current generated under worst case input conditions, i.e., inputs at +0.6 volts, and temperature at the rated maximum. This point is discussed further in the next section.

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Driving R, X, Q, and L Lines

The R, X, Q, and L lines are driven from the module to single receivers in the crate controller or an L-grader unit. A typical circuit for an R, X, or Q line is shown in Fig. 4.

Note that in the logic 1 state, if for example, Vcc = 5 volts, Vo = 0.5 volts, and Ip = 9.6 mA, the pullup would be Rp = 470 Ω.

In the logic 0 state, the effect of the reverse currents of up to 23 outputs should be checked. According to the 7401 specification, each output could contribute 250 μA or .25 mA for a total contribution of 23×.25 = 5.74 mA. This would cause a drop of over 3 volts through an Rp of 470 Ω, assuming the reverse current remained constant with voltage. In this case, the circuit would be inoperable.

Fortunately, in practice the manufacturers' specification of 250 μA appears to be very conservative. In an actual measurement, the worst collector reverse current obtained on several samples (Signetics and Sprague 7401's) was just over 1 μA at the maximum specified Vcc of + 5.5 volts, + 0.6 volts on the inputs, and a temperature of 100°C. At 70°C the current was typically 0.2 μA, or about 10^3 times less than the quoted specification. Therefore, in practice, reverse currents should cause negligibly small voltage drops through Rp. A recommended procedure would be to test each module under worst case conditions and reject any IC's with unusually high reverse output currents.

Each L line can be handled similarly as in Fig. 5. In this case, leakage in the logic 0 state will be entirely negligible.

Driving W, A, F, Status and N Lines

All lines are again essentially identical in that one driver in the controller serves up to 23 module receivers. The pullup terminator remains in the controller as shown in Fig. 6.

In this case, the driver sink requirements in the logic 1 state for all except S and N lines are

$$I_{sink} = (1.6\ mA)(23) + Ip$$

where Ip is determined by the choice of pullup resistor.

The 7401 considered previously has a current sinking capability of only about 16 mA minimum; thus it is inadequate for this application. A unit with higher sinking capability, such as the Motorola MC858 Quad Power Gate which can sink up to 100 mA, is therefore required.

All controller-driven lines except the S and N lines have this same drive requirement. The N line, since it drives but a single receiver, could use a 7401 driver. The S lines require larger current sink capability (lower pullup resistors) in order to insure adequate speed of response, as well as to minimize pickup due to crosstalk from other dataway lines. Note that in every case, the pullup termination is located in the controller.

In the logic 0 state, leakage currents in the back-biased inputs will cause drops in Rp, analogous to the case of the read lines. The manufacturers' specification is typically about 40 μA maximum reverse input current. As in the case of the open collectors, the actual currents tend to be considerably less. Actual samples measured showed typical values of 2-3 μA at 70°C. Hence the total reverse current of up to 100 inputs should cause negligible voltage drops in Rp.

It should be noted that in practice, the number of driver outputs or receiver inputs is not restricted to one per module per line on the read or write lines respectively; therefore reverse currents should be given careful consideration in any design.

Dataway Timing Considerations

The speed of operation obtainable on the dataway is in general a function of:

a. Speed of the driver in both (+) and (-) directions.
b. Capacitance and inductance of the dataway lines.
c. Net capacitance of all loads attached to the dataway
d. Effects of crosstalk on the dataway lines.

The typical propagation delay of a 7401 is in the order of 10 to 20 ns. For open collector drivers, the actual speed in a system depends to some extent on the net capacitive load. The open collector drivers on the read lines present a capacitive load to whichever driver is using the line at that moment. Similarly, the paralleled inputs of many receivers capacitively load the write lines (or the B, A, F, Z, etc. lines). As discussed above, the equivalent resistive load of the back-biased inputs or outputs is usually negligible.

If capacitive loading of the lines were negligible, the maximum speed at which data could be read into a register in the controller would simply depend on the total delay through all gates involved, in addition to any fixed delays in the timing signals. For example, the S1 strobe must be delayed with respect to address and data signals in order to assure proper deskewing of read or write signals before storing the data. The CAMAC specification dictates tolerances both of delays and of transition times of the various signals on the dataway. The dataway timing cycle for an addressed operation is shown in Fig. 7.[2]

The following points should be noted in Fig. 7:

a. The N, F, A and B signals are allowed 150 ns after the first transition of any line (reference time t_0) to reach the 1 state.

b. The R, W, X and Q lines are allowed 400 ns from time t_0 to reach the 1 state.

c. The S1 signal must reach the 1 state no earlier than 400 ns, and no later than 500 ns, after t_0.

d. Strobe S1 must dwell at logical 1 for at least 100 ns.

e. Strobe S1 must return to the zero state no later than 700 ns after t_0.

f. Strobe S2, which initiates the removal of data, must reach logic 1 no earlier than 700 ns and no later than 800 ns after t_0.

g. Strobe S2 must dwell at logic 1 for at least 100 ns, and return to logic 0 no later than 1000 ns after t_0.

h. A new dataway timing cycle can begin no earlier than 1000 ns after t_0. Old data must be removed, and new data established, no later than 1400 ns after t_0, i.e., corresponding to the earliest allowable time for the next S1 strobe.

Clearly, the dataway timing cycle is specified in Fig. 7 to be completed in not less than 1 μs. The tolerances on delays and transitions are large compared with the typical propagation delays of 7401 gates mentioned earlier. Propagation delays along the dataway itself are of a similar order. For example, a measurement was made in which a Clear pulse was initiated at a crate controller input port, and the time taken for data from the most remote module to change at the controller output port was observed. The signal path included 7 levels of gating, plus the 2-way delay of the dataway; the total delay observed was 125 ns, or about 18 ns per gate, neglecting the effects of the dataway.

Assuming the dataway is designed to operate with the specified 1 μs cycle time, then, the two main constraints

are:

a. The total capacitive loading of R, X, or Q open-collector gates should not cause risetimes to be outside the tolerances given in Fig. 7; and

b. Signal transitions should not be so fast that cross-coupling along the dataway, particularly on strobe lines, becomes a problem.

Point a) is essentially a limitation imposed by the devices, namely gates; while b) is a function of the physical design of the dataway. The effects of a) can be estimated. Point b) will not be dealt with further, except to note that immunity from cross-coupling should be a very important consideration in crate design.

A discussion with one manufacturer[3] indicated that the typical "off" collector capacitance for the 7401 is 5-10 pF. An actual measurement, at +5.0 volts, yielded 5.5 pF. Thus we can estimate the low-to-high transition time, after turn-off of the active driver. Assume the following typical values:

Vcc	= 5.0 volts
$V_{threshold}$	= 2.0 volts
Von	= 0.4 volts
Rp	= 500 Ω
Co	= 10 pF (max)
N	= 24 (no. loads)

These values give a time-constant of 72 ns, and a time to the 2-volt threshold of 88 ns. The dataway operation should not be impaired with such a response. However, suppose there were 4 registers per module, each tied to the dataway. The transition from 0.4 to 2.0 volts would then take 352 ns, which is only slightly less than the 400 ns response allowed (t_9 to t_{12}) in Fig. 7. Thus, capacitive loading effects can indeed be significant, and should be considered carefully in module and system design.

Controller Drivers and Receivers

The crate controller must buffer the read and write lines from the dataway, and combine these into a single set of 24 line-pairs to interface with the Branch Highway outside the crate controller.[4] (The Branch Highway in turn interfaces up to 7 crates into a Branch Driver.) Also, the sorted or graded L (GL) signals must be combined onto the dataway R lines. This is shown functionally in Fig. 8. In Fig. 8, T_A and T_B are master timing and response signals originating in the Branch Driver and Crate Controller respectively. The function of these signals is to gate the RW lines of the addressed crate controller(s) onto the Branch Highway during a command operation.

The characteristics of dataway drivers and receivers have already been discussed. Note that in Fig. 8, actual implementation of the logic will require more circuits than shown, for several reasons. First, logic inversions are required on all lines if NOR's and NAND's (rather than OR's or AND's) are used. Second, the drive requirements of the Branch Highway are considerably heavier than those of the dataway, and different drivers are required. And third, the Branch Highway receivers should preferably have high impedance inputs to minimize Branch Driver current requirements.

Branch Highway Operations

A CAMAC system of up to 7 individual crates with crate controllers communicates with a computer through a Branch Highway leading into a Branch Driver. The Branch Driver is the source, as far as the crates are concerned, of a set of standard address and timing signals, as well as a set of 24 RW lines which are daisy-chained to all crates. A summary of the Branch Highway signals is as follows:

Name	Abbreviation	Line Pairs in Branch
Branch Demand	BD	1
Timing A	BTA	1
Timing B	BTB	7 (1 per crate)
Graded L Request	BG	1
Crate Address	BCR	7 (1 per crate)
Station Number	BN	5 (5 bits)
Subaddress	BA	4 (4 bits)
Function	BF	5 (5 bits)
Read-Write	BRW	24
Response	BQ	1
Initialize	BZ	1
Command Accepted	BX	1
Reserved	BV	7
Cable Screen	BSC	1

Signals originating in the crate (or crate controller) are Demand (BD), Response (BQ), Command Accepted (BX), and Read (BRW). All other signals originate in the Branch Driver (BDR).

The BD signal is used to call attention to the BDR that some crate or individual module in the system requires service. BG represents a request from the BDR back to the crate controller for Graded-L information. A single BDR line is selected at each crate controller so that each crate in contact with the Branch Driver has a unique single-line address. BN, BA and BF are binary-coded signals which after being processed in the crate controller become N, A and F respectively. BQ, BX and BZ are analogous to Q, X and Z already described. BRW of course becomes the combination of R and W in the crate dataway.

Two new timing signals are encountered in the Branch Highway, namely BTA and BTB. BTA is used to signal a particular crate controller that BCR, BN, BA, BF (and perhaps BRW) have been established on the Branch. BTB and BX are used to acknowledge that the particular command has been received and executed by the crate controller. Note that both BCR and BTB lines are selected so that each controller has both a unique crate address line and a unique response line back to the Branch Driver.

The timing of a Branch read operation is illustrated in Fig. 9.[5] The basic points of the operation are as follows:

a. The Branch Driver sets up BCR, N, A, F and then after a suitable delay generates the timing reference BTA.

b. At time t_0, which is the same t_0 referred to in Fig. 7, R, X and Q data are set up. It is assumed in Fig. 9 that N is used as a delayed strobe to gate R, X and Q onto their respective dataway lines.

c. At time t_3, S1 is generated, which initiates the acknowledge signal, BTB, to be sent back to Branch Driver.

d. On receipt of all BTB's in the Branch Driver BTA is terminated to acknowledge.

e. The removal of BTA is sensed back at the crate controller, which in response generates S2. S2 initiates removal of the read data from the dataway, and must itself be terminated by time t_9. At this time, BTB is removed, signifying back to the Branch Driver that the controller action is complete.

f. Removal of BTB is sensed at the Branch Driver and, after a delay, the original BCR, BN, BA, BF command data are removed to complete the cycle.

The main points of note in the above-described read operation are as follows:

a. In addition to the delays already described in the dataway cycle between t_0 and t_9 (Section 6), there are delays involved in the initial setup of command data in the Branch

Driver; in conditioning BTA in the module; in deskewing before reading and terminating BTA; in deskewing BTB's; and finally in clearing the command data.

b. The overall read operation, or any command operation, requires two complete round-trips of timing signals BTA and BTB on the branch; thus a delay of 4 t_d is incurred, where t_d is the one-way propagation delay of the line.

c. Signal sources attached to the BQ, BX, BRW, and BD must be coupled through intrinsic OR devices. It is generally good practice to implement all other lines in this manner unless there are strong reasons to the contrary.

d. The BTB response is opposite in polarity to all other signals. Thus all on-line crates must hold BTB in the 1 state (low) when not addressed, which enables detection of off-line and absent crates.

Other operations can proceed in a similar manner to the read cycle just described.

Branch Highway Voltage and Current Standards

The voltage and current standards for the branch, analogous to Fig. 1 for the dataway, are shown in Fig. 10.

From Fig. 10, it is evident that either discrete transistor or multiple IC drivers are necessary to provide the specified 133 mA current sinking capability. This large current capability arises because of the necessity to drive up to 8-1.6 mA inputs in parallel, plus one or two terminations which may be as low as 70 Ω each. In one system implemented at SLAC, two parallel MC858 DTL Power Gates[6] (open-collector) were used as a single driver to provide > 133 mA sink capability.

For receivers, up to 1.6 mA sink current is allowed per gate. However, since the minimum input (1) level is specified as 2.4 V, 7400 series gates cannot be used. In the Crate Controller Type A, an allowable input current of 0.3 mA is specified, which necessitates the use of a unit such as the SP380[2] quad 2-input NOR. This unit meets the minimum (1) input level of 2.4 volts.

Each of the signal lines in the dataway is specified to be a twisted pair, with a characteristic impedance of between 70 and 100 ohms. In practice, then, the actual current sinking requirements will depend upon the Z_0 of the line, and upon whether a termination is used at each end of the branch, or at just the BDR end. For optimum speed of operation, a termination is recommended at each end.

The maximum output voltage of the termination circuit is specified as 4.5 volts; or 4.1 volts preferred at a Z_0 of 100 Ω and a short circuit current of 50 mA. This implies an arrangement as shown in Fig. 11. If we assume a Vcc of 5.0 volts, a negligible receiver input current, and a Z_0 of 100 Ω, we calculate R1 = 122 Ω, R2 = 555 Ω. In this case the short-circuit current would be 41 mA per termination; thus all specifications are satisfied.

It appears that the primary reason for specifying a maximum output voltage of 4.5 volts, rather than Vcc, is to allow the use of a device such as the SP380, with its higher input Z and threshold voltage. This device has a base at the input which is not meant to operate close to Vcc; otherwise large input currents could result. If higher current devices such as 7400 series gates are used, there is no technical reason for not using a single pullup termination (R_1) connected to Vcc at each end of the Branch. However, the maximum levels specified should in general be maintained in order to assure compatibility with Type A controllers in possible future applications.

Conclusion

This report has described the voltage, current and some timing characteristics of CAMAC Dataway and Branch Highway signals.

It has been seen that some Dataway lines such as the read lines have drive requirements which can be met with standard 7401 TTL integrated circuits. In the case of other lines such as the write lines, a heavier current driver such as the DTL MC858 is necessary.

The Branch drive requirements demand > 133 mA current sinking capability, which can be met with either a discrete transistor driver, or two or more IC drivers in parallel. An example given was that of two parallel sections of an MC858. The Branch preferred input current requirement of 0.3 mA must be met with a discrete device, or a high impedance device such as the Utilogic SP380.

The Dataway timing specification, which essentially dictates a 1 μs minimum cycle time, is seen to incorporate delays which are liberal compared with typical TTL propagation delays. Additional delays inherent in the set up of commands in the Branch Driver, plus transmission delays in the Branch, will cause a typical Branch-Dataway operation to require somewhat longer than 1 μs.

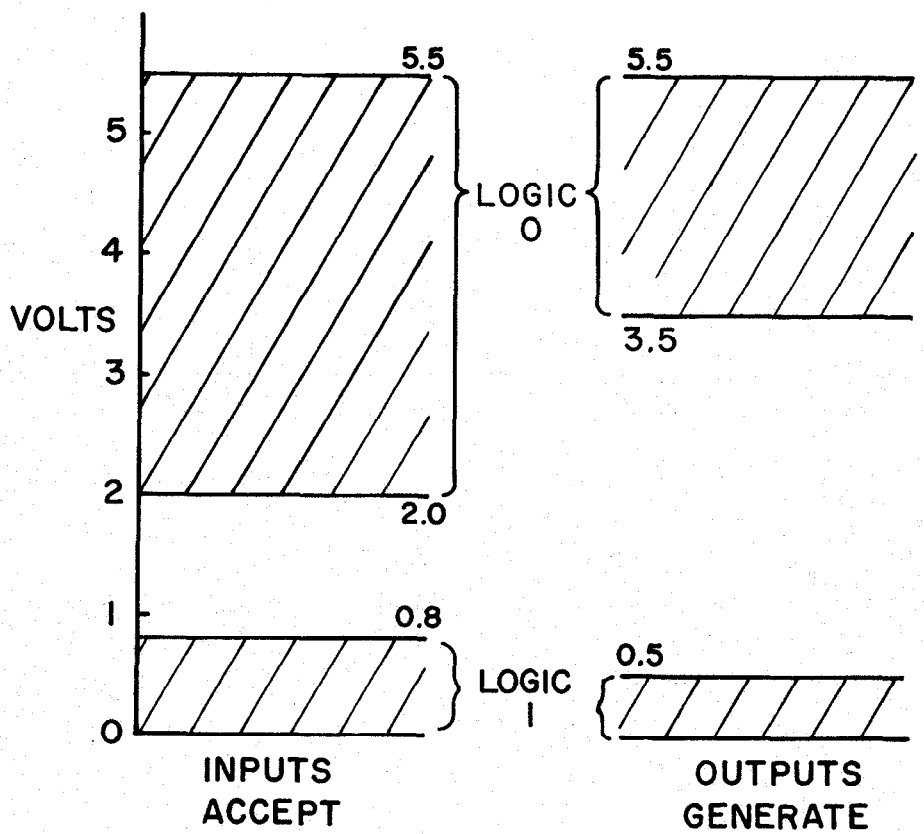
Reverse current loading is seen to be not a practical problem, although conservative IC specifications suggest testing of units where it appears that maximum rated reverse currents could cause trouble.

Capacitive loading of a large number of open collectors could be significant only if a very large number of loads are involved.

Extremely fast rising dataway signals (< 10 ns) could cause cross-coupling problems. Cross-coupling should be an important consideration of the physical design of the dataway.

References

1. Data are taken from Signetics data sheets.
2. Refer to EUR 4100e, p. 40, Fig. 9.
3. Signetics Corp., Sunnyvale, California.
4. See, "CAMAC Organization of Multicrate Systems," USAEC TID-25876, March 1972, Fig. 7, showing a CAMAC Crate Controller Type A.
5. Ibid, Fig. 3.
6. Motorola MDTL Series: I_{sink} = 60 mA/unit, all loaded simultaneously; 100 mA normally.
7. Signetics Corp., Utilogic Series.



VOLTAGE

A. RECEIVER INPUTS

I IN (MAX) at +0.5V = 1.6s mA FOR WAFSBZIC LINES;
11.2 mA FOR LQRX WITH PULLUP SOURCE;
1.6 mA EACH FOR LQRX WITHOUT PULLUP SOURCE;
3.2 mA EACH FOR N LINES;

ILKG (MAX) at 3.5V = 100 (25-s) μA ALL EXCEPT S1, S2 } UNITS WITH PULLUP SOURCE
= 9.9 mA FOR S1, S2 }

= 100s μA ALL EXCEPT N } UNITS WITHOUT PULLUP SOURCE
= 200 μA FOR N }

B. TRANSMITTER OUTPUTS

I SINK (MIN) at +0.5V = 16 mA FOR LQRX LINES
= 6.4 mA FOR N LINES
= (25-s) 1.6 mA FOR WAFSBZIC LINES

ILKG (MAX) at +3.5V = 100s μA

C. PULLUP CURRENT

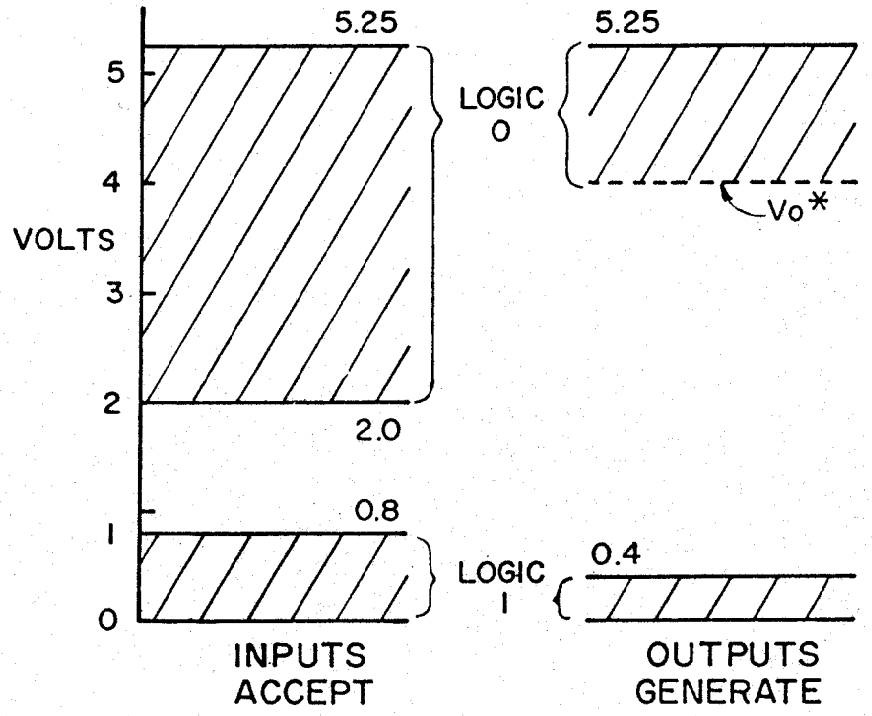
Ip at +0.5V
$6 \leq Ip \leq 9.6$ mA ALL EXCEPT S1, S2
$38 \leq Ip \leq 58$ mA FOR S1, S2

Ip at +3.5V
$2.5 \leq Ip$ mA ALL EXCEPT S1, S2
$10 \leq Ip$ mA FOR S1, S2

CURRENT

1754A1

FIG. 1



A. INPUTS

I IN (MAX) at 0.4V = −1.6mA

B. OUTPUTS

I SINK (MIN) at 0.4V = 16mA

I LKG (MAX) at 5.5V = 250μA

VOLTAGE

CURRENT

* NOTE-Vo DEPENDS ON REVERSE COLLECTOR CURRENT(S) AND PULL-UP Rp

1754A2

Fig. 2

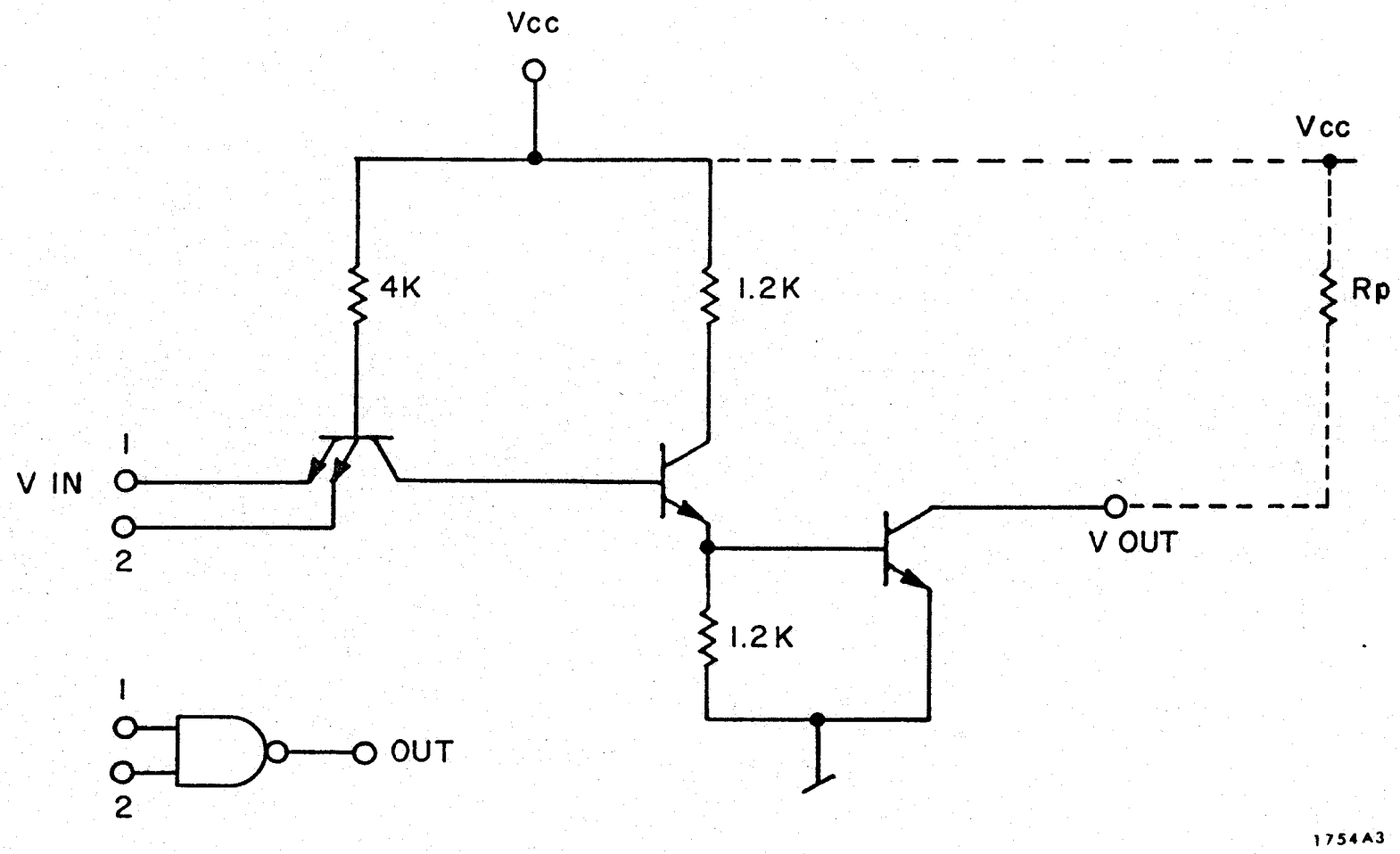


Fig. 3

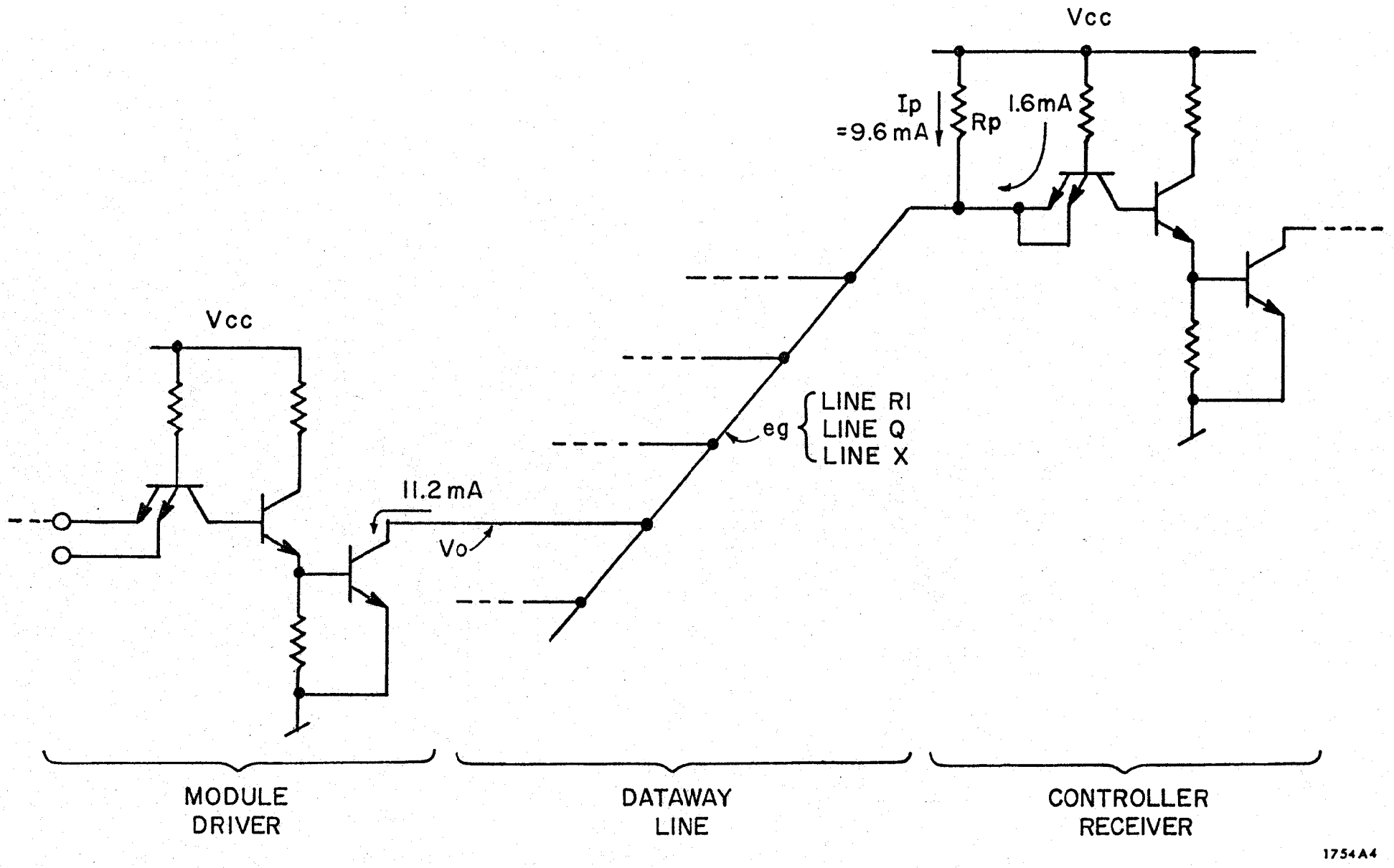

Vcc
Ip
=9.6 mA
Rp
1.6mA
Vcc
eg
LINE RI
LINE Q
LINE X
11.2 mA
Vo
MODULE
DRIVER
DATAWAY
LINE
CONTROLLER
RECEIVER
1754A4

FIG. 4

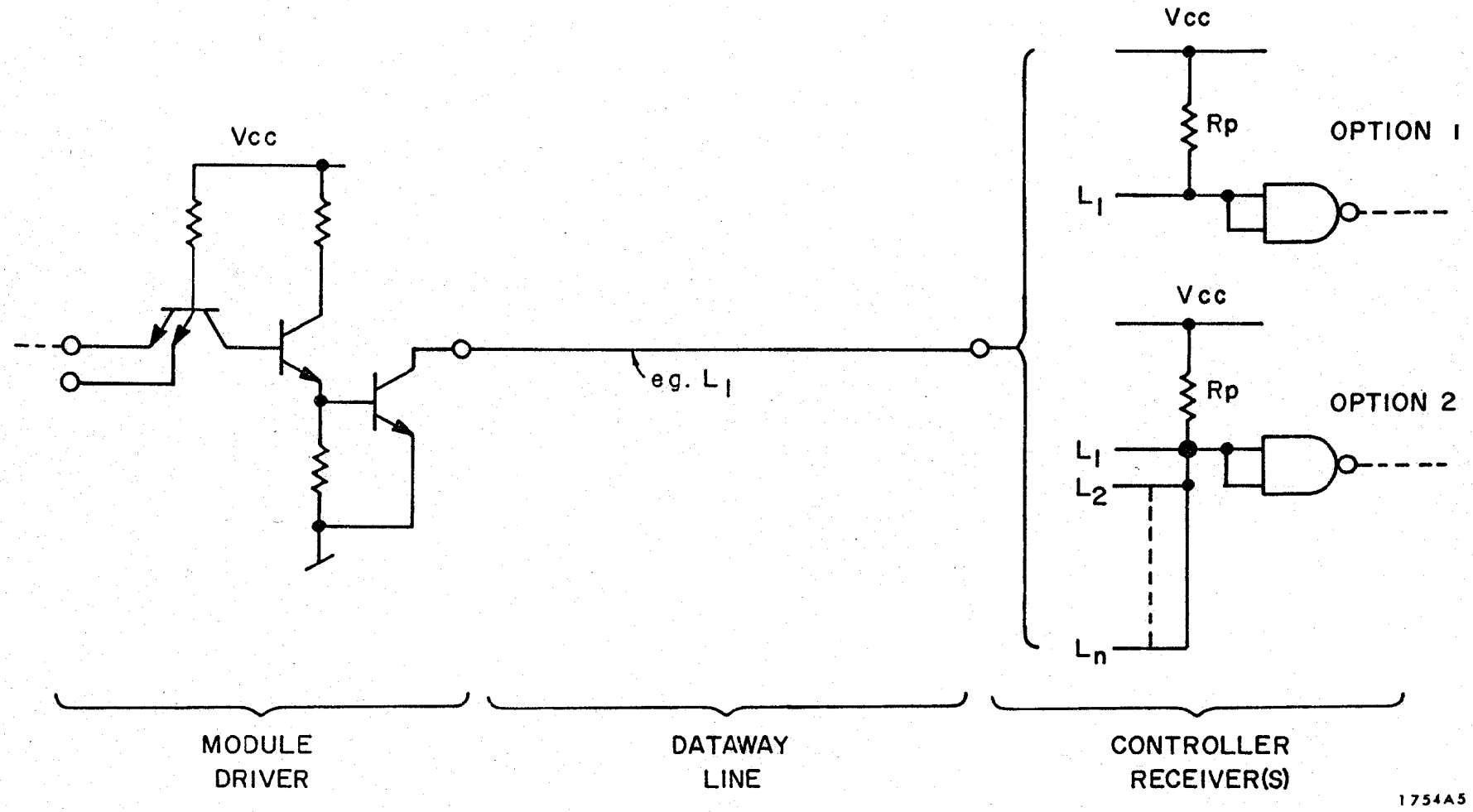

Vcc
Vcc
Rp
OPTION 1
L_1
Vcc
Rp
OPTION 2
L_1
L_2
L_n
eg. L_1
MODULE
DRIVER
DATAWAY
LINE
CONTROLLER
RECEIVER(S)
1754A5

Fig. 5

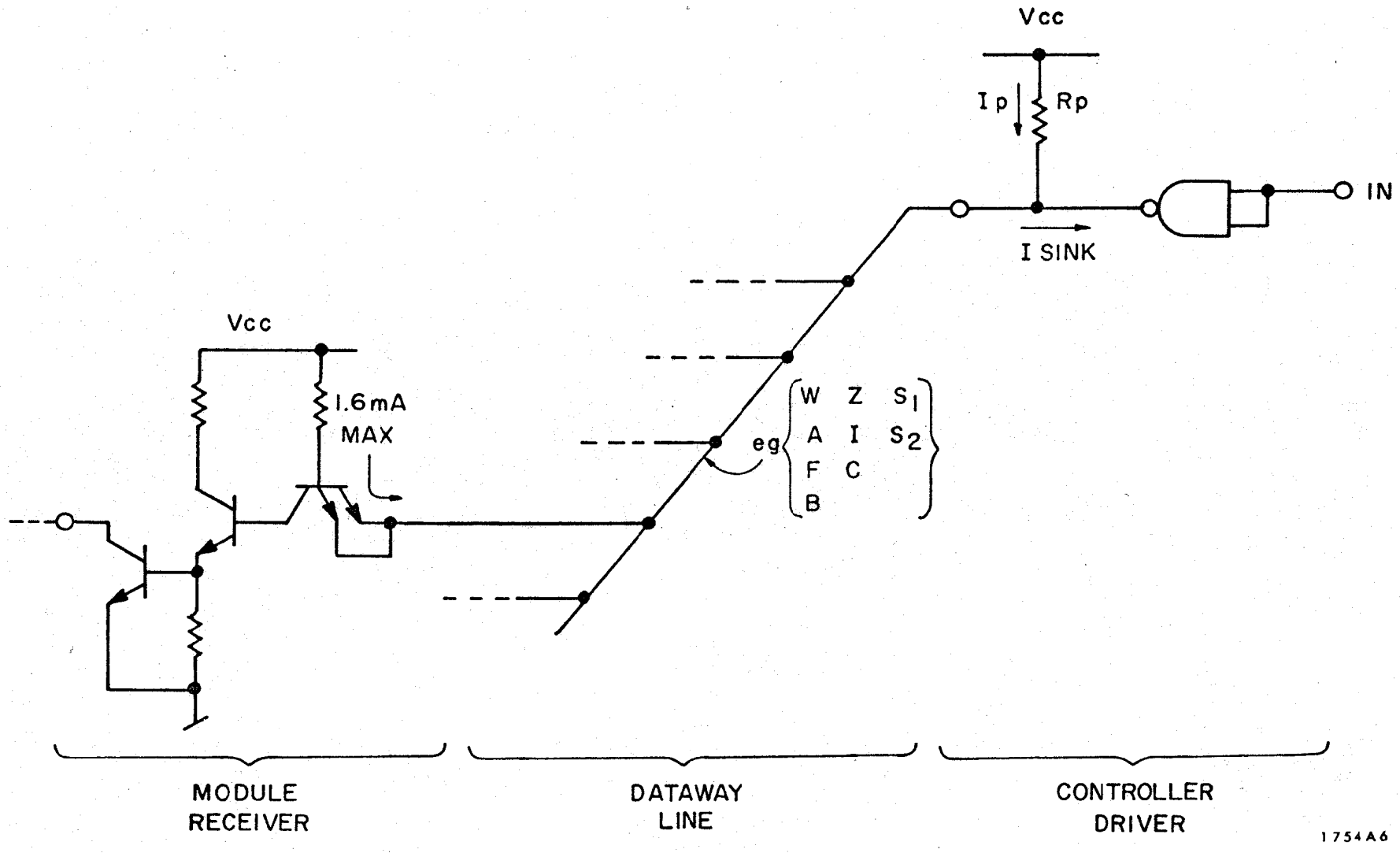
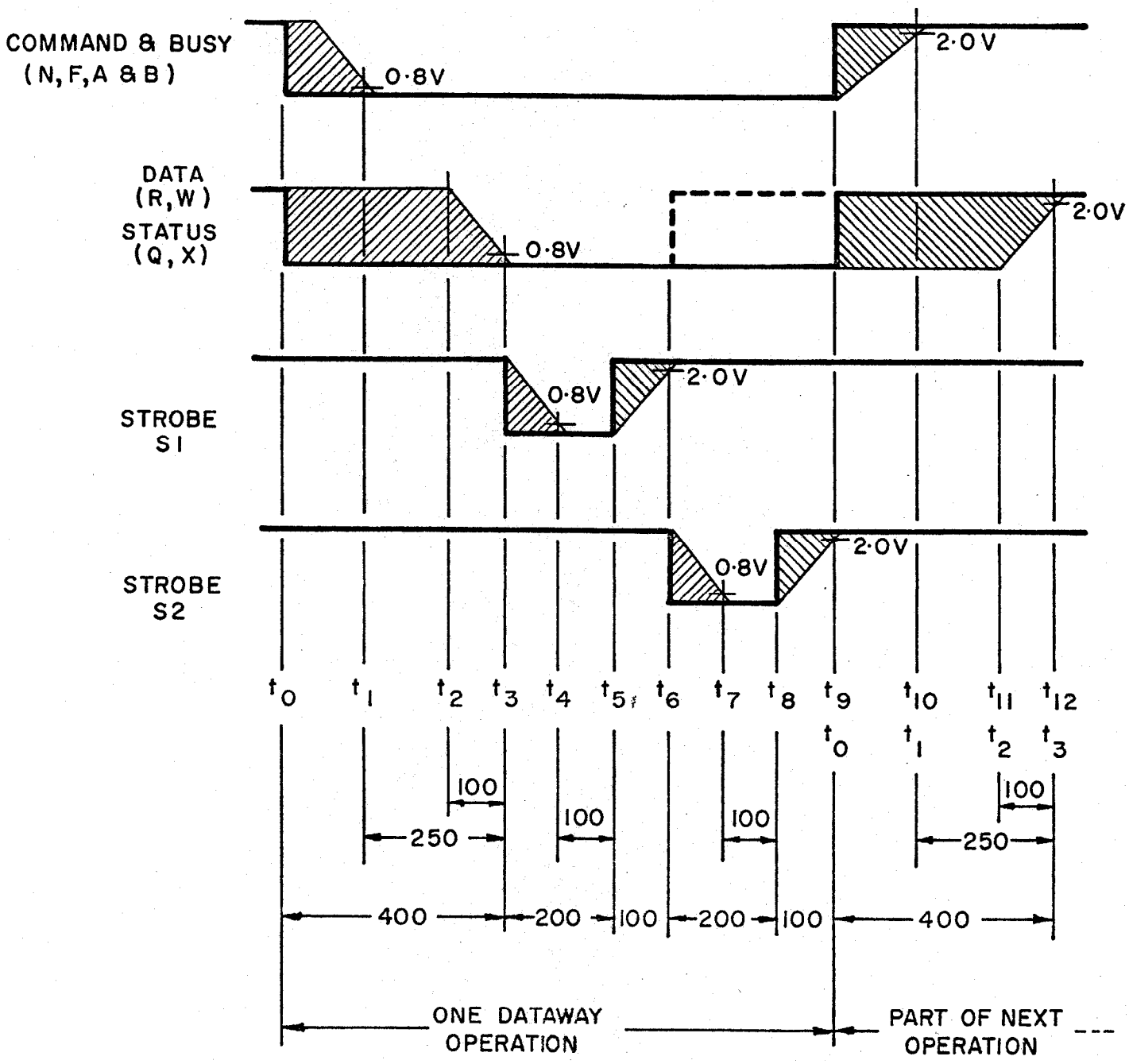

Vcc
Ip
Rp
IN
I SINK
Vcc
1.6mA
MAX
eg
W Z S1
A I S2
F C
B
MODULE
RECEIVER
DATAWAY
LINE
CONTROLLER
DRIVER
1754A6

Fig. 6

DATAWAY TIMING



TIMES GIVEN ARE MINIMUM VALUES IN NANOSECONDS

NOTE: L-TIMING (NOT SHOWN) IS $(\overline{R,W})$ OR $(\overline{Q,X})$

1754A7

FIG. 7

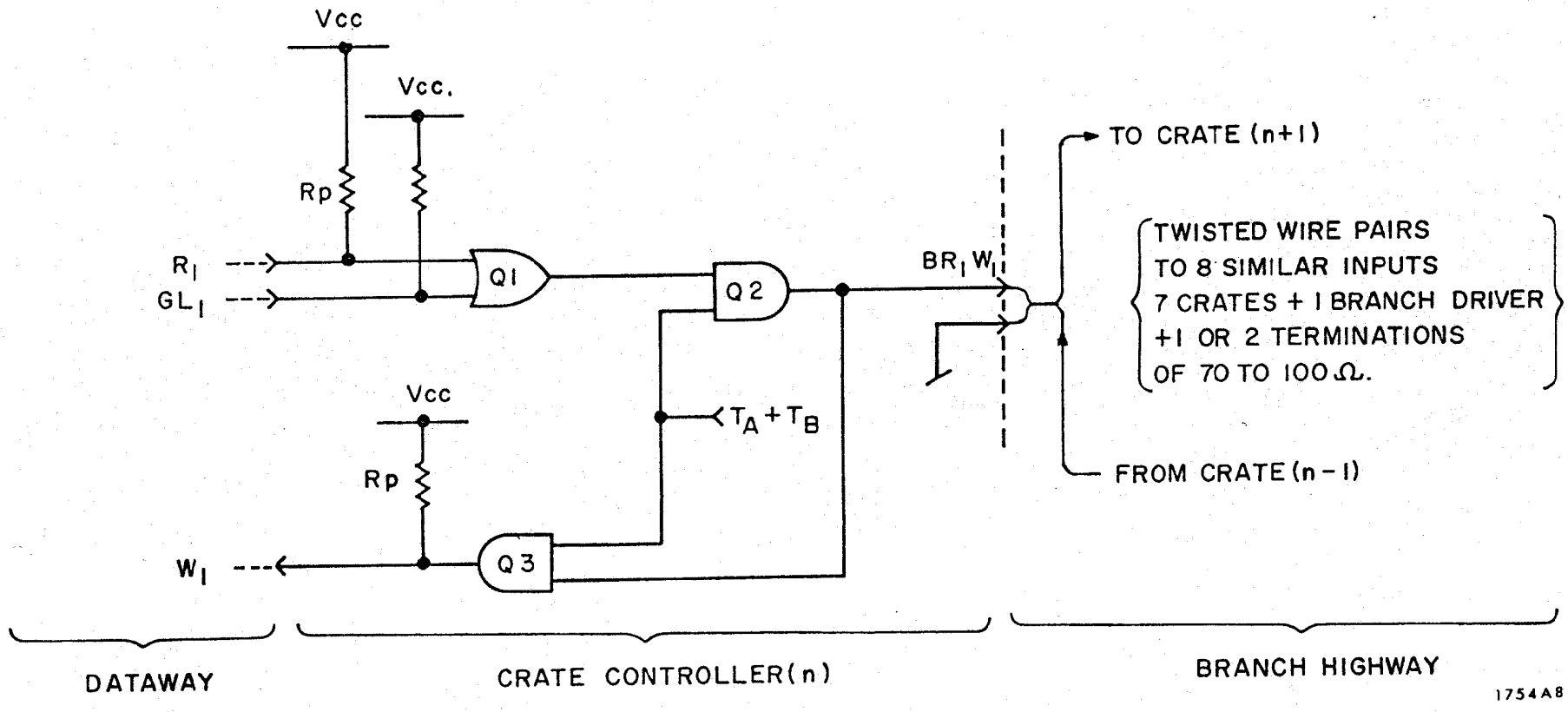

Vcc
Vcc.
Rp
R_1
GL_1
Q1
Q2
BR_1 W_1
TO CRATE (n+1)
TWISTED WIRE PAIRS
TO 8 SIMILAR INPUTS
7 CRATES + 1 BRANCH DRIVER
+1 OR 2 TERMINATIONS
OF 70 TO 100 Ω.
Vcc
$T_A + T_B$
Rp
W_1
Q3
FROM CRATE (n-1)
DATAWAY
CRATE CONTROLLER(n)
BRANCH HIGHWAY
1754A8

Fig. 8

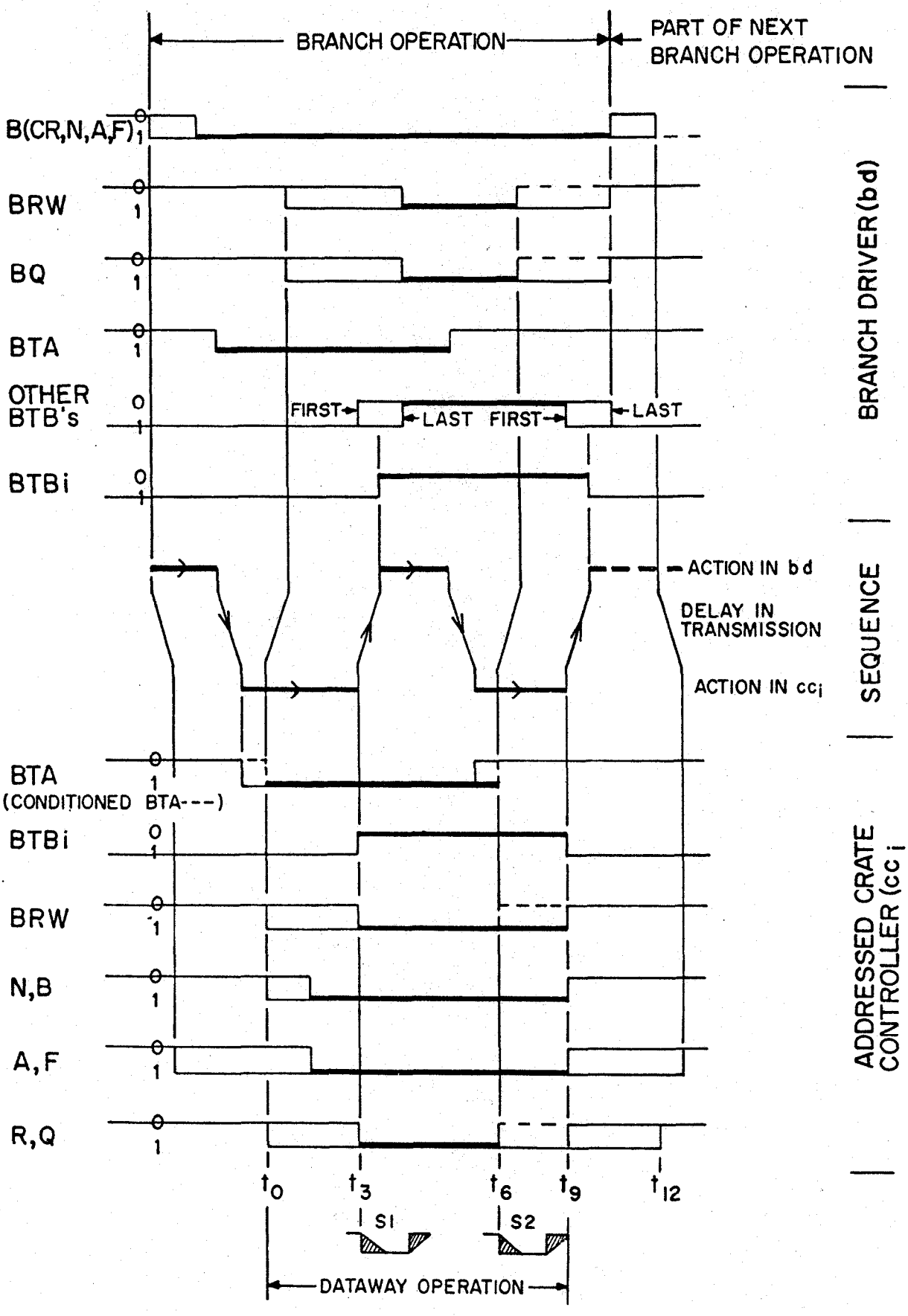
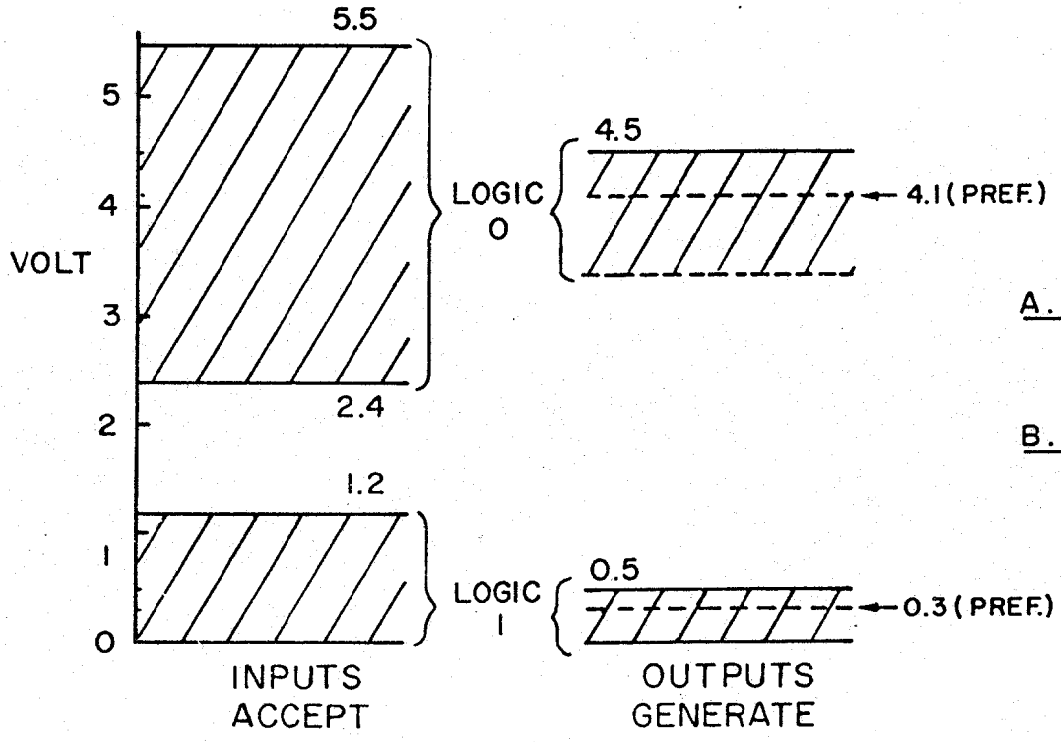

BRANCH OPERATION
PART OF NEXT BRANCH OPERATION
B(CR,N,A,F)
BRW
BQ
BTA
OTHER BTB's
FIRST
LAST
FIRST
LAST
BTBi
BRANCH DRIVER (bd)
ACTION IN bd
DELAY IN TRANSMISSION
ACTION IN cci
SEQUENCE
BTA (CONDITIONED BTA---)
BTBi
BRW
N,B
A,F
R,Q
ADDRESSED CRATE CONTROLLER (cci)
t0
t3
t6
t9
t12
S1
S2
DATAWAY OPERATION
1754A9

Fig. 9



A. RECEIVER INPUTS

I IN (MAX) at 0.5V = −1.6mA
(0.3mA PREFERRED)

B. TRANSMITTER OUTPUTS

I SINK (MIN.) at 0.5V = 127 mA
(133mA PREFERRED)

CURRENT

Fig. 10

1754A10

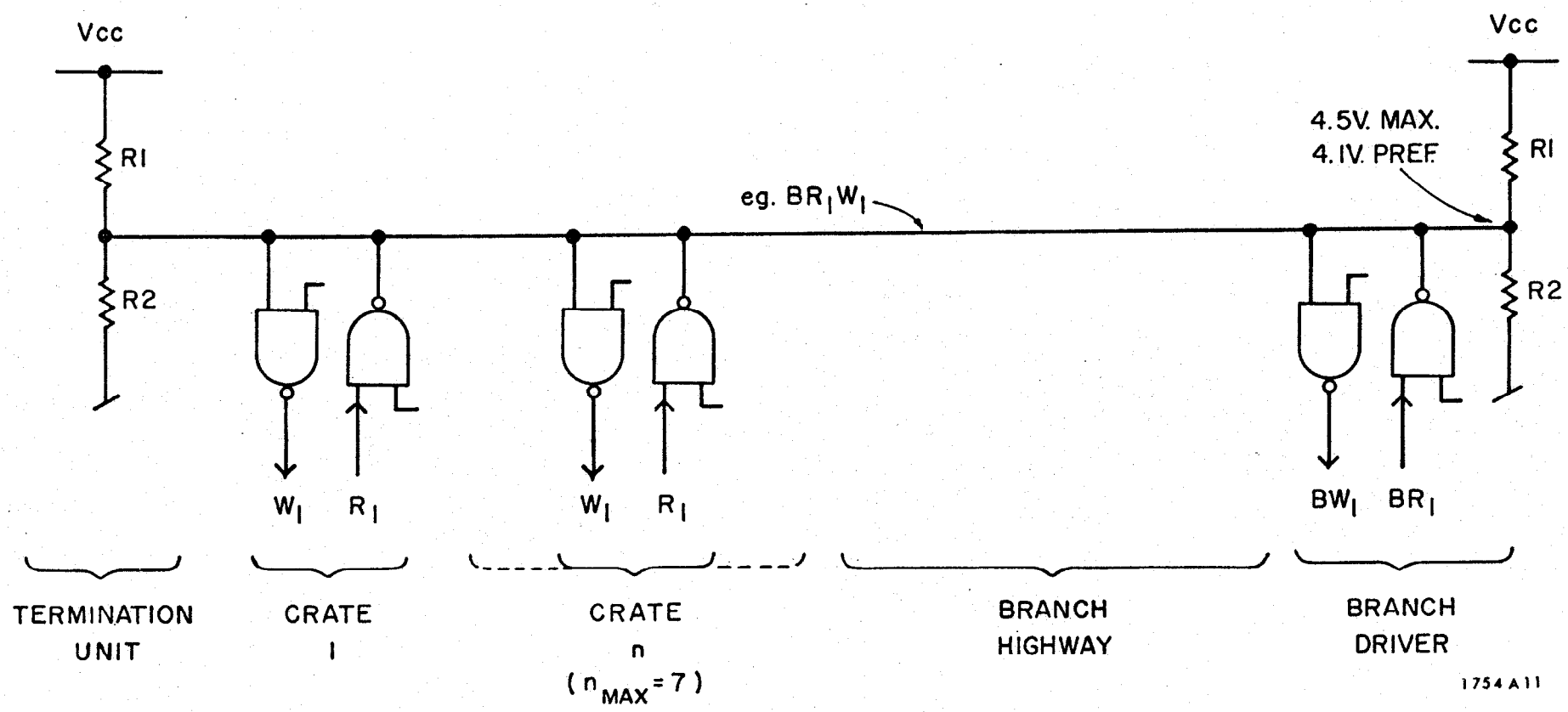

Vcc
RI
R2
W1
R1
W1
R1
eg. BR1W1
4.5V. MAX.
4.1V. PREF.
Vcc
RI
R2
BW1
BR1
TERMINATION UNIT
CRATE 1
CRATE n (nMAX = 7)
BRANCH HIGHWAY
BRANCH DRIVER
1754 A11

Fig. 11