SLAC-PUB-191
May 1966

CHARACTERISTICS OF SMALL COMPUTER SYSTEMS FOR ON-LINE APPLICATIONS*

Richard M. Brown

Stanford Linear Accelerator Center, Stanford, California

ABSTRACT

A summary of the characteristics of 31 domestic computers relevant to on-line applications is presented. Some of the problems specific to on-line use are discussed and the alternatives available in different models are described. For the survey, a small computer is taken as any which might be dedicated to on-line operation, excluding time-sharing systems.

(Presented at Argonne National Laboratory, AEC-ANL Conference, Use of Computers in Analysis of Experimental Data on Control of Nuclear Facilities, May 4-6, 1966)

* Work supported by U. S. Atomic Energy Commission.

CHARACTERISTICS OF SMALL COMPUTER SYSTEMS FOR ON-LINE APPLICATIONS*

Richard M. Brown

Stanford Linear Accelerator Center, Stanford, California

At the Karlsruhe conference in 1964 Levin[1] surveyed small computer systems for on-line use, covering 19 domestic models. For this paper, two years later, Edward Mueller and I have included 31 computers of which only nine overlap Levin's set and most of these have incorporated added features which reflect desirable special characteristics and/or software. This is a measure of the problems facing the experimentalist trying to select an on-line computer from a broad and rapidly changing spectrum of models.

For this survey, the meaning of the term "small computer" has been extended from Levin's price limit of $150,000 to cover any computer that might be dedicated to a small number of on-line operations, excluding the concept of the centralized time-sharing computer. Practically, this results in an upper limit of the order of $600,000 to $1,000,000 although many of the new large time-sharing models would make excellent data acquisition computers if the importance of the installation justified it.

Since Levin's paper summarized many of the features of computers desirable for on-line use, we shall discuss only additional requirements and features that experience with on-line data systems has revealed. Specifically covered are the techniques for interrupt execution, the problems of the response times of computers to interrupts, the difficulties in interfacing the experimental

* Work supported by U. S. Atomic Energy Commission.

and computer hardware, and costs and capabilities in acquiring programming flexibility to meet changing experimental configurations.

INTERRUPT IMPLEMENTATION

The explicit interrupt mechanisms are critical for on-line operation since they provide asynchronous control of the interaction between the computer and the external environment. The principal differences between computer models lie in the extent to which the components of the interrupt process are implemented in hardware as opposed to software. Two specific elements of this are: the mechanism by which conflicts between simultaneous interrupt requests are resolved, and secondly the techniques for identifying the particular interrupt of the allowed set.

The simplest system funnels all external interrupt requests through a single process with appropriate software procedures for subsequent identification and scheduling. This technique has the advantage of flexibility, particularly with regard to dynamic establishment of priorities for interrupt execution. On the other hand programmed control of interrupts expends a substantial overhead in memory space and time. At the other end of the spectrum are the completely hardware-realized systems wherein each external device has a separate interruption input which uniquely identifies the source and by means of hardware priority chains establishes the order in which interrupt request conflicts shall be resolved. Some manufacturers offer as many interrupt channels as there are memory cells. An upper limit of 16-32 interrupt levels is more reasonable and is set by the inability of the computer to process effectively more than that number of interrupt components. In

actual practice it is extremely difficult to allocate more than three or four significant programs with fixed execution deadlines within a priority scheme and to guarantee satisfactory performance. As a result, in most multiple priority programs only a very limited set of the programs are assigned to the highest priority levels and the remainder of the interrupts are allocated with non-critical ordering. The ability to disable individual or grouped interrupts is available in many models and provides greater flexibility in organizing a priority interrupt scheme.

The addition of single instruction interrupts, that is, those which permit the execution of only one instruction before resumption of the interrupted program, represents a trend toward special interrupt categories to incorporate special functions hitherto accomplished by external apparatus. In particular where operating speeds permit, many scaling and counting operations can be inexpensively absorbed into the computer program. As the speeds of on-line computers increase, the interface between the computer processor and the experimental equipment will move closer to the basic data sensors to give improved flexibility at much lower cost.

INTERRUPT RESPONSE TIME

In many experimental configurations the time before the computer can usefully service an interrupt request can be critical, for example where data is transient or where there is a periodic requirement for servicing. If the minimum response time requirements are not met, additional buffering equipment must often be added between the computer and the experimental equipment. Furthermore, in systems driven by more than one interrupt operating under an

execution deadline, the response times as well as execution times are additive in a worse case analysis and can seriously interfere with desired performance. In this survey, the following components to the response time were assessed:

1) The longest non-interruptible instruction or instruction sequence that might conceivably delay response to an interrupt,
2) The actual execution time of the transfer of control out of the interrupted program, and
3) The time to save all hardware states of the machine necessary for subsequent program restoration.

Two response times are given: the first includes the first two components mentioned which constitute a minimum worst case value; the second adds in the estimated state preservation time. The latter can sometimes be reduced if only a fraction of the machine registers will be perturbed.

The delay time awaiting completion of a non-interruptible instruction dominates the first response time and can exceed the figures quoted if the programs include interrupt-disabled states of long duration or under execution of a very long indefinite address chain. Also some models have optional special instructions for extended precision arithmetic or multiple operations which create non-interruptible times in the hundreds of microseconds. On the other hand by avoiding the use of the longer instructions the worst case and average response times can be minimized.

The total response times in the models surveyed ranged from 14 to 140 microseconds. The models with the faster responses generally enabled interruption within instruction execution and also had special provision for rapid machine state preservation.

EXPERIMENT-COMPUTER INTERFACE

Since a sine qua non for on-line data acquisition is tight coupling between the computer and the experimental apparatus, the varieties of such connections available on any model are of considerable importance. Most computers surveyed offer at some cost one or more standard buffered channels capable of transferring information between device and computer independently of program execution. There is, of course, a hidden interaction between the channel operation and program execution in that access to a common memory is time-shared. Some models also use the equipment of the central processing unit to control the data transmission at actual communication time, thus unobtrusively delaying program execution for several cycles on each transmission. In assessing a computer model, required data rates should be carefully estimated and the resultant slow-down on central processor execution rates calculated.

A more serious problem exists with systems having multiple priority interrupt programs sharing a limited number of conventional buffered channels for communication to peripheral devices. This channel sharing overturns carefully laid out priority schemes, since rarely can the channel be interrupted and subsequently resumed. To alleviate this, some of the computers have interlaced multiplexed channels capable of concurrently servicing a number of external devices. This is a considerably less expensive mechanism for removing the channel bottleneck without multiplying the number of channels. Since the peripheral devices in this case compete for the multiplex channel on a unit transmission basis, these are useful primarily for slower data rate devices.

Another real problem with the experimental apparatus arises in the fact that the experimenter often constructs a considerable amount of the apparatus himself and must interface it electrically and logically with the computer hardware. Although all computer manufacturers sell digital cards for use in such purposes, only five do so as a commercial product with proper documentation and assistance toward the design process itself. Needless to say, no computer circuits from different manufacturers can be directly connected to one another. It is a significant advantage to be able to connect a computer to apparatus constructed with the manufacturer's own compatible digital building blocks.

PROGRAMMING FLEXIBILITY

Many of the current on-line data acquisition systems have been constructed by experimenters themselves writing in assembly language. For the smaller computers the techniques and aids for programming have been rather primitive. Unfortunately, while a 4000 word memory computer is a small computer, a 4000 word program written in machine language is a large program and tedious to construct and modify. This constitutes one of the most serious handicaps in the development of small computer on-line systems.

To overcome this, several approaches are available. First of all, programs for some of the smaller computers can be assembled on larger models so that all of the power of a modern assembler can be applied to off-line assembly of the data acquisition programs. This includes the use of MACROS or generalized procedures and the availability of magnetic tape and line printer equipment for easy program editing and listing. Unfortunately

remote assembly on computers of different manufacturers is not available, although modern assembler construction techniques make it feasible.

Many installations are also turning to Fortran and in the future possibly PL/I to speed up program construction and modification. As yet there is no suitable high-order language adequate for many of the detailed control and I/O functions that must be programmed into a data acquisition and analysis system. Whether the richness of PL/I will permit complete program construction in this language is as yet undetermined. The cost in overhead of such higher order languages is often seriously underestimated. We have attempted to assess the number of memory cells required to support a simple Fortran subroutine containing formatted I/O. The resulting overhead for memory space varied from 1500 to 7000 words of memory. This included not only the basic I/O driver routines, but also all Fortran library routines brought in to interconnect the user program and the system resident. Although a considerable fraction of the higher figure of 7000 words was wasted in terms of subroutine packages unused in simple I/O operations, it is clear that considerable costs are incurred in the use of high-order languages and that honest estimates of these costs should be included in any computer selection.

Another important programming feature concerns the ease of constructing re-entrant procedures or subroutines. Such procedures may be interrupted during execution and re-entered without destroying volatile information from the previous call, such as the return address link or temporary results. Since the alternative involves either expensive duplication of subroutines or the disabling of interrupts during subroutine execution, most on-line

computer systems meet the re-entrancy requirements either with software or by special instructions and hardware. In some computers of older design this can be quite awkward, as noted in the survey.

The characteristics chart presented here summarizes the returns from a questionnaire sent to all known domestic computer manufacturers. The replies were checked with the computer reference manuals when appropriate. However, the entries should be viewed as tentative, particularly with regard to software where it was difficult to separate promises from realizations. Many of the features cited are standard or special options obtainable with increased cost and delivery time. It is impossible to tabulate meaningful price figures for the individual computers, since there is no standard configuration available for all. For example, one manufacturer includes a disc file as standard equipment on one model and quotes only on that basis.

It is hoped that this survey will be useful to experimentalists contemplating the acquisition of a data gathering system. Since there is no reliable metric of computer power and since tests with benchmark problems are generally infeasible because of the unique I/O connections of any installation, the selection process must necessarily be an iterative one involving increasing detail of system layout and programming specific to the installation and computer model under consideration. The characteristics summary can help in the early restriction of attention to a small set of appropriate computers.

References

1. Levin, Jules S., "General Survey: A Review of Characteristics of Available Small Computer Systems with regard to their On-Line Applications," Proc. EANDC Conf. on Automatic Acquisition and Reduction of Nuclear Data, Karlsruhe, July 1964, p. 418-423. See also Nucleonics 22, No. 10, December 1964.

APPENDIX I

Explanatory Notes

A. Manufacturers: ASI - Advanced Scientific Instruments; CCC - Computer Control Co.; CDC - Control Data Corp.; DEC - Digital Equipment Corp.; EAI - Electronic Associates Inc.; GE - General Electric; IBM - International Business Machines; ITI - Information Technology Inc.; RAYTH - Raytheon; SEL - Systems Engineering Labs; SDS - Scientific Data Systems.

B. Word Size: The normal length in bits for arithmetic operations is given. For byte-oriented machines a normal fixed point length is given.

C. Memory Size: <Minimum> / <Maximum> - <cycle time in μs>.

D. Add Time: Fixed point addition from core memory to accumulator except Floating point only.

E. Index Registers: Number allowed, Hardware or Memory implemented.

F. Indirect Addressing: Maximum number of indirect levels addressable or Indefinite.

G. Relocation Register: Either a fixed base added on all memory accesses or a memory paging scheme.

H. Multiply/Divide: Hardware or Software.

I. Floating Point Arithmetic: Hardware or Software.

J. Multiple Precision Arithmetic: Hardware or Software.

K. Interrupt Response Time (μsec): First value is sum of longest non-interruptible instruction and interrupt execution times; second is first value plus time to save all hardware states of machine in memory. Indefinite indirect addressing not included.

L. External Interrupts: Number of separate external interrupt triggering signals allowed.

M. Interrupt Selection Scheme: Hardware if control transfers directly to program unique to interrupting trigger, else Software.

N. Interrupt Priority Levels: Number of levels of hardware-controlled priority interrupt.

O. Interrupt Enable/Disable: Individual enabling of each interrupt source; Group enabling of sets of interrupts; All interrupts enable/disabled only.

P. Single Instruction Interrupt: Execution of a single instruction with automatic program resumption.

Q. Compilers Available: Algol, Fortran, Real-time Fortran (re-entrant procedures).

R. Fortran Support Package: Total memory space required for system and library subroutines to support subroutine linkage and formatted I/O.

S. Re-entrant Procedures: Hardware if machine instructions to save subrouting return links and temporary storage in pushdown list; Software if return links placed in index registers or other preserved hardware; Awkward if return links placed in fixed memory cells requiring special procedures to ensure re-entrancy.

U. Buffered I/O Channels: Maximum number of I/O channels that operate in parallel with the central processing unit but capable of handling transmission to only one peripheral device at a time.

V. Interlaced Multiplexed I/O Channels: First value is maximum number of I/O channels each capable of concurrently transmitting to several peripheral devices; second value is the maximum number of devices (subchannels) connectable to any such channel.

W. External State Sensing: Maximum number of external states or devices whose binary value can be individually determined under program control.

X. Parallel Work I/O Instruction: Capability for direct input/output of individual external data words under program control.

Y. Logic Modules: Compatible digital circuit cards offered as a commercial product (not as maintenance or replacement items).

Z. Peripheral Equipments: Standard options: Disc or Drum mass memory units; Cathode ray displays; Incremental tape units; Links to other computers. All manufacturers offer conventional magnetic tape transports.

ON-LINE COMPUTER CHARACTERISTICS

April 1966

A Mfg.	Model	B Word Size	C Memory	D Add Time	E Index Regs.	F Indirect Addr.	G Reloc. Reg.	H Multiply/ Divide	I Floating Point	J Mult. Prec.	K Interrupt Response Time	L External Ntrpts.	M Ntrpt. Selection	N Ntrpt. Priority Levels	O Ntrpt. Enable/ Disable	P Single Instr. Ntrpt.	Q Compilers Available	R Fortran Support Pkg.	S Re-Entrant Procedures	T Macro Assmblr.	U Buffered I/O Channels	V Interlaced Multiplexed I/O	W External State Sensing	X Parallel Word I/O Instr.	Y Logic Mod.	Z Peripherals
ASI	6020	24	4/32K-1.9μ	3.8	3M	I	No	H	S	S	51.3/81.7	64	H	32	I,G	Yes	F,R	2000	A	Yes	8	1-16	Yes	Yes	No	D,C,I,L
ASI	6040	24	4/32K-1.9μ	3.8	3H	I	No	H	S	S	51.3/81.7	64	H	32	I,G	Yes	F,R	2000	A	Yes	8	1-16	Yes	Yes	No	D,C,I,L
ASI	6050	24	4/32K-1.9μ	3.8	3H	I	No	H	H	H	51.3/81.7	64	H	32	I,G	Yes	F,R	1760	A	Yes	8	1-16	Yes	Yes	No	D,C,I,L
ASI	6070	24	4/32K-1.9μ	3.8	3H	I	No	H	H	H	51.3/81.7	64	H	32	I,G	Yes	F,R	1760	A	Yes	8	1-16	Yes	Yes	No	D,C,I,L
ASI	6130	16	8-32K/.9μ	1.8	3H	I	No	H	S	H	7.2/14.4	128	H	128	I,G	No	F,R	---	A	Yes	6	1-16	Yes	Yes	No	D,C,I,L
CCC	DDP-116	16	4-32K/1.7μ	3.4	1M	I	No	H(opt)	S	S	23/38.3	256	H	16	I	No	F	---	A	No	8	0	Yes(opt)	No	Yes	D,C,L
CCC	DDP-124	24	8-32K/1.75μ	3.5	(1 or 3)H	I	No	H	S	S	25.5/36	96	H	16	I	No	F	---	A	No	4	0	Yes	Yes	Yes	D,C,L
CCC	DDP-224	24	4-65K/1.9μ	3.8	3H	I	No	H	H(opt)	S	28.8/53.5	128	H	16	I	Yes	F	---	A	No	4	0	Yes	Yes	Yes	D,C,L
CDC	3100	24	4-32K/1.75μ	3.5	3H	I	No	H	H(opt)	H(opt)	10.5/17.5	68	S	0	I	No	F,R	3000	A	Yes	4	4-64	Yes(opt)	Yes	No	D,C,L
CDC	3300	24	8-262K/1.25μ	2.5	3H	I	Yes	H	H(opt)	H(opt)	7.5/20.0	72	S	0	I	No	F,R	3000	A	Yes	8	8-64	Yes(opt)	Yes	No	D,C,L
CDC	1700	16	4-32K/1.1μ	2.2	1H & 1M	I	No	H	S	S	20.2/29.0	16	H	16	I	Yes	R	3000	A	Yes	2	2-64	Yes	Yes	No	D,C,L
DEC	PDP-7	18	4-32K/1.75μ	3.5	8M	1	No	H(opt)	S	S	17/34.5	1000	H	16	A	Yes	F	4000	A	No	4	0	Yes	Yes	Yes	C,L
DEC	PDP-8	12	4-32K/1.5μ	3.0	8M	1	No	H(opt)	S	S	48.5/71	64	S	1	A	No	F	2500	A	Yes	7	0	Yes	Yes	Yes	C,L
EAI	8400	32	8-65K/2.0μ	5.3(F)	7H	I	Yes(opt)	H	H	H	25/45	256	H	272	I,G	Yes	F,R	3700	A	Yes	8	0	Yes	Yes	No	D,C,I,L
GE	4020	24	2-32K/1.6μ	3.2	7M	O	No	H	S	S	34/58	128	H	128	G	Yes	F,R	6000	H	No	16	1-28	Yes	Yes	No	D,C,L
GE	4040	24	2-16K/5.0μ	16.0	7M	O	No	S	S	S	89/140	1024	H	128	G	Yes	F,R	6000	H	No	16	0	Yes	Yes	No	D,C,L
GE	4050-II	24	4-64K/3.2μ	6.4	7M	1	No	H	H(opt)	H	64/112	1024	H	128	G	Yes	F,R	6000	H	No	16	1-28	Yes	Yes	No	D,C,L
GE	4060	24	4-64K/1.6μ	3.2	7M	1	No	H	H(opt)	H	47/71	1024	H	128	G	Yes	F,R	6000	H	No	16	1-28	Yes	Yes	No	D,C,L
IBM	1800	16	4-32K/2.0μ	4.5	3H	1	No	H	S	S	48.5/92.8	384	H	24	I,G	No	F,R	2500	S	No	9	0	No	Yes	No	D,L
IBM	360/44	32	8-65K/1.0μ	2.25/4.75	16(H or M)	O	Yes	H	H(opt)	H	42/82	8192	H	32	I,G	No	F	---	S	Yes	1	3-64	No	No	No	D,C,L
ITI	4900	18	2.5-100K/1.75μ	4.0	10M	1	No	H	H	H	104/153	1000	S	1000	I	Yes	None	None	S	Yes(H)	1000	0	Yes	Yes	No	C,D,I,L
RAYTH	520	24	4-32K/1.0μ	3.0	7H	O	No	H	S	S	16/31	4	H	4	I,G	Yes	F,R	2000	S	Yes	4	0	Yes	Yes	Yes	D,C,L
SDS	9300	24	4-32K/1.75μ	3.5	3H	I	No	H	H	H	22.8/49	992	H	1021	I	Yes	F,A,R	7000	A	Yes	8	1-128	Yes	Yes	Yes	D,C,L
SDS	930	24	4-32K/1.75μ	3.5	1H	I	No	H	S	S	21/47.3	896	H	947	I	Yes	F,A,R	5500	A	Yes	8	1-128	Yes	Yes	Yes	D,C,L
SDS	925	24	4-16K/1.75μ	3.5	1H	I	No	H(partial)	S	S	36.8/63	896	H	910	I	Yes	F,A,R	5500	A	Yes	8	1-128	Yes	Yes	Yes	D,C,L
SDS	92	12	4-32K/1.75μ	3.5	1H	I	No	H	S	S	17.5/43.8	256	H	261	I	Yes	F	---	A	No	1	1-128	Yes	Yes	Yes	D,C,L
SDS	SIGMA-7	32	4-128K/1.2μ	2.4	(7-112)H	1	Yes	H	H	H	25/31	224	H	240	I	Yes	F,R,PLI	8000	H	Yes	8	1-32	Yes	Yes	Yes	D,C,L
SEL	810	16	4-32K/1.75μ	3.5	1H	I	No	H(opt)	S	S	22.8/29.8	3840	H	96	I	Yes	F	2000	A	No	8	0	Yes	Yes	Yes	D,C,I,L
SEL	840	24	4-32K/1.75μ	3.5	3H	I	No	H(opt)	H(opt)	H(opt)	29.8/40.3	2400	H	60	I	Yes	F,R	2000	A	No	8	0	Yes	Yes	Yes	D,C,I,L
UNIVAC	418-I	18	4-65K/4μ	8	8H	1	No	H	H	H	57.2/137.2	2048	H	4	A	Yes	F	4000	A	Yes	16	16-64	No	No	No	D,C,I,L
UNIVAC	418-II	18	4-65K/2μ	4	8H	1	No	H	H	H	28.6/68.6	2048	H	4	A	Yes	F	4000	A	Yes	16	16-64	No	No	No	D,C,I,L

522-C