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A 50 Nanosecond Printed Circuit Linear Gate Using Transistors*

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ABSTRACT

A fifty nanosecond linear gate with primary use in high energy physics experiments is described. The gate has a pedestal of less than 0.1% of the maximum output pulse height and a feedthrough of less than 0.2% over a pulse height range of 100 to 1. Design considerations, construction details, and performance are discussed.

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1. INTRODUCTION

Precision pulse height analysis of scintillation counter outputs in high energy physics experiments at the 1.5 GeV Electron Synchrotron at the California Institute of Technology prompted the development of the gate described here. Since its first use in 1961,[1] it has been utilized at the Enrico Fermi Institute for Nuclear Studies at the University of Chicago,[2] and recently at the Lawrence Radiation Laboratory at the University of California.[3]

Block and schematic diagrams of the circuit are shown in Figs. 1 and 2 respectively. After being inverted by T1, the attenuated input signal enters the emitters of the gating transistors T3 and T4. The gating pulses applied to the bases steer the signal current introduced at the common emitters either to the output via T4 or to ground via T3. The pedestal resulting from the standing current in T3 is canceled by mixing a fraction of one of the gating pulses with the gated signal at the output. The signal from T4 proceeds to the outputs via the output inverter T7. In the "External" position of the gating switch, the gate input pulse is applied to the gate generator T5 and T6, producing two symmetrical gating pulses controlling T3 and T4. When the gating switch is in its "On" position, the gate is permanently open; in its "Off" position the gate is always closed.

The circuit operates on negative input pulses. Input impedances are 125 ohms, and the three identical outputs are each intended to drive a 125 ohm resistive load. Ten percent monitors of the signal input, the gate input, and the output are provided on the front panel.

2. DESCRIPTION OF THE CIRCUIT

The input signal first enters an attenuator, consisting of 125 Ω T networks inserted in 11 steps of 2 dB each. The output of the attenuator is applied to the base of transistor T1, which acts as an inverter and limiter. Its collector is a nearly ideal current source for driving the gating transistors T3 and T4. Since the standing current in T1 is critical in canceling the pedestal, the 56 μF capacitor in its emitter circuit is recovered at high counting rates by T2. In order to aid the cancellation of temperature drifts, T1 and T2 are identical transistors with matched betas and similar collector currents. The 6.3 mA standing current in T2 sets an upper limit on the average input signal voltage, corresponding to a 10% duty rate of -5 volt pulses. With this limitation the circuit is effectively DC coupled up to the collector of T4.

Whether the signal from the input inverter is or is not passed by the gating transistors is determined by D1, D2, D3, and D4, which are controlled by the gate shaper T5 and T6 (see below). When D1 and D4 are conducting, T3 conducts and T4 is cut off by approximately 0.5 volts.[4] Thus, any change in the collector current of T1 originating from an input signal will pass into the emitter of T3 and thence to AC ground on its collector, unless the voltage on the emitter of T4 becomes large enough to turn it on. In order to reduce such feedthrough effects, a transistor with a low base spreading resistance (≈10Ω) was chosen for T3. When D2 and D3 are forward biased, T4 conducts and T3 is cut off. The input signal current from the collector of T1 is passed into the emitter of T4 and emerges at its collector. This signal is inverted by T7, which has an output impedance of less than 10Ω and produces an

output voltage proportional to the collector current of T4. This voltage is applied to the output loads via three emitter followers T8, T9, and T10.

The gate shaper consists of transistors T5 and T6, which shape the gate input pulse into a pair of gating pulses, one positive and one negative. This part of the circuit is DC coupled, to allow the use of long gates and the possibility of simulating gating pulses by the gating switch. When the potential on the base of T5 is near ground, T6 carries the 23 mA standing current, T5 is cut off, and D1 and D4 are conducting. When the potential on the base of T5 is between -2 and -3 volts, T5 conducts, T6 is cut off, and diodes D2 and D3 are turned on.

With the gating switch in the "Ext." position, the gate input is connected to the base of T5. In order to achieve fast operation, a minimum gate input pulse of about -2.5V is required. However, since the collector of T5 rises to -3.1V, the pulse has to be no more negative than -3V in order to prevent saturation.

3. CONSTRUCTION

Initially the circuit was built on a copper plate.[5] Later, as experience was gained in the construction of a printed circuit modular instrumentation system, compatible printed circuit construction was employed for the gate. The board has a size of 4.5 in. by 8 in. by 0.064 in. with a copper clad of 1 oz/in.^{2} Twelve of these, or similar, units plug into a 5.25 in. by 19 in. card file.

Signal as well as power leads connect through a rear printed circuit connector. The gating switch and the three monitor coaxial connectors are fastened to a 1.35 in. by 4.75 in. photoengraved front panel. The

input attenuator thumbwheel switch, which is mounted on the printed circuit board, is accessible from the front. A gate constructed at the Fermi Institute is shown in Fig. 3.[6]

4. LINEARITY, FEEDTHROUGH, AND PEDESTAL

The linearity, feedthrough, and pedestal of the circuit were measured with the setup shown in Fig. 4. These measurements used a 10 nsec wide rectangular signal input pulse with a rise time of less than 1 nsec. A fast univibrator[7] provided a 50 nsec wide gate input pulse with 12 nsec rise time and -3 volts height (Fig. 5). The output pulse of the gate circuit was shaped to a 50 nsec wide critically damped pulse by a passive pulse shaper network, used with most subsequent circuits. This shaper, when terminated by 125 Ω, has an output pulse height of approximately $\frac{1}{5}$ of that of a 10 nsec wide input pulse (See Appendix). The same pulse shaper was used to calibrate the input amplitude for the linearity and feedthrough measurements. For the low level feedthrough measurements an auxiliary transistor distributed amplifier with an amplification of 10 and a rise time of 3 nsec was inserted.[8]

The linearity and feedthrough properties of the gate are shown in Fig. 6. The straight line section of the "On" output as function of the input can be approximated as $V_{out} \approx (kV_{in})^{1-\epsilon}$ where $\epsilon < 3\%$ and $k = 1 \pm 5\%$. A typical pulse produced by the circuit at the output of the shaper is shown in Fig. 7.

The gate pedestal at the output of the shaper with no signal input is shown in Fig. 8. It consists mainly of a transient with a peak value of less than 15 mV, stable over long times to approximately ±5 mV. The shaped

gate output pulse height as function of the input delay, depicted in Fig. 9, shows a substantial timing margin for 50 nsec wide gate input pulses.

The output rise time without the pulse shaper (Fig. 10) is essentially a constant 4 nsec up to pulse heights of -2V and increases to approximately 10 nsec at -5V.

5. PERFORMANCE

Performance data are available on the use of the gate in a 28 counter telescope for detecting K^+ mesons produced by photons from the Cal-Tech 1.5 GeV Synchrotron. Particles are allowed to stop in a stack of 15 plastic scintillation counters. Amplitude discrimination and logical operations are performed on 10 pulse heights. If all criteria are satisfied, the output signals of 18 counters are passed by 18 gates and simultaneously pulse height analyzed into 100 channels each.[9] Input rates to the gates are typically 300 kc/sec, and the output rates are in the vicinity of 1kc/sec.

During a year of operation there were no failures in the 18 gate circuits. Linearity and stability, including the pulse height analyzer but excluding the photomultiplier tubes, were measured with a mercury pulser. The linearity and the stability during five days were better than ±1 channel, corresponding to ±3 millivolts at the output of the shaper.

ACKNOWLEDGEMENTS

The suggestions and comments of Dr. Alvin V. Tollestrup have been very valuable.

The cooperation of Mr. L. Nesleny and of Ransom Research in the preparation of the printed circuit board is gratefully acknowledged.

APPENDIX

50 Nanosecond Pulse Shaper

For a delta function input of charge Q from a 125Ω source, the response of the shaper (Fig. 11) into a 125Ω load can be written as:

$$i_{out} = \frac{Q}{2\tau} \frac{t}{\tau} \exp(-t/\tau)$$

With τ = 20 nsec, the 10% to 90% rise time is 11.2 nsec (= 0.56τ), the full width at half maximum is 48 nsec (= 2.4τ), and the time of the peak is 20 nsec (= τ).

FOOTNOTES

1. A. Barna and J.H. Marshall, "A 50 Nanosecond Linear Gate Circuit Using Transistors", Report CTSL-18, California Institute of Technology, Pasadena, California (February 1961).
2. A. Barna and D.F. Torzewski, "Modular Instrumentation Handbook", Report EFINS-63-83, The University of Chicago.
3. M. Brown, "Instrumentation of a High Energy Cyclotron Experiment", Nuclear Instruments and Methods 23, 109-116 (1963).
4. For small pedestal transients, small voltage swings on the bases of T3 and T4 are desired to reduce capacitive currents which produce an output transient when the gate turns on.
5. A. Barna and J.H. Marshall, op. cit.
6. The cooperation of Mr. D.F. Torzewski is gratefully acknowledged.
7. A. Barna, J.H. Marshall and M. Sands, "A Multifold Coincidence-Veto Circuit Using Transistors", Nuclear Instruments and Methods 12, 43-59 (1961).
8. A. Barna and J.H. Marshall, "A Distributed Amplifier Using Transistors", Report CTSL-27, California Institute of Technology, Pasadena, California (April 1961).
9. D.E. Groom and J.H. Marshall, "A 25-Input Pulse-Height Recording System", Review of Scientific Instruments 33, 1249-1255 (November 1962).

FIGURE CAPTIONS

Fig. 1. Block diagram.

Fig. 2. Schematic diagram. Shaded and filled symbols denote normally conducting semiconductors. Resistors are $\frac{1}{2}$W, 1% unless otherwise noted. Not shown are 0.05 μF ceramic disk capacitors by-passing polarized electrolytic and tantalytic capacitors. Power supply decoupling and bypass components are omitted. C1 and C2 (typically 0 to 100 pF) are adjusted for optimum pedestal transient. Circled letters refer to rear connector pins.

Fig. 3. Three views of a gate constructed at the Fermi Institute.

Fig. 4. Test setup.

Fig. 5. Gate input pulse generated by fast univibrator. Tektronix 541 oscilloscope with Type L preamp. Vertical: 2V/major division. Horizontal: 20 nsec/major division. Oscilloscope rise time: 12 nsec.

Fig. 6. Linearity and feedthrough.

Fig. 7. Shaped output of the gate for a -0.5 volt, 10 nsec signal input in coincidence with the gate input of Fig. 6. Vertical: 50 mV per major division. Horizontal: 20 nsec per major division.

Fig. 8. Gate Pedestal with no signal input as seen at the output of the pulse shaper. Vertical: 10 mV per major division. Horizontal: 20 nsec per major division.

Fig. 9. Output pulse height vs input delay.

Fig. 10. Output rise time vs pulse height.

Fig. 11. 50 nsec pulse shaper.

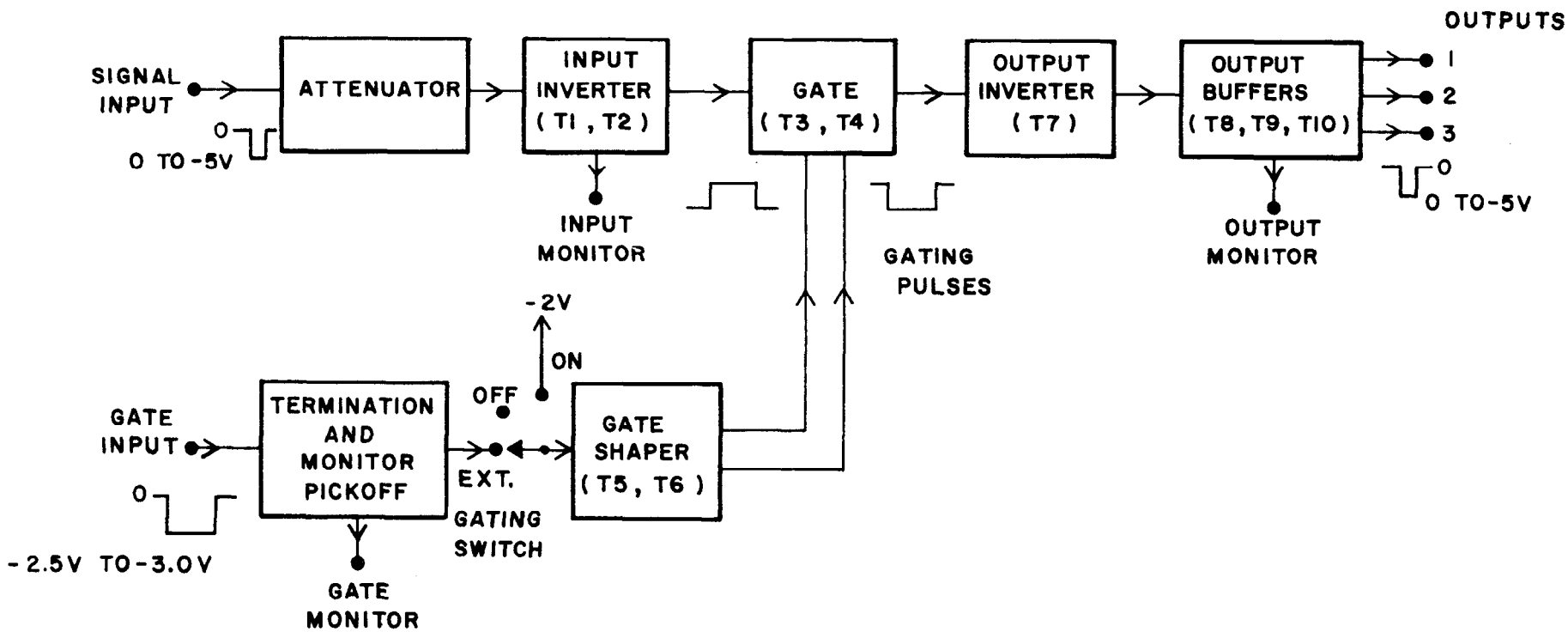
SIGNAL INPUT
0
0 TO -5V
ATTENUATOR
INPUT INVERTER (T1 , T2)
INPUT MONITOR
GATE (T3 , T4)
GATING PULSES
OUTPUT INVERTER (T7)
OUTPUT BUFFERS (T8, T9, T10)
OUTPUT MONITOR
OUTPUTS
1
2
3
0
0 TO -5V
-2V
ON
OFF
GATE INPUT
0
-2.5V TO -3.0V
TERMINATION AND MONITOR PICKOFF
GATE MONITOR
EXT.
GATING SWITCH
GATE SHAPER (T5 , T6)

FIG. 1

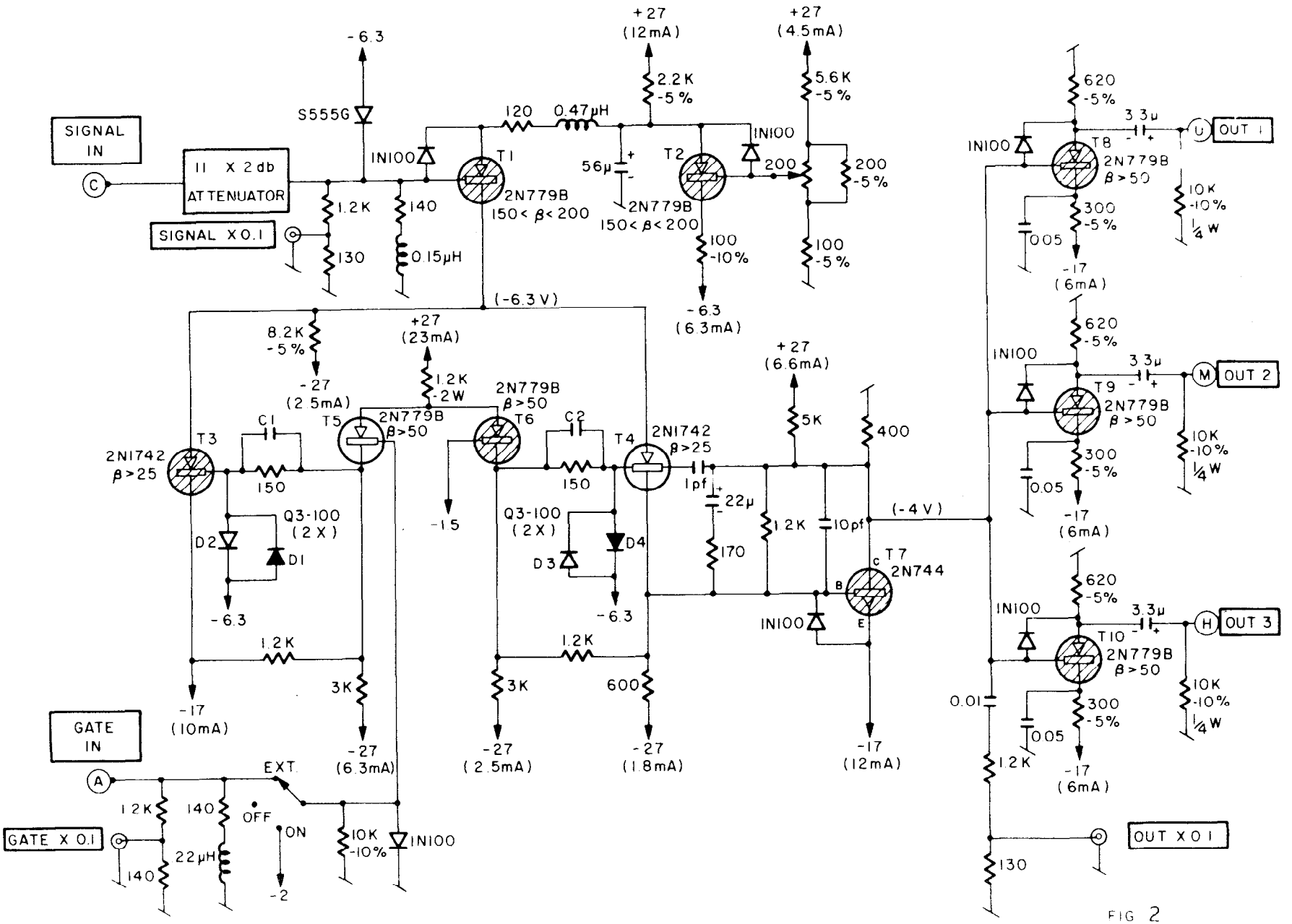
SIGNAL IN
C
11 X 2db ATTENUATOR
SIGNAL X0.1
-6.3
S555G
1.2K
130
140
0.15μH
IN100
T1
2N779B
150< β< 200
120
0.47μH
+27 (12mA)
2.2K -5%
56μ
T2
2N779B
150< β< 200
+27 (4.5mA)
5.6K -5%
IN100
200
200 -5%
100 -10%
100 -5%
-6.3 (6.3mA)
(-6.3 V)
8.2K -5%
-27 (2.5mA)
+27 (23mA)
1.2K -2W
T5
2N779B β>50
T6
2N779B β>50
C1
C2
T3
2N1742 β>25
T4
2N1742 β>25
150
150
-15
+27 (6.6mA)
5K
400
1pf
22μ
1.2K
10pf
170
(-4 V)
Q3-100 (2X)
D2
D1
-6.3
Q3-100 (2X)
D3
D4
-6.3
T7
2N744
C
B
E
IN100
1.2K
3K
-17 (10mA)
1.2K
3K
600
-27 (2.5mA)
-27 (1.8mA)
-17 (12mA)
GATE IN
A
EXT.
OFF
ON
-2
1.2K
140
22μH
140
GATE X 0.1
10K -10%
IN100
620 -5%
IN100
T8
2N779B β>50
3.3μ
U
OUT 1
10K -10% 1/4 W
300 -5%
.005
-17 (6mA)
620 -5%
IN100
T9
2N779B β>50
3.3μ
M
OUT 2
10K -10% 1/4 W
300 -5%
.05
-17 (6mA)
620 -5%
IN100
T10
2N779B β>50
3.3μ
H
OUT 3
10K -10% 1/4 W
300 -5%
.005
-17 (6mA)
0.01
1.2K
130
OUT X 0.1

FIG 2

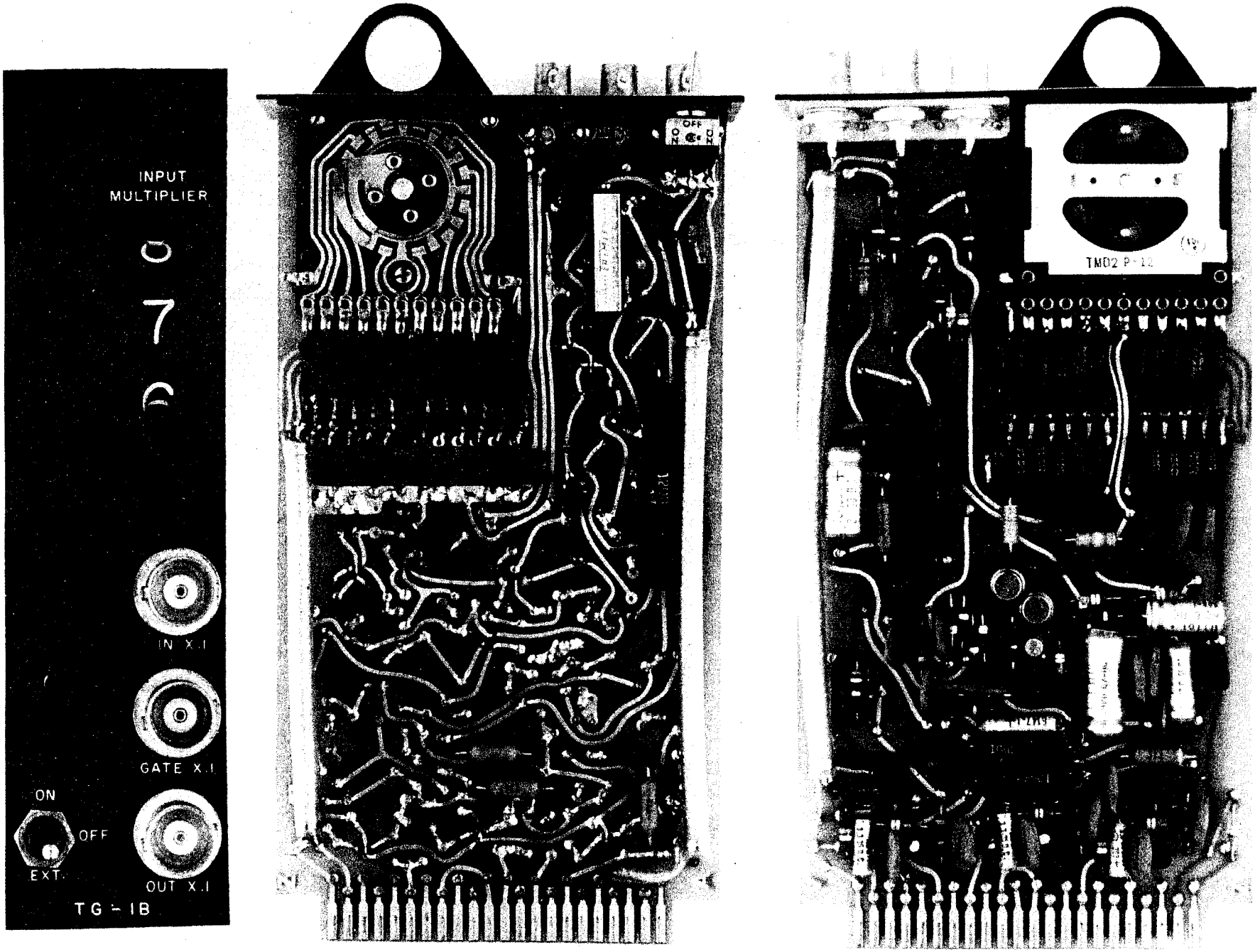

Fig. 3

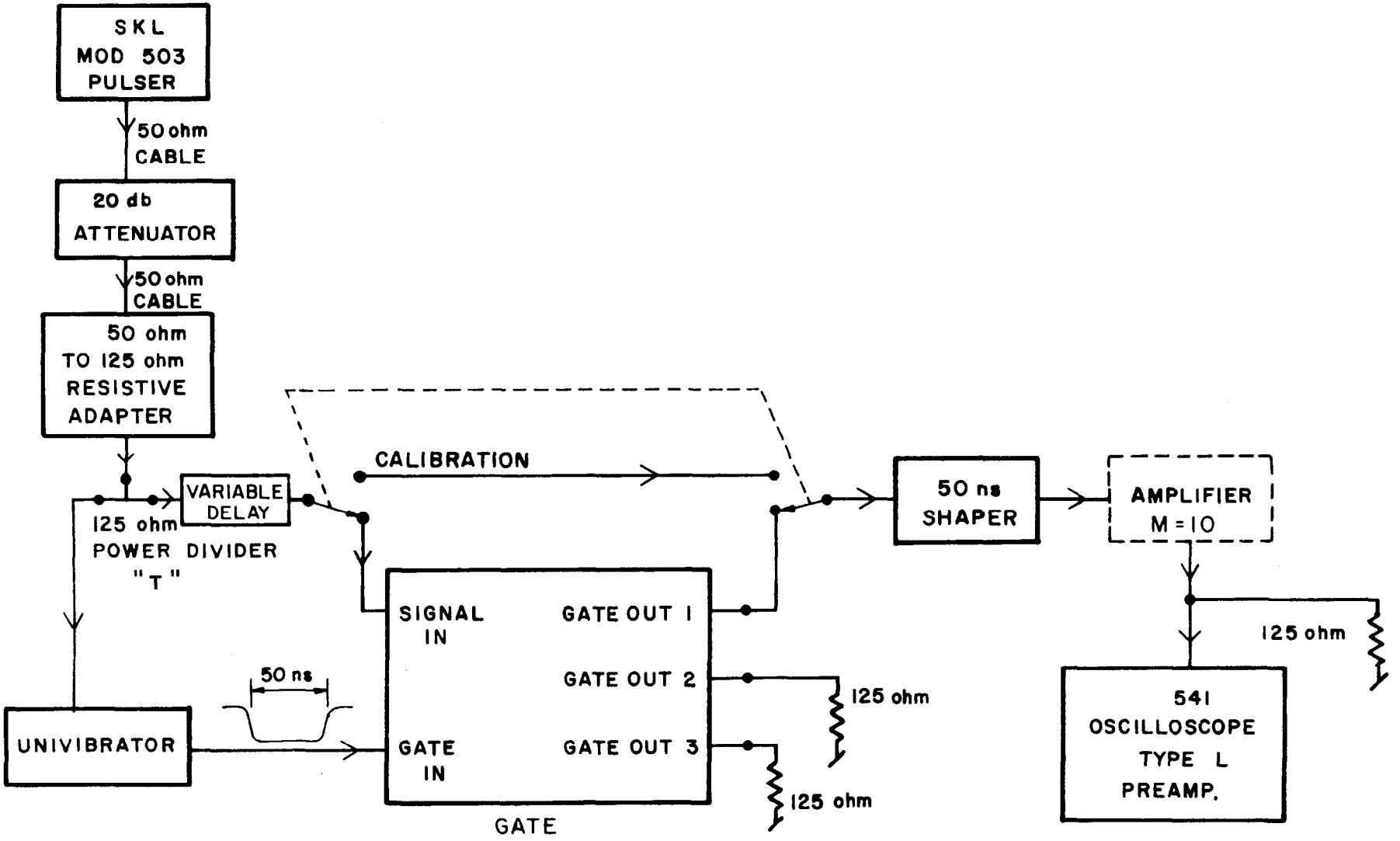
SKL
MOD 503
PULSER
50 ohm
CABLE
20 db
ATTENUATOR
50 ohm
CABLE
50 ohm
TO 125 ohm
RESISTIVE
ADAPTER
CALIBRATION
VARIABLE
DELAY
125 ohm
POWER DIVIDER
"T"
50 ns
SHAPER
AMPLIFIER
M = 10
SIGNAL
IN
GATE OUT 1
GATE OUT 2
GATE OUT 3
125 ohm
125 ohm
125 ohm
50 ns
UNIVIBRATOR
GATE
IN
GATE
541
OSCILLOSCOPE
TYPE L
PREAMP.

FIG. 4

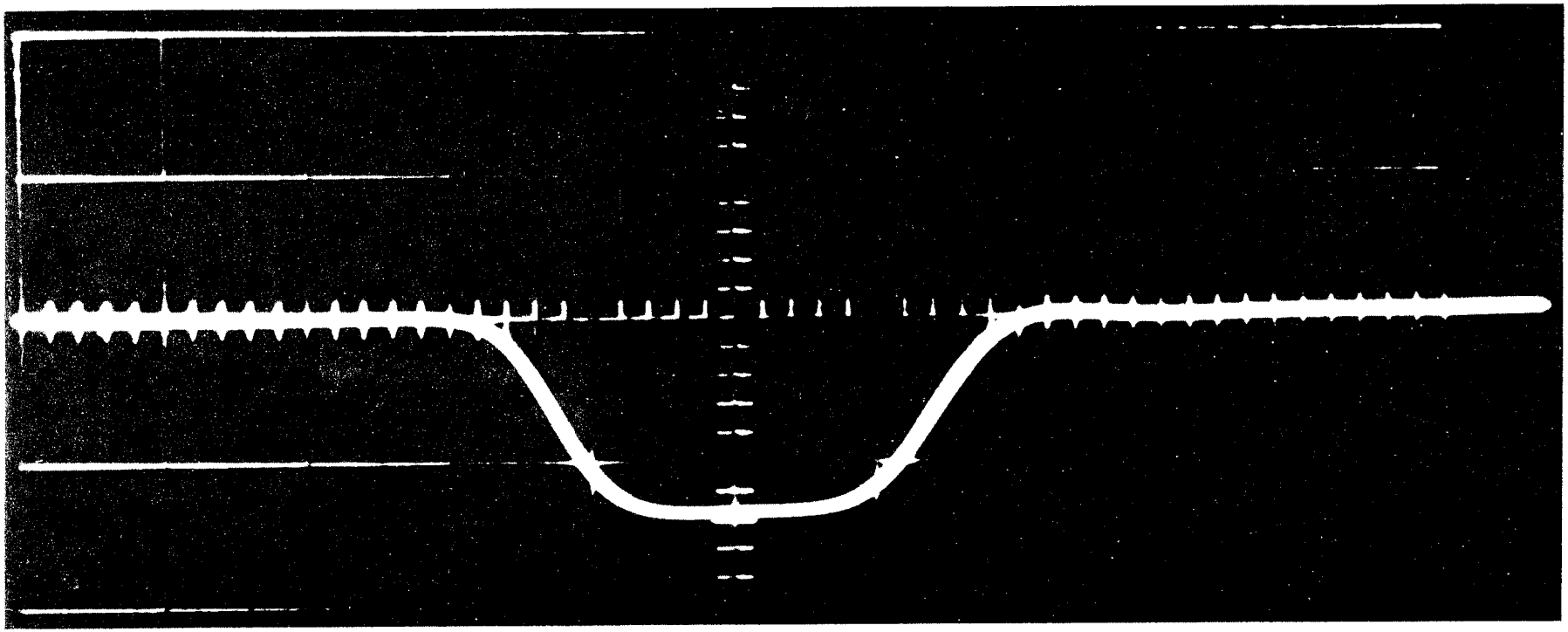

Fig. 5

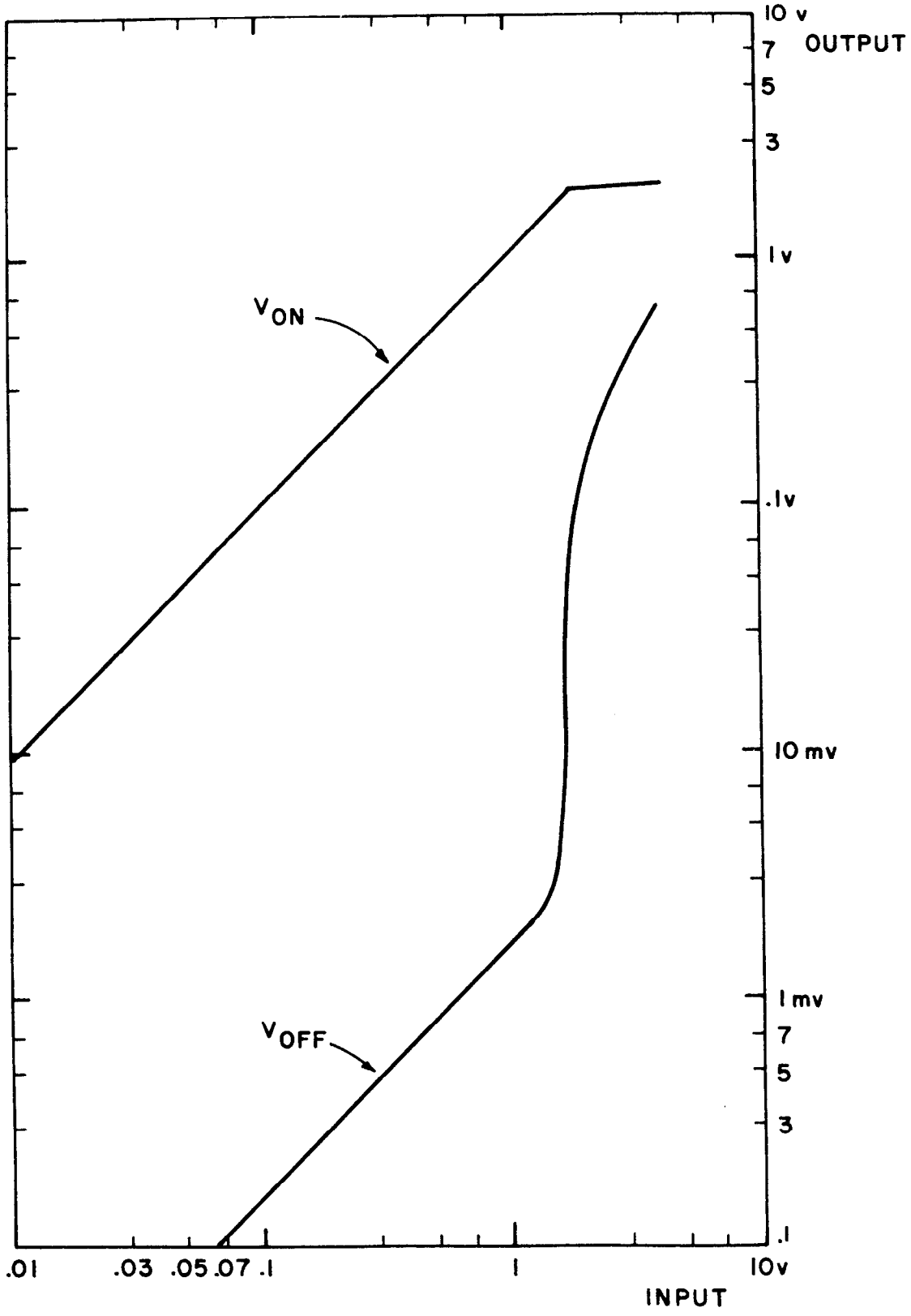
10 v
7
OUTPUT
5
3
1 v
.1v
10 mv
1 mv
7
5
3
.1
V_{ON}
V_{OFF}
.01
.03
.05
.07
.1
1
10v
INPUT

FIG. 6

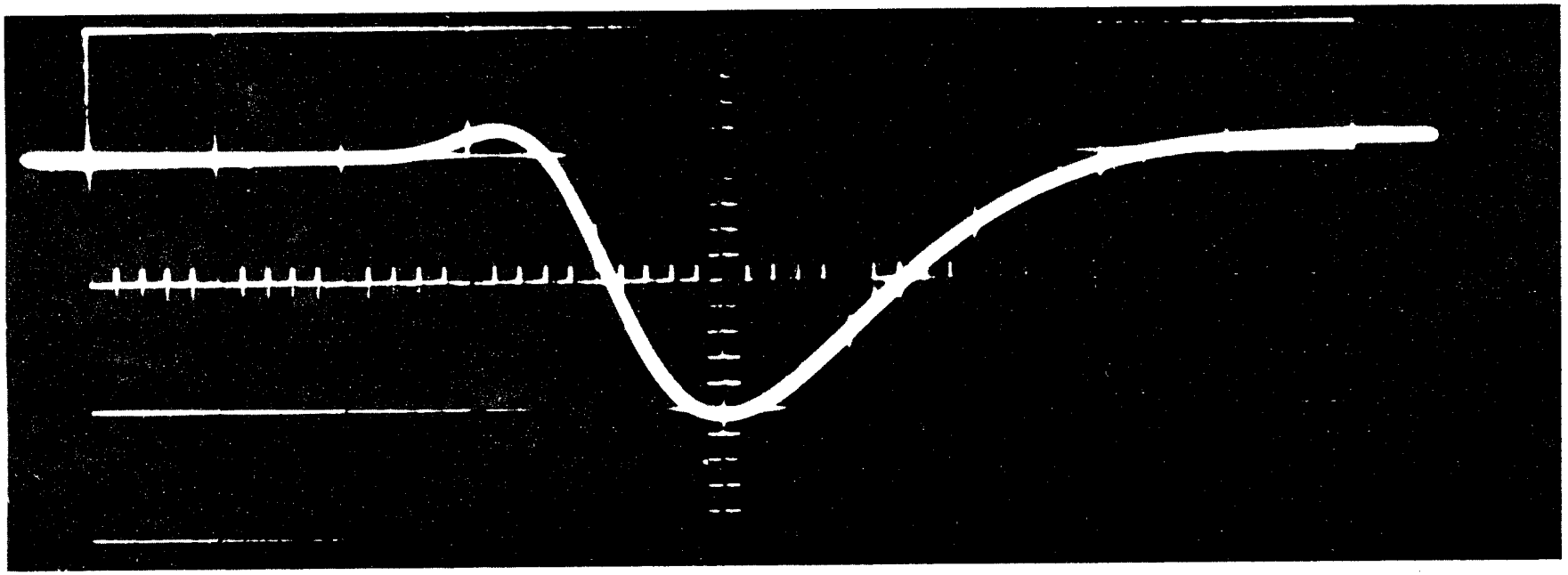

Fig. 7

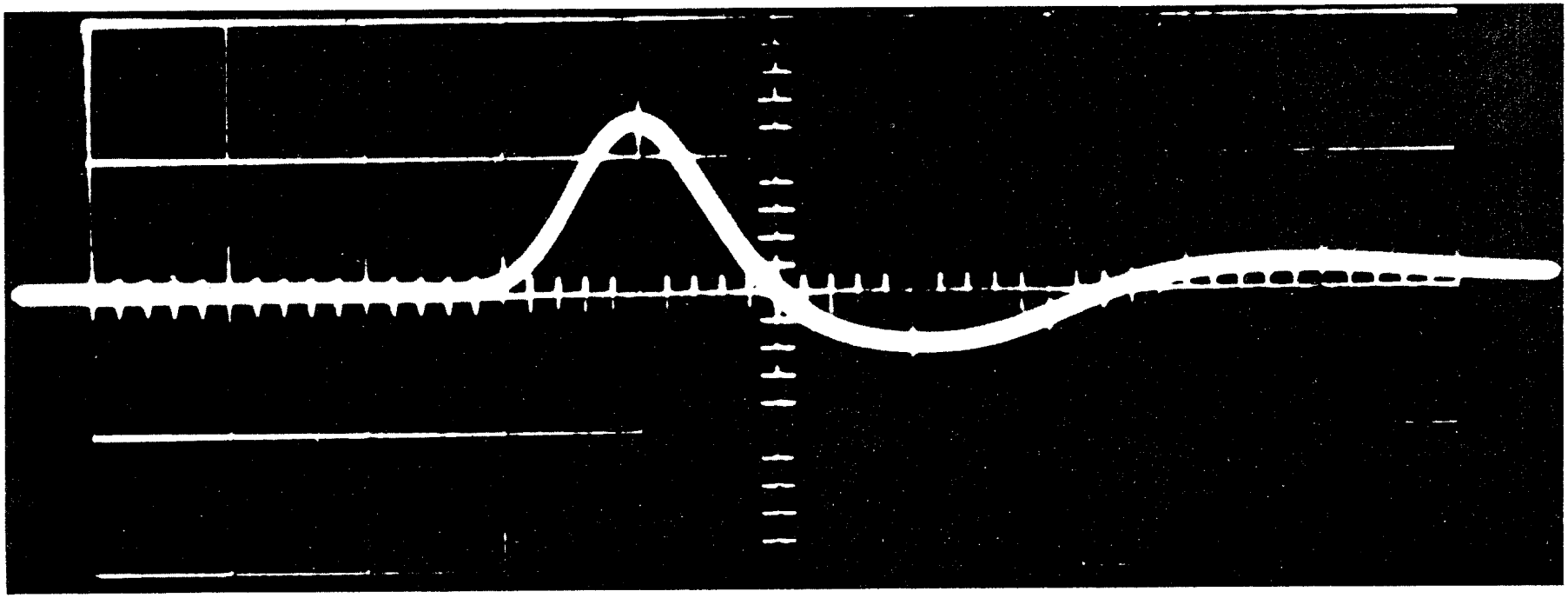

Fig. 8

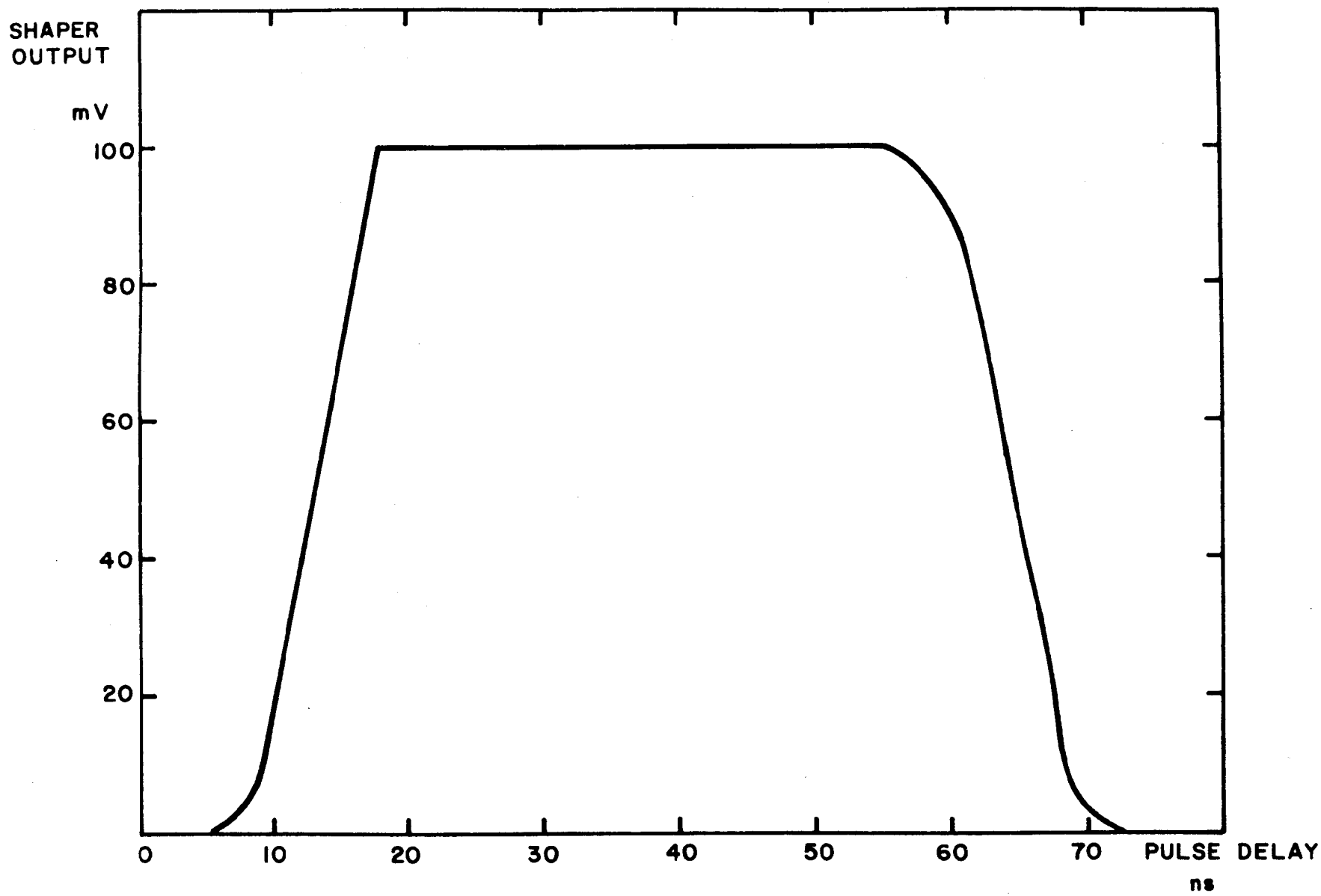
SHAPER
OUTPUT
mV
100
80
60
40
20
0
10
20
30
40
50
60
70
PULSE DELAY
ns

FIG. 9

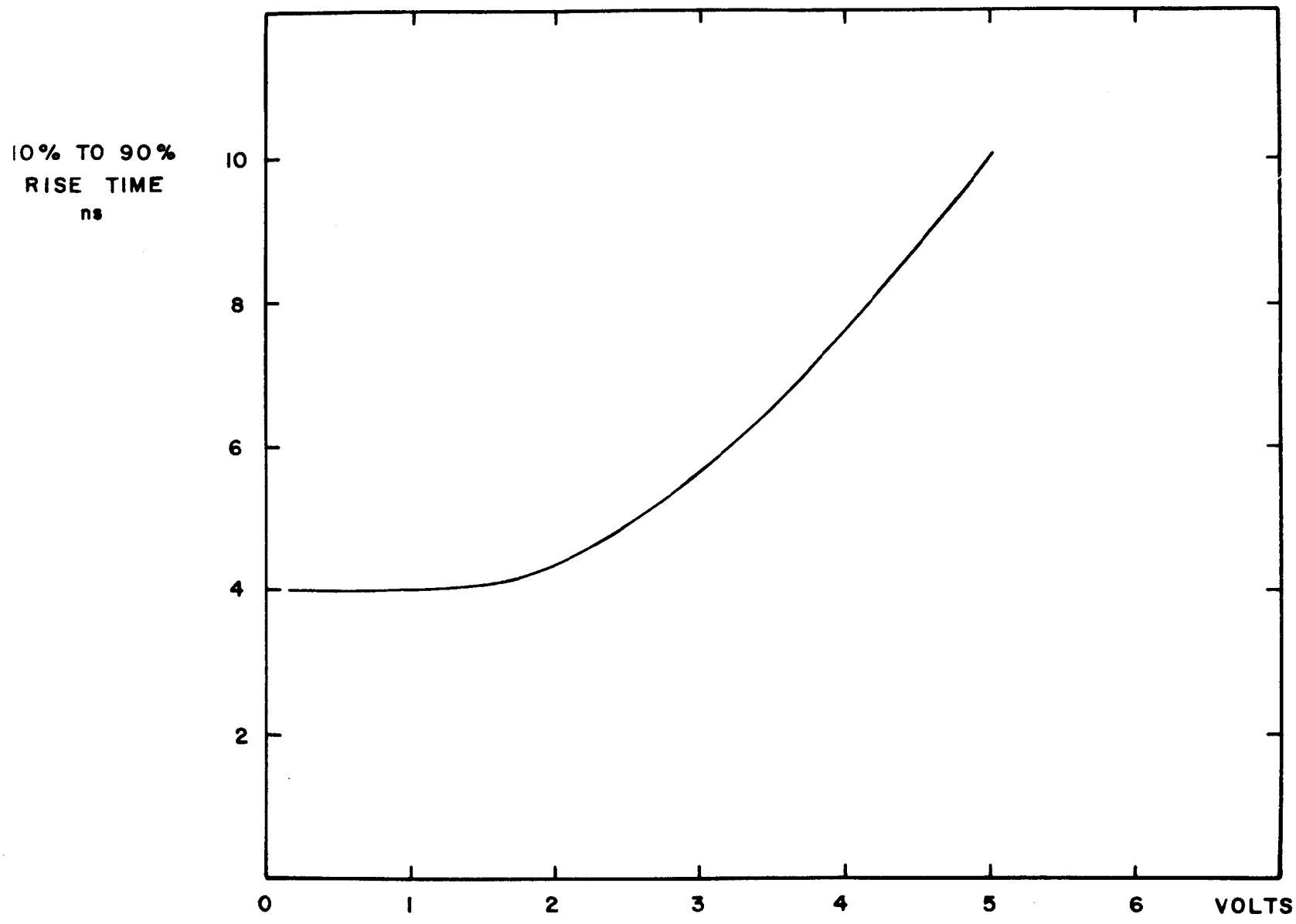

FIG. 10

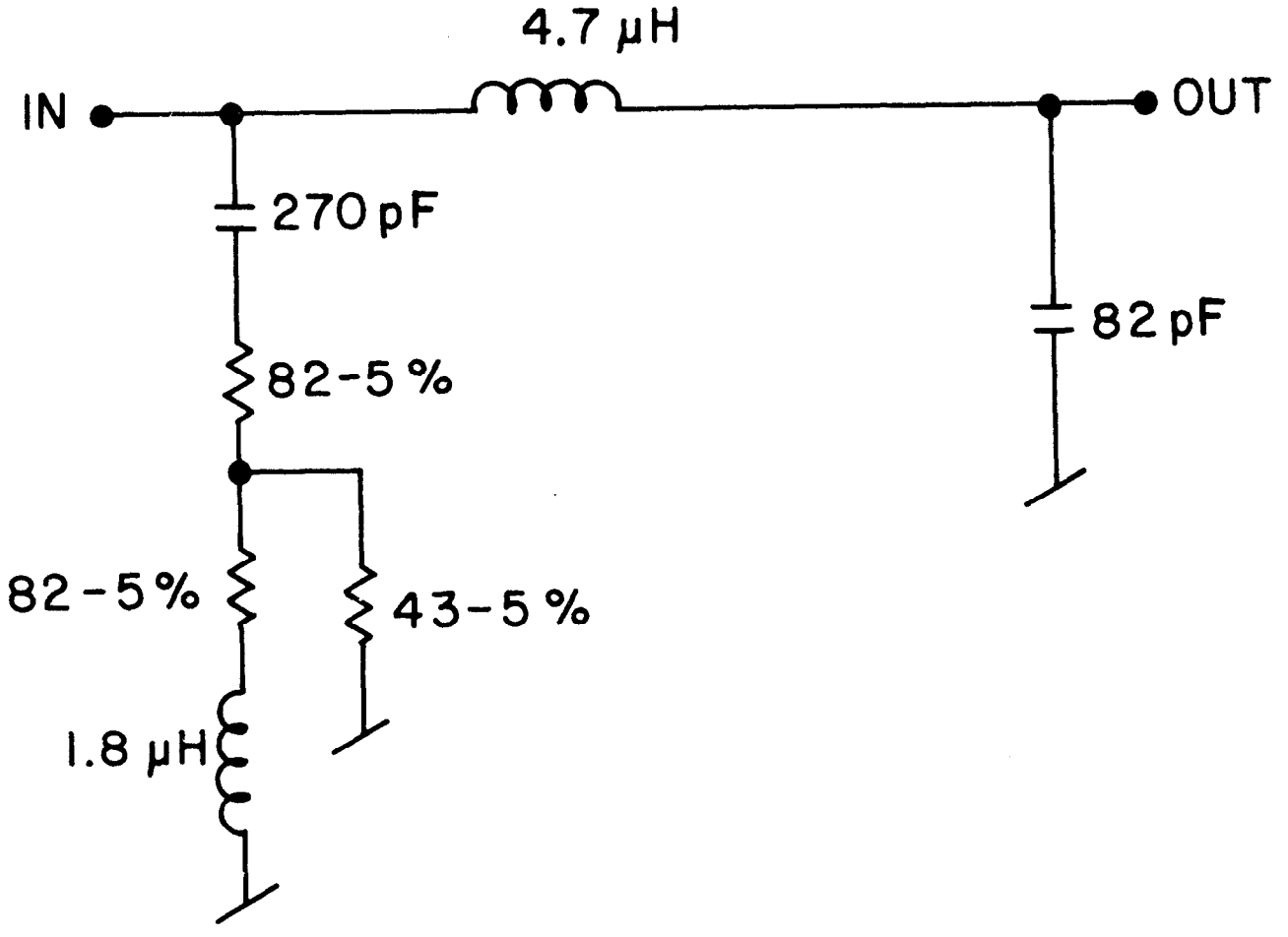

FIG. 11