The Design and Initial Testing of a Beam Phase and Energy Measurement for LEDA*

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Abstract. A diagnostic system being designed to measure the beam phase and beam energy of the Low Energy Demonstration Accelerator (LEDA) is described and the characterization of the prototype presented. The accelerator, being built at LANL, is a 350 MHz proton linac with a 100 mA beam. In the first beam experiments, the 6.7 MeV RFQ will be characterized. Signals received from an rf cavity probe in the RFQ and capacitive pick-ups along the high-energy beam transport line will be compared in phase in order to calculate the beam phase and energy. The 350 MHz signals from four pick-ups will be converted to 2 MHz in a VXI-based down converter module. A second VXI phase processor module makes two, differential-phase measurements based on its four 2 MHz inputs. The heart of this system is the phase processor module. The phase processor consists of an analog front end (AFE), digital front end (DFE), digital signal processing (DSP) modules and the VXI bus interface. The AFE has an AGC circuit with a >60 dB dynamic range with a few degrees of phase shift. Following the AFE is the DFE which is uses an in-phase and quadrature-phase (I and Q) technique to make the phase measurement. The DSP is used to correct the real-time data for phase variations as a function of dynamic range and system offsets. The prototype phase module gives an absolute accuracy of ±0.5 degrees with a resolution of <0.1 degrees and a bandwidth of 200 kHz.

INTRODUCTION

A diagnostic system is being designed to measure the beam phase and beam energy for the LEDA accelerator. We have chosen to base the design of this new system on work previously done at Los Alamos on the Ground Test Accelerator (GTA) program (1). A simplified diagram of this approach is shown in Figure 1. The LEDA beam is bunched at 350 MHz by the RFQ. The energy of the beam is calculated by measuring the time-of-flight of the beam between a pair of pickups with a known separation. To calculate the time-of-flight we measure the difference in phase of 350 MHz beam signals from the two pickups.

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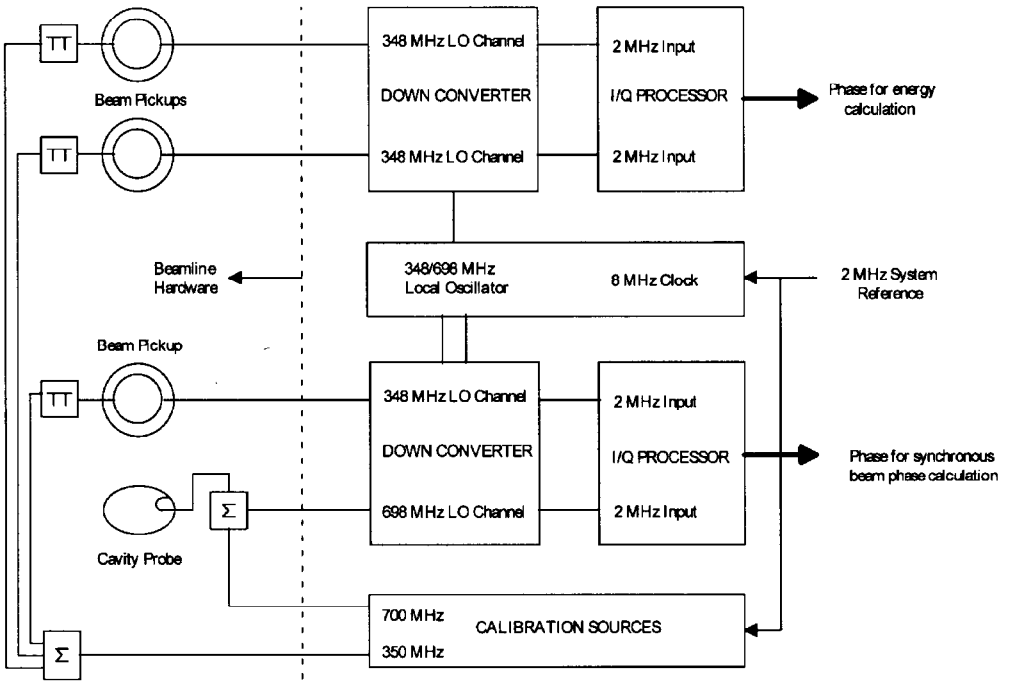

FIGURE 1. Block diagram of the beam phase and energy measurement system to be used on the LEDA accelerator.

To compare the performance of the RFQ with the theory, we also need to measure the phase of the beam, relative to the cavity field, as it exits the RFQ. This measurement is made by measuring the phase difference between signals from a cavity field probe and a nearby beamline pickup. We translate the phase measured at the pickup location back to the RFQ exit location, based on the measured beam energy and the separation distance.

The system is comprised of four major components. These are the capacitive beam pickups, rf down-converter module, I/Q phase processing module, and the calibration hardware. Though each of these components will be described, this paper will concentrate on the I/Q (in-phase/quadrature-phase) processor module.

Capacitive Beam Probes

The LEDA beamline of interest is a 1.87 in.-i.d. pipe assembled with 4.5 in.-o.d. Conflat® flanges. Each capacitive probe is assembled within a single Conflat® flange to conserve space. The capacitive probe consists of a ring, which is supported by two SMA feedthrough connectors. This ring is 0.2 inches long and slightly larger in i.d. than the i.d. of the beamline pipe. Figure 2 shows a probe assembled within a 4.5 in. diameter flange. The dimensions of the ring and the cavity into which it is mounted were selected such that the ring forms a 100 Ω transmission line. When the probe is connected between two 50 Ω cables it presents a very low impedance perturbation (two short lengths of near-100 Ω line in parallel). This design was chosen to allow a

calibration signal to be injected in one connector, passing through to the normal output connector on the opposite side.

FIGURE 2. A capacitive beam probe within a 4.5 in. Conflat® vacuum flange. The impedance of the ring is 100 Ω to match the 50 Ω termination.

One potential problem with this type of probe is that the phase of the beam signal is dependent on the position of the beam to some degree. All of our probes are calibrated in a transmission line-test fixture using a centered center conductor. As the beam moves away from the center of the probe, an offset error is introduced. In our energy-measurement case, the beam is expected to be in essentially the same location in the two probes used for the measurement and hence the error is differentially subtracted. In the case of the output phase measurement, only one probe is used, but the beam is expected to be near the center of the probe where the error is minimal. For small variations in beam position we expect to see an error of approximately 0.5 deg/mm offset, at 350 MHz.

Down-converter Module

The 350 MHz and 700 MHz signals from the capacitive probes and the cavity sample probe are being down-converted to 2 MHz where more precise phase measurements can be made. We have built a prototype 4-channel unit that is packaged within a single wide VXI module. The I/Q phase processor is packaged similarly.

Each channel of down-conversion is housed in a small metal box for improved isolation. A standard design is used which includes input diplexers for broadband frequency matching, a double-balanced mixer and a low-gain output amplifier. The

levels of the signals being down-converted are as large as 20 dBm and attenuation is actually required at the input of each down-converter.

One important aspect of the down-conversion is that the local oscillator frequencies must be phase-locked to the 2 MHz system reference frequency. These 348 MHz and 698 MHz sources have yet to be designed.

I/Q Processor Module

The phase measurements are all made at a frequency of 2 MHz in the I/Q processor module. This module has four input channels, configured as two differential-phase channels. A block diagram of a single phase-measurement channel is shown in Figure 3. This includes the rf input, down converter, 2 MHz phase measurement, DSP processing and the VXI interface to the control system.

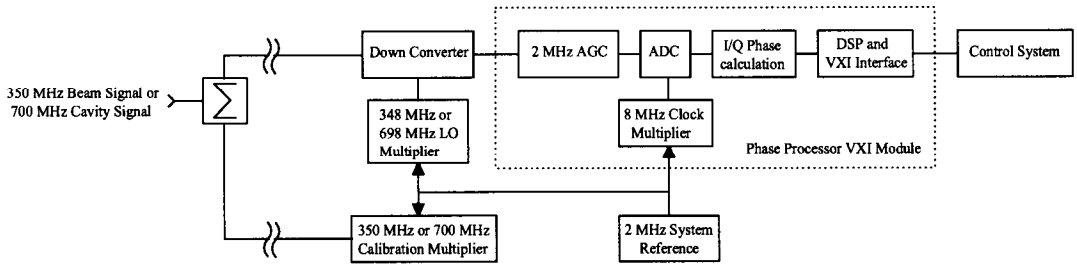

FIGURE 3. Block diagram of a single phase-measurement channel.

Phase Module Design

The phase-measurement technique employed is to sample the 2 MHz input signal at an 8 MHz clock rate which, is phase-locked to the 2 MHz system reference. By sampling at four times the input frequency, we produce a repeating pattern of I, Q, –I and –Q values (see Figure 4). This data stream phase would be arbitrary except for the fact that all phase measurement channels are sampled with the same 8 MHz clock. One of the important aspects of this technique is the high common-mode rejection of low-frequency noise. The digital process includes subtracting –I from I (and –Q from Q) removing the common mode error in both the signal and the ADC circuit. The phase is then calculated the as arctangent of the ratio I/Q.

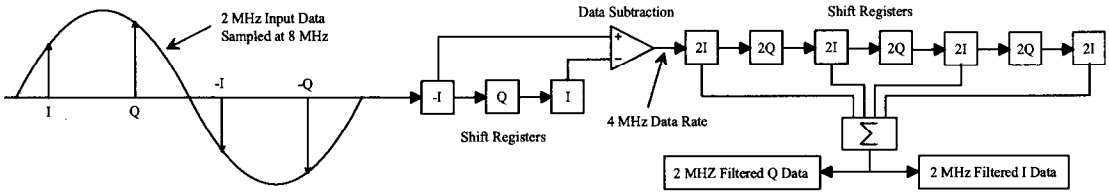

FIGURE 4. The I and Q data is created by sampling the 2 MHz input at 8 MHz. A simplified diagram of the digital process that follows the sampling is shown.

The I/Q processor contains two independent differential-phase channels. Figure 5 shows a block diagram of one differential phase channel. Two of these channels are in each processor module. The input circuits contain AGC stages to allow the input level to vary by over 60 dB while providing a constant level to the ADCs. Each AGC uses an Analog Devices AD600 dual, variable-gain amplifier as the heart of the circuit. This device is unique in that it has a fixed-gain amplifier proceeded by a 40 dB variable attenuator (2). This provides a more constant group-delay over the entire gain range. Two stages are used in series to achieve about 76 dB of constant-output range. This is considerably more than the 46 dB range in beam current that we expect.

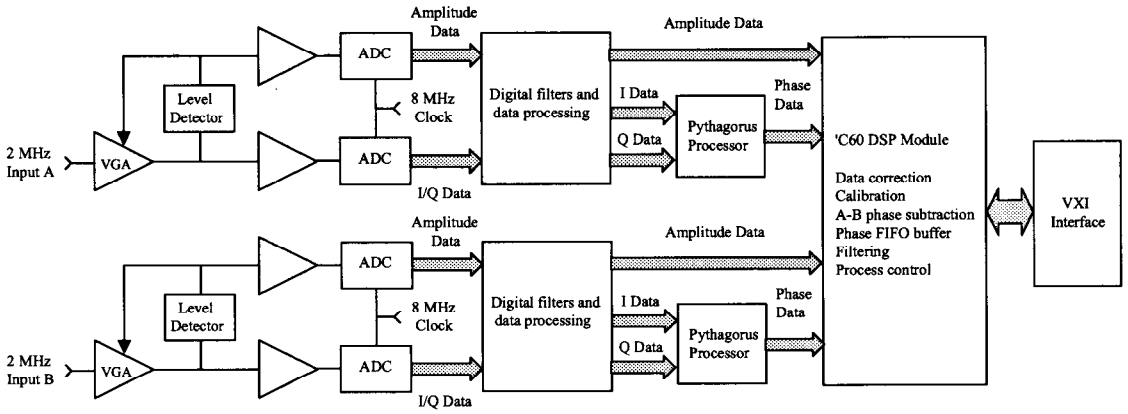

FIGURE 5. Two phase-measuring channels are processed and the data subtracted to produce a single differential-phase measurement block. The phase module contains two independent differential-phase measurements like the one shown.

The AGC circuit is followed by two Analog Devices ADS802, 12 bit ADC circuits. One samples the 2 MHz output to generate the I and Q data and another is used to digitize AGC control voltage. The gain control signal is linear at 32 dB/V. This amplitude data is used in the phase calibration algorithm.

The two data streams for each of the differential channels is processed in a custom programmable logic array, which contains the functions shown in Figure 4. These include the de-multiplexing of I and Q, data subtraction, and four-tap filtering to reduce the overall bandwidths to about 210 kHz. Though not shown in Figure 4, the amplitude data is filtered to 210 kHz as well. The most significant 16 bits of the I and Q data are passed to a Plessey Semiconductor PDSP16330 Pythagoras processor which calculates the arctangent of I/Q (as well as the magnitude, which is not used). This chip provides 12 bits of phase data for a resolution of $360/2^{12}$ or 0.0879 degrees (3).

Two DSP modules control the operation of the phase processor. These are Spectrum Signal Processors TIM-40 units with 40 MHz Texas Instruments TMS320C40 DSP chips. One processor will control each differential phase channel as well as pass data to and from the VXI interface logic. The DSP modules support several important functions. These functions include controlling the module calibration (as a function of signal amplitude), storing correction data into local RAM, and real-time correction of the phase data. The DSP modules also maintain a FIFO array of the corrected phase data and filter the data with various bandwidths down to below 10 Hz. Real-time, filtered data is available to the VXI interface as well as being output to the front panel via DAC circuits.

Performance of the AFE and DFE Circuits

At this time, the analog-front-end (AFE) and digital-front-end (DFE) circuits have been designed and tested and the complete phase processor VXI module is just now beginning initial testing. The overall performance of the phase measurement system is dominated by the characteristics of the analog- and digital-front-end circuits and these will now be presented.

The resolution and absolute accuracy of the phase measurement measure the performance of the AFE and DFE circuits. We expect the LEDA accelerator beam current to be tunable over a 46 dB range and we desire a absolute accuracy of ±0.5 degrees for the energy measurement. A resolution of 0.1 degrees should be adequate (defined as one standard deviation) at a bandwidth of 200 kHz. These requirements lead to the selection of the AGC front end and 12-bit ADC designs. The theoretical signal-to-noise ratio of the AFE is fixed at 79 dB for the first 40 dB of its gain range, and then decreases, dB for dB, as the second 40 dB of gain is utilized. At our lowest expected beam current of –46 dB, the S/N ratio should be 73 dB. For S/N ratios of 79 and 73 dB, the phase resolution should be 0.04 and 0.92 degrees respectively. The measured noise performance is shown in Figure 6. The measured resolution of about 0.05 degrees is fairly constant for the first 40 dB of signal range, increasing to about 0.12 degrees at –46 dB.

The absolute accuracy of the measurement system will depend on the linearity of the I/Q phase measurement, the accuracy of the calibration system, and the stability of the system between calibrations. At this point, we can only report on the linearity of the I/Q phase measurement. The linearity of the AFE/DFE circuits was measured by using two synthesized oscillators locked to a common reference frequency.

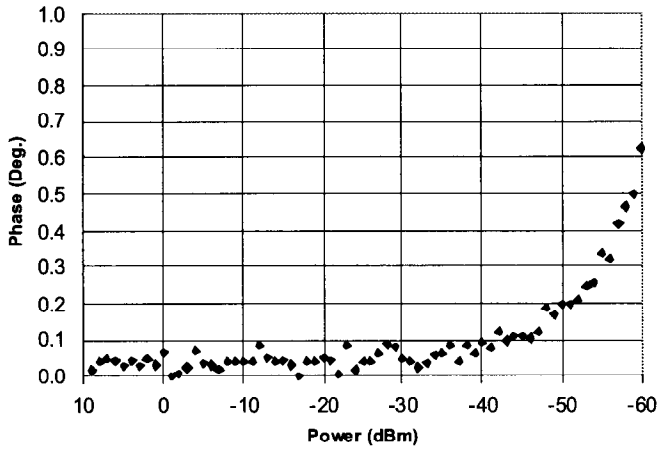

FIGURE 6. The resolution of the phase measurement as a function of input power is shown. Each point is the standard deviation of 1024 data points.

One is set to a frequency of 8 MHz while the other is set to 1.999 MHz. This provides a constant phase slew of 360 deg/ms resulting in 2000 phase measurements per cycle (2 MHz data rate). Both channels of the differential AFE/DFE circuit are simultaneously driven. The analysis includes subtracting the data from the two channels and comparing the result with a perfectly linear phase ramp. Analyzing the differential data removes a slight defect (actually a characteristic) of the programmable synthesized signal generators

used. The results of this measurement are shown in Figure 7. The rms error is 0.06 degrees with a peak-to-peak error of 0.6 degrees.

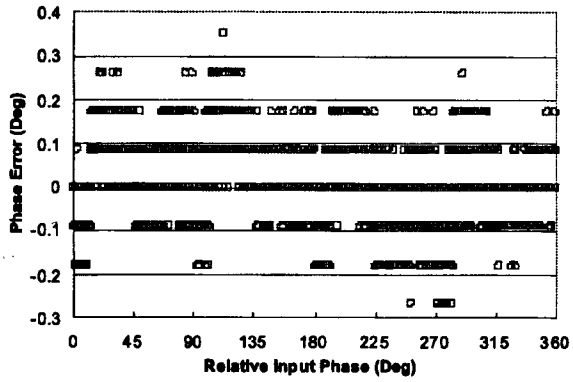

FIGURE 7. The resolution of the phase measurement as a function of input power is shown. Each point is the standard deviation of 1024 data points.

Calibration System

The calibration hardware and signal generation circuits will be located in a separate chassis that is controlled by the phase processor module over the VXI bus. The calibration system will generate 350 MHz and 700 MHz signal sources, which are phase-locked to the 2 MHz system reference and have programmable amplitudes over a 63.5 dB range. When enabled, these signals pass through the phase probes as well as being coupled into the cavity field probe. The calibration signals will pass through the entire signal chain to allow for a complete system calibration in situ. In most cases, the calibration signals for a pair of beam probes are derived from a passive rf splitter with short (<1 m) cable runs between the probes. In such cases, we need only be concerned with the phase stability of the splitter and two short cables and not that of the oscillator or the 150-foot-long cable runs between the electronics and the beamline. The single exception is the 700 MHz signal for the cavity probe and its associated 350 MHz beam signal. These calibration signals will include errors due to cable stability and oscillator phase drifts.

CONCLUSION

The design and testing of a new beam-phase and energy measurement system is in progress. Beam and cavity-field signals at 350 MHz and 700 MHz are down-converted to 2 MHz for phase measurement. Both the down-converter and phase processors are packaged in the VXI format. The I/Q phase processor has demonstrated a dynamic range well beyond the 46 dB required, with a resolution of near 0.1 degrees and an absolute accuracy of ±0.3 degrees. Testing of the DSP control hardware and software is underway.

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