General Standards Corporation
High Performance Bus Interface Solutions

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PMC-16AI64SS

REFERENCE MANUAL

64-CHANNEL 16-BIT
SIMULTANEOUS SAMPLING
PMC ANALOG INPUT BOARD

PRELIMINARY; EXTENDED CAPABILITIES
(Highlighted in red)

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SECTION 1.0

INTRODUCTION

1.1 General Description

The PMC-16AI64SS board is a single-width PCI mezzanine card (PMC) that provides high-speed simultaneous 16-bit analog input capability for PMC applications. 64 analog input lines can be digitized simultaneously at rates up to 200,000 conversions per second per channel, with software-controlled voltage ranges of ±2.5V, ±5V or ±10V. The board is functionally compatible with the IEEE PCI local bus specification Revision 2.2, and is mechanically and electrically compatible with the IEEE compact mezzanine card (CMC) specification IEEE 1386. A PCI interface adapter supports the "plug-n-play" initialization concept.

Autocalibration determines offset and gain correction values for each input channel, and the corrections are applied subsequently during acquisition. A selftest switching network routes calibration reference signals to each channel through internal selftest switches, and permits board integrity to be verified by the host.

Power requirements consist of +5 VDC from the PCI bus in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional air cooling. Specific details of physical characteristics and power requirements are contained in the PMC-16AI64SS product specification. Figure 1.1-1 shows the physical configuration of the board, and the arrangement of major components.

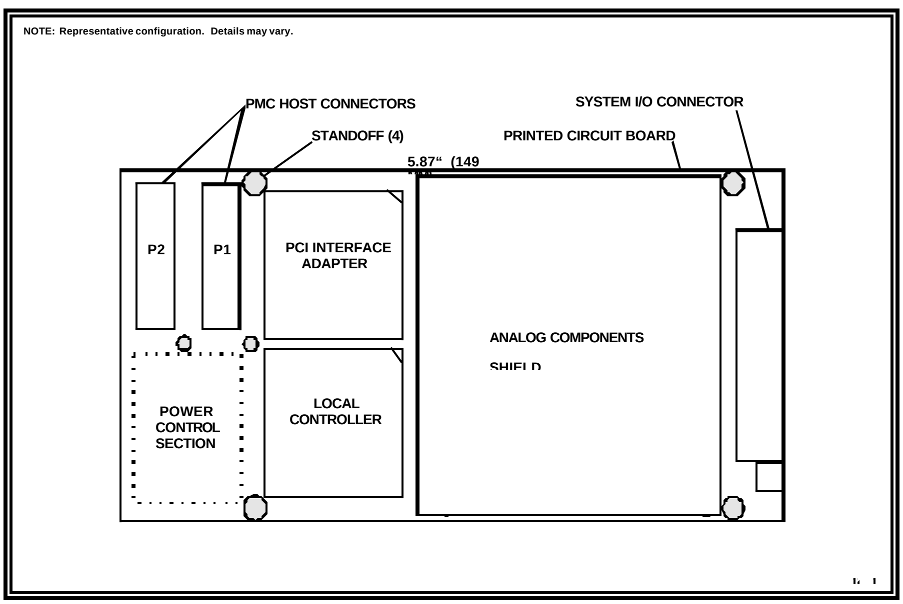

Figure 1.1-1. Physical Configuration

The board is designed for minimum off-line maintenance, and includes internal monitoring and autocalibration features that eliminate the need for disconnecting or removing the module from the system for calibration. All system input and output connections are made through a single 80-pin, dual-ribbon front-access I/O connector.

1.2 Functional Overview

Principal capabilities of the PMC-16AI64SS board are summarized in this list of features:

- 64 Single-Ended Simultaneously-Sampled 16-Bit Input Channels
- Software-Selectable Analog Input Ranges of ±10V, ±5V, ±2.5V, 0/+5V or 0/+10V
- 64K-Sample Analog Input FIFO Buffer
- Selectable Differential Processing
- 200 KSPS per Channel Conversion Rate (12.8 MSPS Aggregate Rate)
- Dual cascadeable Internal Rate Generators
- Supports Synchronization of Multiple Boards
- Internal Autocalibration of all Analog Input Channels
- Mastering DMA Engine

The 16-Bit PMC-16AI64SS analog input board samples and digitizes 64 input channels simultaneously at rates up to 200,000 samples per second for each channel. The resulting 16-bit sampled data is available to the PCI bus through a 64K-Sample FIFO buffer. Each input channel contains a dedicated 16-Bit sampling ADC. All operational parameters are software configurable.

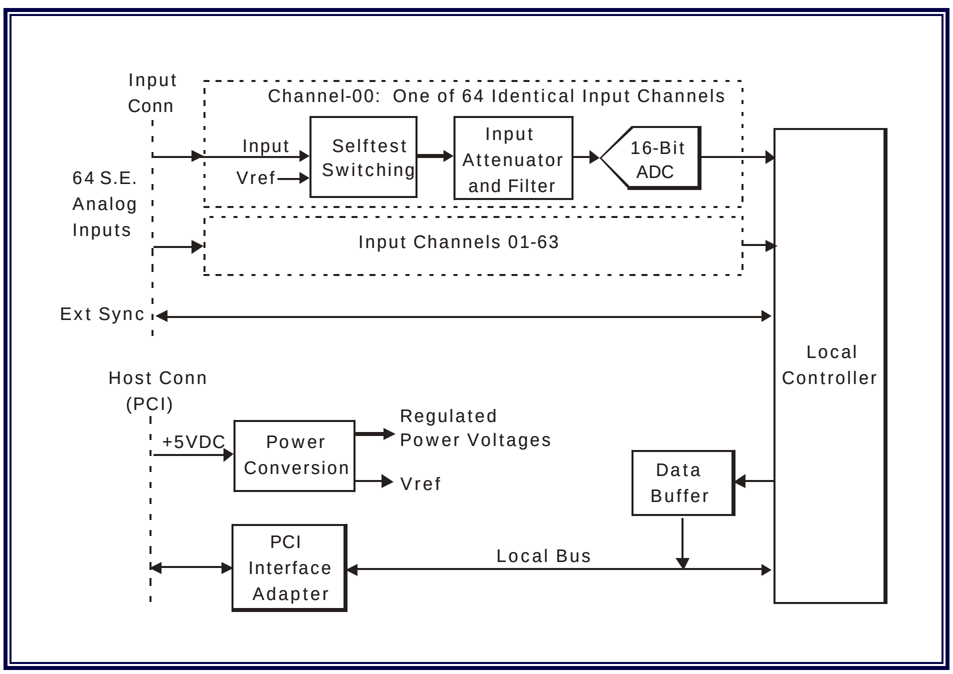

Figure 1.2-1. Functional Organization

Inputs can be sampled in groups of 2, 4, 8, 16, 32 or 64 channels, or any single channel can be sampled continuously. The sample clock can be generated from an internal rate generator, or directly through software, or by external hardware.

SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping envelope, position the board with the shield and standoffs facing the host (carrier) board, and with the I/O connector oriented toward the front panel. Align the two PCI connectors located at the end of the board opposite the I/O connector, with the mating connectors on the host board. Then carefully press the board into position on the host. Verify that the PCI connectors have mated completely and that the standoffs are seated against the host board.

Attach the board to the host with four 2.5 x 6.5mm panhead screws. Pass the screws through the back of the host into the four mounting holes on the board. Tighten the screws carefully to complete the installation. Do not overtighten.

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2-1. The I/O connector is designed to mate with an 80-pin dual-ribbon connector, equivalent to Robinson Nugent #P50E-080-S-TG. The insulation displacement (IDC) Robinson Nugent cable connector accepts two 40-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2-1 and in Figure 2.2-1. Contact the factory if preassembled cables are required.

Table 2.2-1. System Connector Pin Functions

PIN	ROW-A SIGNAL
1	INP00
2	INP01
3	INP02
4	INP03
5	INPUT RTN
6	INP04
7	INP05
8	INP06
9	INP07
10	INPUT RTN
11	INP08
12	INP09
13	INP10
14	INP11
15	INPUT RTN
16	INP12
17	INP13
18	INP14
19	INP15
20	INPUT RTN
21	INP16
22	INP17
23	INP18
24	INP19
25	INPUT RTN
26	INP20
27	INP21
28	INP22
29	INP23
30	INPUT RTN
31	INP24
32	INP25
33	INP26
34	INP27
35	INPUT RTN
36	INP28
37	INP29
38	INP30
39	INP31
40	INPUT RTN

PIN	ROW-B SIGNAL
1	INP32
2	INP33
3	INP34
4	INP35
5	INPUT RTN
6	INP36
7	INP37
8	INP38
9	INP39
10	INPUT RTN
11	INP40
12	INP41
13	INP42
14	INP43
15	INPUT RTN
16	INP44
17	INP45
18	INP46
19	INP47
20	INP48
21	INPUT RTN
22	INP49
23	INP50
24	INP51
25	INP52
26	INP53
27	INPUT RTN
28	INP54
29	INP55
30	INP56
31	INP57
32	INP58
33	INPUT RTN
34	INP59
35	INP60
36	INP61
37	INP62
38	INP63
39	SYNC I/O RTN
40	SYNC I/O

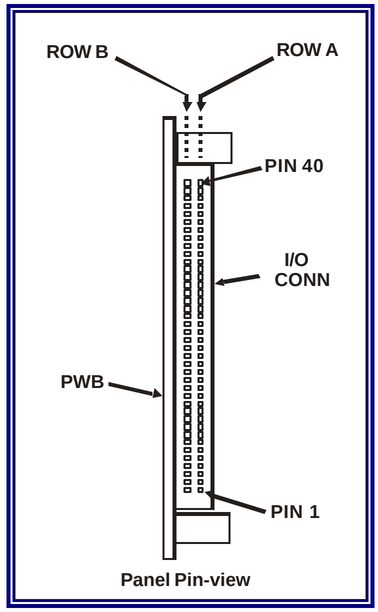

Figure 2.2-1. Input/Output Connector

2.3 System Configuration

2.3.1 Analog Inputs

Analog inputs INP00-INP63 (Table 2.2-1) can be configured as 1, 2, 4, 8, 16, 32 or 64 single-ended channels. Input configurations start at Channel-00, and proceed upward through consecutive channels to the highest-numbered channel in the configuration. The hardware input configuration must be acknowledged by the control software.

Single-ended inputs share a common input return that provides a return path for all inputs, making isolation from other system grounds a critical issue. If the signal sources are returned externally to system ground when operating in this mode, a potential difference between the system ground and input return can cause erroneous measurements, or may generate excessive ground current sufficient to damage the board.

A signal return pin (INPUT RTN) is provided in the I/O connector for every 4 or 5 input channels. If the signal sources are isolated from each other, and from system ground (Figure 2.3-1a), the returns in each 4 or 5 Channel group should be connected together at the source, and to at least one INPUT RTN pin in the connector.

For signal sources that have a common isolated return at the source (Figure 2.3-1b), the common return should be connected to at least one INPUT RTN pin for every 4 or 5 active input channels.

To minimize crosstalk between input channels at higher frequencies, all INPUT RTN pins should be connected to signal source returns. The INPUT-RTN pins are connected together internally within the board, and are electrically common to the system or PCIbus ground.

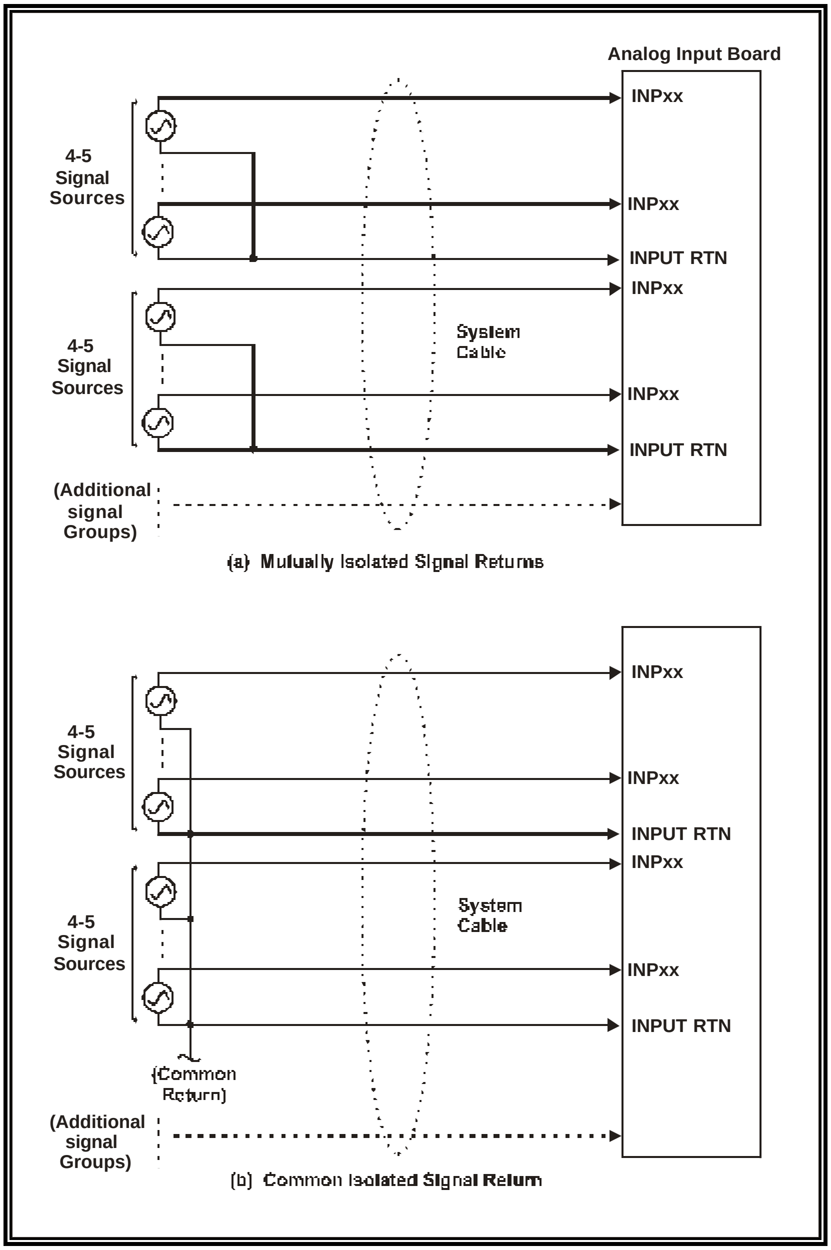

Figure 2.3-1. Analog Input Configurations

2.3.2 External Sync I/O

The SYNC I/O pin in the I/O connector is a bidirectional TTL synchronization signal that provides external control of analog input sample triggering. The SYNC I/O signal is referenced to the SYNC I/O RTN pin, which is connected internally to digital ground.

When configured as an input, this signal initiates a triggered sample of all active input channels. The SYNC I/O input is asserted LOW, and is pulled HIGH internally through a 4.7 KOhm resistor.

When configured as an output, the SYNC I/O signal is asserted for approximately 75-90 nanoseconds at the beginning of each scan. The SYNC I/O output signal is a TTL level that can synchronize the operation of multiple target boards to a single initiator board. Like the SYNC I/O input signal, the SYNC I/O output signal is asserted LOW. Loading of the SYNC output should be limited to 10 milliamps or less.

Specific input/output configurations are determined by individual system requirements, and must be acknowledged by the control software.

2.3.3 Multiboard Synchronization

If multiple boards are to be synchronized together, the SYNC I/O and SYNC I/O RTN pins from one board, the ***initiator***, are connected to the SYNC I/O and SYNC I/O RTN pins of as many as four ***target*** boards (Figure 2.3-2). The controlling software determines specific synchronization functions.

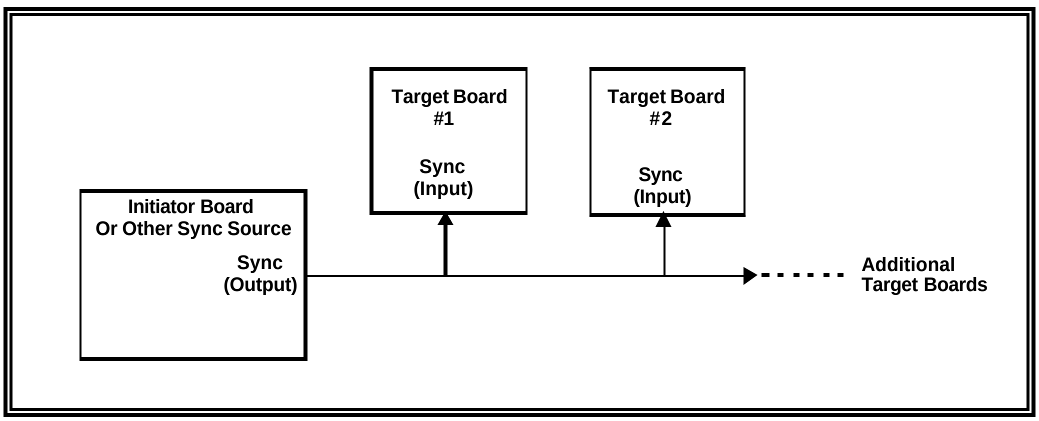

Figure 2.3-2. Multiboard Synchronization

2.4 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference verification and possible adjustment. The optimum verification interval will vary, depending upon the specific application, but in most instances an interval of one year is sufficient.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and system interface signal levels, should be evaluated before troubleshooting of the board itself is attempted. A board that has been determined to be defective should be returned to the factory for detailed problem analysis and repair.

2.5 Reference Verification

All analog input channels are software-calibrated to a single internal voltage reference by an embedded autocalibration software utility. The procedure presented here describes the verification and adjustment of the internal reference.

2.5.1 Equipment Required

Table 2.5-1 lists the equipment required for verifying or adjusting the internal reference. Alternative equivalent equipment may be used.

Table 2.5-1. Reference Verification Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±10 Volts.	Hewlett Packard	34401A
Host board with single-width PMC adapter	(Existing host)	---
Test cable; suitable for connecting the digital multimeter to two 0.024-inch square test posts.	---	---

2.5.2 Verification and Adjustment

The following procedure describes the verification of the single reference voltage that ensures conformance to the product specification. Adjustment of the internal reference, if necessary, is performed with an internal trimmer that is accessible as shown in Figure 2.5-1.

This procedure assumes that the board is installed on a host board, and that the host is installed in a system.

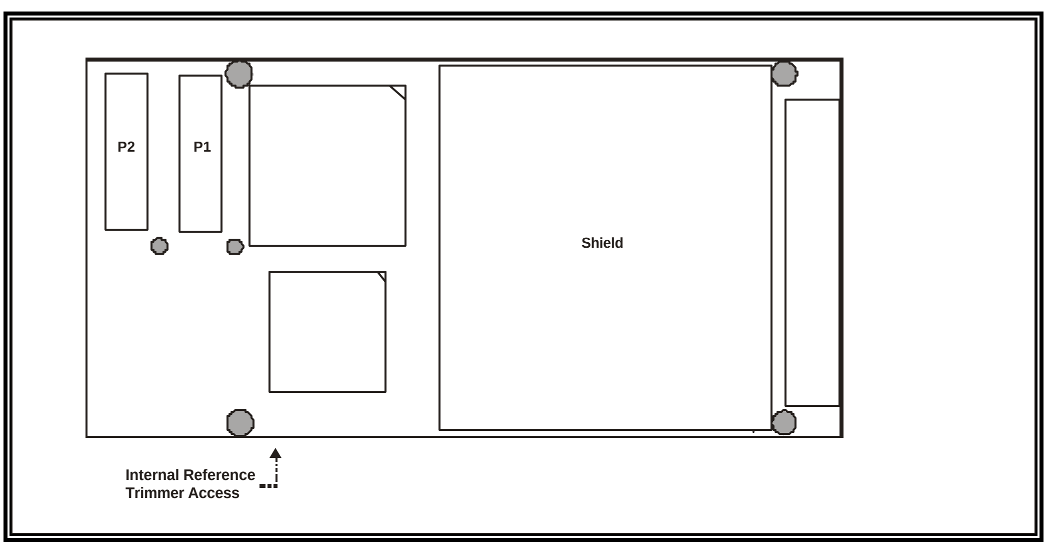

Figure 2.5-1. Reference Adjustment Access

1. Connect the digital multimeter between VCAL_PFS (+) Pin-3, and REF RTN (-) Pin-4 in the J2 test connector.
2. If power has been removed from the board, apply power now. Wait at least 10 minutes after power is applied before proceeding..
3. Select the ±10V input range.
4. Verify that the digital multimeter indication is +9.9900 VDC ±0.0009 VDC. If the indication is not within this range, adjust the INTERNAL REFERENCE trimmer until the digital multimeter indication is within the specified range.
5. Verification and adjustment is completed. Remove all test connections.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PMC-16AI64SS board is compatible with the PCI Local Bus specification, and supports auto configuration at the time of power-up. A PLX™ PCI-9080 adapter controls the PCI interface. Configuration-space registers are initialized internally to support the location of the board on any 16-longword boundary in memory space. After initialization has been completed, communication between the PCI bus and the local bus takes place through the control and data registers shown in Table 3.1-1. All data transfers are long-word D32. Any of the predefined operational conditions identified throughout this section can invoke a single interrupt request from the board. DMA access is supported for data transfers from the analog input data buffer.

Table 3.1-1. Control and Data Registers

OFFSET (Hex)	REGISTER	ACCESS MODE*	DEFAULT	PRIMARY FUNCTION
0000	BOARD CONTROL (BCR)	RW	0000 4060h	Board Control Register (BCR)
0004	INTERRUPT CONTROL	RW	0000 0008h	Interrupt conditions and flags
0008	INPUT DATA BUFFER	RO	0000 0001h	Analog input data buffer
000C	INPUT BUFFER CONTROL	R/W	000X FFFEh	Input buffer threshold and control
0010	RATE-A GENERATOR	RW	0001 0960h	Rate-A generator freq selection
0014	RATE-B GENERATOR	RW	0000 0050h	Rate-B generator freq selection
0018	BUFFER SIZE	RO	0000 0000h	Number of values in the input buffer
001C	(Reserved)	---	---	Inactive
0020	SCAN AND SYNC CONTROL	R/W	0000 0005h	Channels per scan; Clocking and Sync sources.
0024	(Reserved)	---	---	Inactive
0028	FIRMWARE REVISION **	RO	000x xxxxh	Firmware revision
002C	AUTOCAL VALUES **	R/W	0000 080xh	Autocal value readback.
0030-3F	(Reserved)	---	---	Inactive

R/W = Read/Write, RO = Read-Only. ** Nonsupported register; Shown for reference only.

3.2 Board Control Register (BCR)

As Table 3.2-1 indicates, the BCR consists of 16 control bits and status flags. Specific control bits are cleared automatically after the associated operations have been completed. Control and monitoring functions of the BCR are described in detail throughout the remainder of this section.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 0000 4060h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	AIM0	0	Analog input mode. Selects system inputs or selftest mode. Defaults to System Inputs mode.
D01	R/W	AIM1	0	
D02	R/W	AIM2	0	.
D03	R/W	UNIPOLAR INPUTS	0	Selects unipolar inputs when HIGH, bipolar inputs when LOW.
D04	R/W	RANGE0	0	Analog input range. Defaults to ±10V range.
D05	R/W	RANGE1	1	
D06	R/W	OFFSET BINARY	1	Selects offset-binary analog I/O data format when asserted HIGH, or two's complement when LOW.
D07	R/W	ENABLE EXTERNAL SYNC	0	Configures the board for external sync I/O when HIGH. (The Scan and Sync control register selects TARGET or INITIATOR mode).
D08-09	R/W	DIFFERENTIAL PROCESSING	0	Selects standard or differential processing modes.
D10-11	R/W	(Reserved)	0	---
D12	R/W	*INPUT SYNC	0	Triggers a single sample of active channels when BCR Input Sync is selected in the Scan and Sync Control Register. Clears automatically upon scan completion,
D13	R/W	*AUTOCAL	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion,
D14	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets defaults for all registers.
D16-D31	RO	(Reserved)	0	Inactive

R/W = Read/Write, RO = Read-Only. *Clears automatically when operation is completed

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3-1.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

Loading of the PCI configuration registers is completed within 3 milliseconds after the assertion of a PCI bus reset, and should be required only once after the initial application of power. PCI register configuration terminates with the PCI interrupts disabled (Section 3.7).

3.3.2 Initialization

Internal control logic can be initialized without invoking configuration by setting the INITIALIZE control bit in the BCR. This action initializes the internal logic, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following default conditions:

- The BCR is initialized; all defaults are invoked,
- Analog input voltage range is ±10 Volts,
- 32 channels are active,
- Input sample clocking is from the Rate-A generator at 13,889 samples per second,
- Analog input data coding format is offset binary,
- The analog input buffer is reset to empty,
- Input rate generator Rate-A is disabled (Rate Generator Register D16 = HI).

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Input Parameters

3.4.1 Input Voltage Range

BCR control field RANGE[], as shown in Table 3.4-1 selects the analog input voltage range.

Table 3.4-1. Analog Voltage Range Selection

RANGE[1:0]	ANALOG INPUT RANGE
0	±2.5 Volts
1	±5 Volts
2	±10 Volts
3	±10 Volts

When the UNIPOLAR INPUTS control bit is HIGH in the BCR (Table 3.2-1), the ±2.5V and ±5V input ranges become 0/+5V and 0/+10V, respectively.

3.4.2 Timing Organization

Figure 3.4-1 illustrates the manner in which timing signals are organized within the board. The input sample clock selector is controlled by the Scan and Sync control register, which provides direct software control of clocking and sync operations. The external sync input and output lines permit external control of timing. Two rate generators operate directly from the master clock, which has a frequency of 33.333 MHz on the PMC-16AI64SS board.

A sample clock can be generated by either rate generator, by the INPUT SYNC control bit in the BCR, or by an external sync source. Each Input Sample Clock triggers a sample of all active input channels. An active channel group can contain from two to 64 channels, or any single channel can be sampled individually. Each active channel group commences with Channel 00, and proceeds upward through consecutive channels to the selected number of channels.

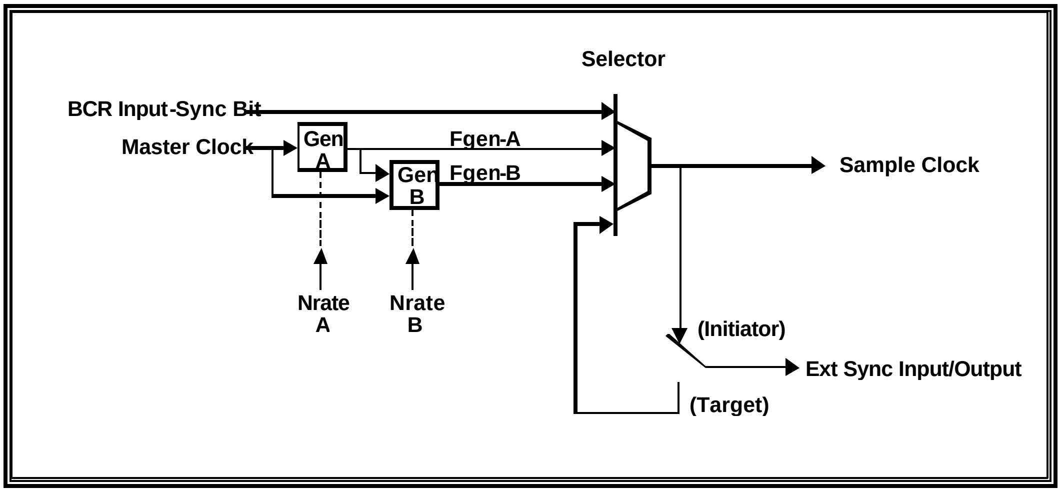

Figure 3.4-1. Clock and Sync Organization

3.4.3 Scan and Sync Control Register

The Scan and Sync control register (Table 3.4-2) controls the configuration of internal timing signals. The ACTIVE CHANNELS control field selects the number of active channels from two channels to 64 channels, or selects the single-channel mode if zero. (See Paragraph 3.5.5; Sampling Modes).

3.4.4 Sample Rate Generators

Each of the two rate generators consists of a 16-bit down-counter that divides the master clock frequency by a 16-bit integer contained in the associated rate register. The two rate registers are organized as shown in Table 3.4-3. Bits D00-D15 represent the frequency divisor Nrate, and D16 disables the associated generator when set HIGH. To prevent the input buffer from filling with extraneous data at power-up, D16 defaults to the HIGH state in the Rate-A control register.

3.4.4.1 Sample Rate Control

Each rate generator is controlled by a *divisor* **Nrate** that can be adjusted up to a maximum value of FFFFh (65535 decimal). With a master clock frequency of 33.333 MHz, the output frequency **Fgen** of each generator is determined as:

Fgen (Hz) = 33,333,000 / Nrate,

where **Nrate** is the decimal equivalent of D0-D15 in the rate generator register. **Fgen** is the sample clocking frequency, and establishes the rate at which all active channels are sampled. The maximum permissible sampling frequency **Fgen-max** is 201 KSPS.

Fgen-max = 201 KSPS.

Table 3.4-2. Scan and Sync Control Register

Offset: 0020h **Default: 0000 0005h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D02	R/W	ACTIVE CHANNELS	5	Number of active input channels: 0 => Single-Channel mode * 1 => 2 channels (00-01) 2 => 4 channels (00-03) 3 => 8 channels (00-07) 4 => 16 channels (00-15) 5 => 32 channels (00-31); Default value 6 => 64 channels (00-63) 7 =>(Reserved) * Channel selected by Single-Channel Select field below.
D03-D04	R/W	SAMPLE CLOCK SOURCE	0	Selects the analog input sample clocking source: 0 => Internal Rate-A generator output 1 => Internal Rate-B generator output 2 => External Sync input line (Selects TARGET mode) 3 => BCR Input Sync control bit.
D05-D09	R/W	(Reserved)	0	---
D10	R/W	RATE-B CLOCK SOURCE	0	Selects the clock input source for the Rate-B generator: 0 => Master clock 1 => Rate-A generator output.
D11	R/W	(Reserved)	0	---
D12-17	R/W	SINGLE-CHANNEL SELECT	0	Selects the input channel number when operating in the Single-Channel scanning mode.
D18	R/W	(Reserved)	0	---
D19-D31	RO	(Reserved)	0	Inactive

R/W = Read/Write, RO = Read-Only.

Table 3.4-3. Rate Generator Register

Offset: 0010h (Rate-A), 0014h (Rate-B) **Default: 0001 0960 (Rate-A), 0000 0050h (Rate-B)**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D15	R/W	NRATE	---	Rate generator frequency control
D16	R/W	GENERATOR DISABLE	1	Disables the rate generator when HIGH
D17-D31	RO	(Inactive)	0	---

R/W = Read/Write, RO = Read-Only.

Table 3.4-4. Rate Generator Frequency Selection

Nrate (RATE[15..0])		FREQUENCY Fgen *
(Dec)	(Hex)	(Hz)
166	00A6	200,801
167	00A7	199,599
---	---	Fgen (Hz) = 33,333,000 / Nrate

* ±0.015 percent.

3.4.4.2 Generator Cascading

To provide very low sample rates, the Rate-B generator can be configured to operate from the output of the Rate-A generator instead of from the master clock. When operating in this *cascaded* configuration, the output frequency of the Rate-B generator is:

Fgen-B (Hz) = 33,333,000 / (Nrate-A * Nrate-B) ,

which can produce sample rates as low as 0.0078 Hz.

3.4.5 Multiboard Synchronization

Multiple boards can be interconnected externally to produce synchronous analog input sampling. Figure 2.3-2 illustrates the interconnections required. External sync I/O is enabled by setting the ENABLE EXTERNAL SYNC control bit HIGH in the BCR. One of the boards is designated as the *Initiator*, and the remaining boards are designated as *targets*.

A board that is enabled for external sync I/O is designated as a ***target*** by selecting External Sync Input Line in the SAMPLE CLOCK SOURCE field in the Scan and Sync control register. Any other value for the SAMPLE CLOCK SOURCE field designates the board as an ***initiator***. The sync signal can originate either from an initiator board, or externally as an input to a group of targets.

If the ENABLE EXTERNAL SYNC control bit is set HIGH in the BCR, an initiator generates a sync pulse at the selected sample rate, and each of the target boards responds to the sync pulse by acquiring a single sample of all of its designated active channels.

NOTE: To avoid contention on the SYNC I/O line, all initiator/target designations should be assigned before enabling external sync I/O operation. No more than one board can be designated as an initiator.

3.5 Analog Input Control

3.5.1 Input Data Organization

Processed conversion data from the analog-to-digital converters (ADC's) flows directly into the 64K-sample analog input FIFO data buffer, and from the data buffer to the PCI bus as analog input data. The data buffer appears to the PCI bus as a single read-only register.

3.5.1.1 Input Data Buffer

Analog input data from the analog input data buffer is right-justified to the LSB, and occupies bit positions D00 through D15 (Table 3.5-1). D16 is HIGH for all Channel 00 values, and LOW for data from all other channels. Bits D17-D31 are always returned as zero's. An empty buffer returns the value 0000 0001h.

Table 3.5-1. Input Data Buffer

Offset: 0008h **Default: N/A**

DATA BIT	MODE*	DESIGNATION	DESCRIPTION
D00	RO	DATA00	Least significant data bit
D01-D14	RO	DATA01 - DATA14	Intermediate data bits
D15	RO	DATA15	Most significant data bit
D16	RO	CHANNEL 00 TAG	Indicates a Channel-00 data value
D17-D31	RO	(Inactive)	---

* RO indicates read-only access. Write-data is ignored.

3.5.1.2 Data Coding Format

Analog input data is arranged as 16 active right-justified data bits with the coding conventions shown in Table 3.5-2. The default format is offset binary. Two's complement format is selected by clearing the OFFSET BINARY control bit LOW in the BCR.

Note: Unless indicated otherwise, offset binary coding is assumed throughout this document.

Table 3.5-2. Input Data Coding; 16-Bit Data

ANALOG INPUT LEVEL	DIGITAL VALUE (Hex)	
	OFFSET BINARY	TWO'S COMPLEMENT
Positive Full Scale minus 1 LSB	0000 FFFF	0000 7FFF
Zero plus 1 LSB	0000 8001	0000 0001
Zero	0000 8000	0000 0000
Zero minus 1 LSB	0000 7FFF	0000 FFFF
Negative Full Scale plus 1 LSB	0000 0001	0000 8001
Negative Full Scale	0000 0000	0000 8000

3.5.2 Input Data Buffer Control

The Input Data Buffer control register shown in Table 3.5-3 controls and monitors the flow of data through the analog input data buffer. Asserting the CLEAR BUFFER control bit HIGH clears, or empties, the buffer. The Threshold Flag is HIGH when the number of values in the input data buffer exceeds the input threshold value defined by bits D00-D15, and is LOW if the number is equal to or less than the threshold value. An interrupt (Section 3.7) can be programmed to occur on either the rising or falling edge of the threshold flag.

Input data is discarded if the DISABLE BUFFER control bit is set HIGH, but data already present in the buffer is unaffected and can be accessed from the PCIbus.

The Buffer Size register shown in Table 3.5-4 contains the number of input values present in the buffer, and is updated continuously.

Table 3.5-3. Input Data Buffer Control Register

Offset: 000Ch **Default: 0000 FFFEh**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-D15	R/W	THRESHOLD VALUE	FFFEh	Input buffer threshold value.
D16	R/W	CLEAR BUFFER *	0	Clears (empties) the input buffer and processing pipeline when asserted HIGH.
D17	RO	THRESHOLD FLAG	0	Asserted HIGH when the number of values in the input buffer exceeds the THRESHOLD VALUE.
D18	RW	DISABLE BUFFER	0	Prevents data from loading into the buffer when HIGH.
D19-D31	RO	(Inactive)	0	---

*Clears automatically when operation is completed

Table 3.5-4. Buffer Size Register

Offset: 0018h **Default: 0000 0000h**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-D15	RO	BUFFER SIZE	0000h	Number of values in the input buffer
D16-D31	RO	(Inactive)	0	---

3.5.3 Analog Input Function Modes

BCR control field AIM[] selects the analog input signal source, and provides selftest modes for monitoring the integrity of the analog input networks. Table 3.5-5 summarizes the input function modes.

3.5.3.1 System Analog Inputs

With the default value of 'Zero' selected for the AIM[] field in the BCR, all ADC channels are connected to the system analog inputs from the system I/O connector.

Table 3.5-5. Analog Input Function Selection

AIM[2:0]	FUNCTION OR MODE
0	System analog input mode (Default mode).
1	(Reserved)
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.
4-7	(Reserved)

3.5.3.2 Selftest Modes

In the selftest modes, the analog input lines from the system I/O connector are ignored and have no effect on selftest results. Specified board accuracy applies to all selftest measurements, and for critical measurements, the averaged value of multiple readings should be used.

The ZERO selftest applies a Zero reference signal to all input channels, and should produce a nominal midscale reading of 0000 8000h for bipolar inputs. For the +VREF test, a precision reference voltage equal to 99.90% of the positive fullscale value for the selected input range is applied to the input channels, and should produce a nominal reading of 0000 FFDFh.

3.5.4 Sampling Modes

The analog inputs can be sampled in groups of 2, 4, 8, 16, 32 or 64 active channels, or any single channel can be selected for digitizing. The number of active channels is selected by the ACTIVE CHANNELS[] field in the scan and sync control register. Each active channel group commences with Channel-00, and proceeds upward through successive channels to the selected number of channels.

For Single-Channel sampling (ACTIVE CHANNELS[] = 0), the channel to be digitized is selected by the SINGLE-CHANNEL SELECT control field.

3.5.5 Differential Processing

Although the hardware inputs are single-ended in nature, differential processing allows the inputs to appear as either pseudo-differential or full-differential channels. Each of these processing modes is characterized by the reference from which the signal in each channel is measured. Differential processing is selected by the DIFFERENTIAL PROCESSING control field in the BCR as shown in Table 3.5-6.

Table 3.5-6. Differential Processing Modes

BCR D08,09	Designation	Processing Function
0	SINGLE ENDED	Default operating mode. Processing of input data is limited to gain and offset error correction.
1	PSEUDO-DIFFERENTIAL	Channel-00 is the input LO reference for all other channels.
2	FULL DIFFERENTIAL	Each odd-numbered channel is the LO reference for each even-numbered HI channel. I.e.: Channels 00 and 01 become Channel-00 HI and Channel-00 LO, respectively.
3	(Reserved)	

3.5.5.1 Default Single-Ended Processing

For single-ended channels, each input signal is measured with respect to the common input return. That is, each channel reports the difference between the input signal voltage and the voltage present on the common input return. This configuration provides the maximum number of input channels, but allows noise and other forms of interference on the common return line to appear in the signal measurement.

3.5.5.2 Pseudo-Differential Mode

Pseudo-differential processing designates input Channel-00 as the reference for all other channels, and subtracts the sampled value in Channel-00 from the sampled values in all other channels. With this arrangement, noise and interference on the common return line is essentially cancelled, and the Channel-00 input line can be used as a 'remote sense' line for Channels 01-63. Channel-00 can no longer be used as a general signal input path, and the number of active input channels is reduced from 64 to 63.

3.5.5.3 Full Differential Mode

If full-differential processing is selected, each odd-numbered channel becomes the reference, or return, for the associated even-numbered channel. For example, Channel-01 becomes the reference for Channel-00, and Channel-00 data is reported as the difference between the actual Channel-00 input signal and the signal in Channel-01. Odd-numbered channels do not appear in the data buffer when operating in full-differential mode.

3.5.5.4 Differential Scaling Considerations

Because differential processing operates by subtracting the signals in two channels, all input ranges are effectively doubled when either differential mode is selected. With the ±10V range and pseudo-differential operation selected for example, Channel-00 data can have any value from -10V to +10V, and all channels using Channel-00 as a reference also have the same range of values. The difference signal then can have any value from -20V to +20V, and the effective input range becomes ±20V.

> **Note: Although differential processing effectively doubles the output data range, the hardware input levels are still restricted to the selected input range.**

In addition to doubling the effective input voltage range, differential processing also always produces a bipolar output signal. Since a reference channel can have a value that is greater than or less than that in a signal channel, differentially processed data is always bipolar in nature.

3.6 Autocalibration

To obtain maximum measurement accuracy, autocalibration should be performed after:

- Power warmup,
- PCIbus reset,
- Input range change,
- Sample rate change, if greater than 20 kHz.

A small error, on the order of 0.04-percent, can be introduced when the input range is changed, or when a large change (>20 kHz) occurs in the sample rate. The following typical sequence ensures that autocalibration is applied to eliminate this error:

- Select the new input range, or enable the new sample rate source and frequency,
- Invoke autocalibration and wait for completion,
- Disable the sample rate source,
- Clear the buffer,
- Re-enable the sample rate source.

During autocalibration, no control settings are altered and external analog input signals are ignored.

Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. The control bit returns LOW automatically at the end of autocalibration. Autocalibration can be invoked at any time, and has a duration of approximately 0.5 second. Completion of the operation can be detected either by selecting the 'Autocalibration Operation Completed' interrupt condition (paragraph 3.7) and waiting for the interrupt request, or by simply waiting a sufficient amount of time to ensure that autocalibration has been completed.

To compensate for component aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the necessary correction values in internal memory. If a board is defective, the autocalibration process may be unable to successfully calibrate the inputs. If this situation occurs, the AUTOCAL PASS status bit in the BCR is cleared LOW at the end of the autocalibration interval, and remains LOW until a subsequent initialization or autocalibration occurs. AUTOCAL PASS is initialized HIGH, and remains HIGH unless an autocalibration failure occurs.

3.7 Interrupt Control

In order for the board to generate a PCI interrupt, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request (Section 3.7.1)
b. The *PCI interrupt* must be enabled (Section3.7.2).

If the internal controller generates a local interrupt request, a PCI bus interrupt will not occur unless the PCI interrupt has been enabled as described in Paragraph 3.7.2.

3.7.1 Local Interrupt Request

The Interrupt Control Register shown in Table 3.7-1 controls the single local interrupt request line. Two simultaneous source conditions (IRQ 0 and1) are available for the request, with multiple conditions available for each source. IRQ 0 and 1 are logically OR'd together to produce the single interrupt available to the board.

When one or more selected conditions occur for either of the IRQ's, a local interrupt request is generated and the associated IRQ REQUEST flag bit is set HIGH. The request remains asserted until the PCI bus clears the request flag. A local interrupt request is generated automatically at the end of initialization, through IRQ0.

Interrupt conditions are *edge-sensitive*, and an interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

3.7.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled or disabled by setting the control bits shown in Table 3.7-2 to the indicated states in the *Runtime Interrupt Control/Status Register.*

The address of the interrupt control/status register usually is obtained by adding 68h to the base address that is located in the PCI configuration register space.

Table 3.7-1. Interrupt Control Register

Offset: 0000 0004h **Default: 0000 0008h**

DATA BIT	MODE	DESIGNATION	DEF	VALUE	INTERRUPT CONDITION
D00-02	R/W	IRQ0 A0,1,2	0	0	Idle. Interrupt disabled unless initializing. Default state after reset.
				1	Autocalibration operation completed
				2	Input sample initiated (Sync)
				3	Input sample completed (data ready)
				4-7	(Reserved)
D03	R/W	IRQ0 REQUEST	1*	---	Group 0 interrupt request flag. Set HIGH when the selected interrupt condition occurs. Clears the request when cleared LOW by the bus.
D04-06	R/W	IRQ1 A0,1	0	0	Idle; no interrupt condition selected.
				1	Input buffer threshold LOW-HIGH transition
				2	Input buffer threshold HIGH-LOW transition
				3-7	(Reserved)
D07	R/W	IRQ1 REQUEST	0	---	Group 1 interrupt request flag. See D03.
D08-31	RO	(Inactive)	0	---	

R/W = Read/Write, RO = Read-Only. * HIGH after reset.

Table 3.7-2. PCI Interrupt Control

Interrupt Control/Status Register Bit	Interrupt Enabled	Interrupt Disabled (Default)
Bit 08	1	0
Bit 11	1	0
Bit 16	1	0

3.8 DMA Operation

DMA transfers from the analog input buffer are supported with the board operating as bus master. Table 3.8-1 illustrates a typical PCI register configuration that would control a non-chaining, non-incrementing DMA transfer, and in which a PCI interrupt is generated when the transfer has been completed. Bit 02 in the PCI Command register (04h) must be set HIGH to select the bus mastering mode. Refer to a PCI-9080 data manual for a detailed description of these registers.

For most applications, the DMA Command Status Register (A8h) should be initialized to the value 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Table 3.8-1. Typical DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial Analog Input Buffer local address (Analog input buffer)	0000 0008h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

Each of 64 single-ended analog input channels contains a dedicated 16-Bit ADC, and input attenuator, and a selftest input switching network (Figure 4.1-1). A PCI interface adapter provides the interface between the controlling PCI bus and an internal local controller (Figure 4.1-1). +5 VDC power from the PCIbus is converted into regulated power voltages for the internal analog networks.

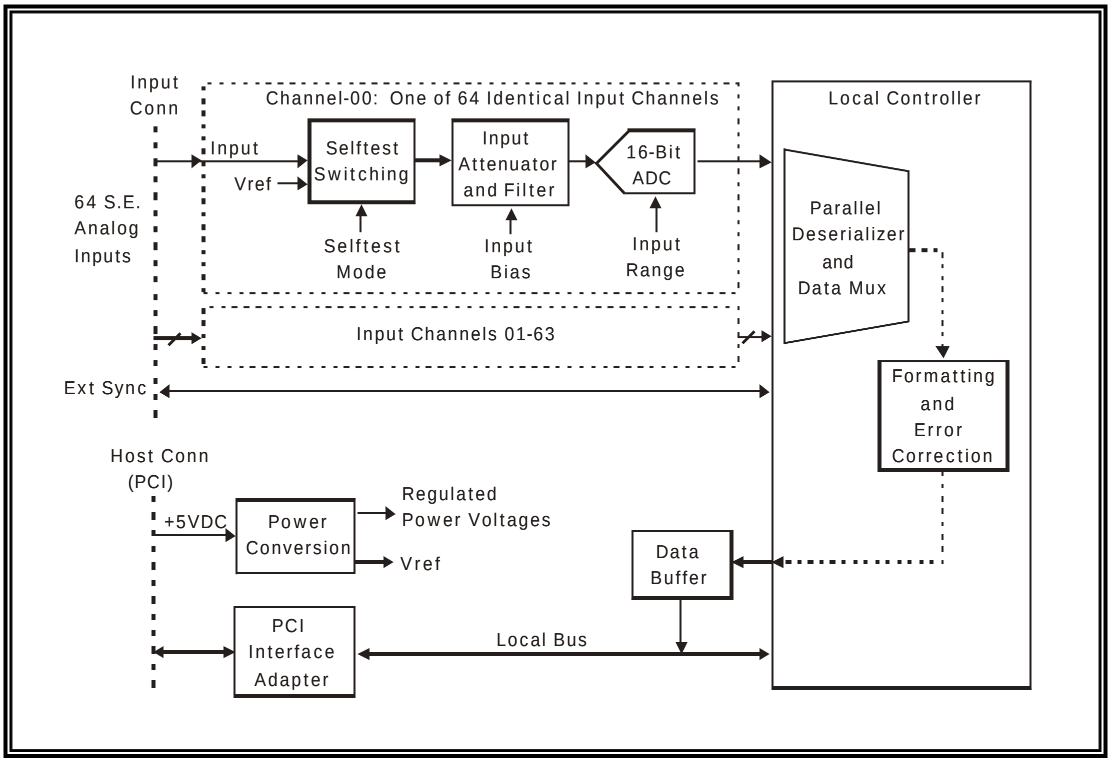

Figure 4.1-1. Functional Block Diagram

Selftest switches at the inputs provide test signals for autocalibration of all input channels, and the input attenuator is biased to accept bipolar input ranges. The input range is controlled by adjusting the 16-Bit ADC reference voltage. Each input sample is corrected for gain and offset errors with calibration values determined during autocalibration. A 64 Ksample FIFO buffer accumulates analog input data for subsequent retrieval by a PMC host.

Analog input sampling on multiple target boards can be synchronized to a single software-designated initiator board. An interrupt request can be generated in response to selected conditions, including the status of the analog input data buffer.

4.2 Analog Inputs

Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the selftest switches shown in Figure 4.1-1. During normal operation, the ADC's receive system analog input signals from the input connector. For selftest and autocalibration operations, the internal voltage reference can be routed through the selftest switches to the ADC. An input attenuator in each channel provides the necessary scaling and offset parameters to support bipolar input ranges.

Serial data from each ADC is deserialized and multiplexed into a parallel data stream within the local controller. The output of the data multiplexer passes through a digital processor that applies gain and offset correction values obtained during autocalibration. The corrected data is formatted, a tag is attached to all Channel-00 data, and the data is finally loaded into the input of the analog input data buffer.

4.3 Rate Generators

The local controller contains two independent rate generators, each of which divides a master clock frequency by a software-controlled 16-bit integer. Either generator can be assigned as a clocking source for the analog inputs, and the generators can be cascaded to produce very long clocking intervals.

4.4 Data Buffer

A 64K-sample FIFO buffer accumulates analog input data for subsequent retrieval through the PCIbus. The buffer is supported by a 'size' register that tracks the number of values in the buffer, and by a threshold flag that can be used to generate an interrupt request when the number of values in the buffer moves above or below a selected count.

4.5 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all analog input channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

An internal voltage reference is used to calibrate the span of each channel, and a zero-reference is used to calibrate the offset value. Correction values determined during autocalibration are applied to each digitized sample that is acquired during acquisition. Correction values are retained until the autocalibration sequence is repeated, or until power is removed.

4.6 Power Control

Regulated supply voltages of +5 VDC and ±15 VDC are required for the analog networks, and are derived from the +5-Volt input provided by the PCI bus, both by switching regulators and by linear regulators.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A
LOCAL REGISTER QUICK REFERENCE

This appendix summarizes the local registers and principle control-bit fields described in Section 3.

Table 3.1-1. Control and Data Registers

OFFSET (Hex)	REGISTER	ACCESS MODE*	DEFAULT	PRIMARY FUNCTION
0000	BOARD CONTROL (BCR)	RW	0000 4060h	Board Control Register (BCR)
0004	INTERRUPT CONTROL	RW	0000 0008h	Interrupt conditions and flags
0008	INPUT DATA BUFFER	RO	0000 0001h	Analog input data buffer
000C	INPUT BUFFER CONTROL	R/W	000X FFFEh	Input buffer threshold and control
0010	RATE-A GENERATOR	RW	0001 0960h	Rate-A generator freq selection
0014	RATE-B GENERATOR	RW	0000 0050h	Rate-B generator freq selection
0018	BUFFER SIZE	RO	0000 0000h	Number of values in the input buffer
001C	(Reserved)	---	---	Inactive
0020	SCAN AND SYNC CONTROL	R/W	0000 0005h	Channels per scan; Clocking and Sync sources.
0024	(Reserved)	---	---	Inactive
0028	FIRMWARE REVISION **	RO	000x xxxxh	Firmware revision
002C	AUTOCAL VALUES **	R/W	0000 080xh	Autocal value readback.
0030-3F	(Reserved)	---	---	Inactive

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 0000 4060h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	AIM0	0	Analog input mode. Selects system inputs or selftest mode. Defaults to System Inputs mode. .
D01	R/W	AIM1	0	
D02	R/W	AIM2	0	
D03	R/W	UNIPOLAR INPUTS	0	Selects unipolar inputs when HIGH, bipolar inputs when LOW.
D04	R/W	RANGE0	0	Analog input range. Defaults to ±10V range.
D05	R/W	RANGE1	1	
D06	R/W	OFFSET BINARY	1	Selects offset-binary analog I/O data format when asserted HIGH, or two's complement when LOW.
D07	R/W	ENABLE EXTERNAL SYNC	0	Configures the board for external sync I/O when HIGH. (The Scan and Sync control register selects TARGET or INITIATOR mode).
D08-09	R/W	DIFFERENTIAL PROCESSING	0	Selects standard or differential processing modes.
D10-11	R/W	(Reserved)	0	---
D12	R/W	*INPUT SYNC	0	Triggers a single sample of active channels when BCR Input Sync is selected in the Scan and Sync Control Register. Clears automatically upon scan completion,
D13	R/W	*AUTOCAL	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion,
D14	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.

D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets defaults for all registers.
D16-D31	RO	(Reserved)	0	Inactive

Table 3.4-1. Analog Voltage Range Selection (BCR field)

RANGE[1:0]	ANALOG INPUT RANGE
0	±2.5 Volts
1	±5 Volts
2	±10 Volts
3	±10 Volts

Table 3.4-2. Scan and Sync Control Register

Offset: 0020h **Default: 0000 0005h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D02	R/W	ACTIVE CHANNELS	5	Number of active input channels: 0 => Single-Channel mode * 1 => 2 channels (00-01) 2 => 4 channels (00-03) 3 => 8 channels (00-07) 4 => 16 channels (00-15) 5 => 32 channels (00-31); Default value 6 => 64 channels (00-63) 7 =>(Reserved) * Channel selected by Single-Channel Select field below.
D03-D04	R/W	SAMPLE CLOCK SOURCE	0	Selects the analog input sample clocking source: 0 => Internal Rate-A generator output 1 => Internal Rate-B generator output 2 => External Sync input line (Selects TARGET mode) 3 => BCR Input Sync control bit.
D05-D09	R/W	(Reserved)	0	---
D10	R/W	RATE-B CLOCK SOURCE	0	Selects the clock input source for the Rate-B generator: 0 => Master clock 1 => Rate-A generator output.
D11	R/W	(Reserved)	0	---
D12-17	R/W	SINGLE-CHANNEL SELECT	0	Selects the input channel number when operating in the Single-Channel scanning mode.
D18	R/W	(Reserved)	0	---
D19-D31	RO	(Reserved)	0	Inactive

R/W = Read/Write, RO = Read-Only.

Table 3.4-3. Rate Generator Register

Offset: 0010h (Rate-A), 0014h (Rate-B) **Default: 0001 0960 (Rate-A), 0000 0050h (Rate-B)**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D15	R/W	NRATE	---	Rate generator frequency control
D16	R/W	GENERATOR DISABLE	1	Disables the rate generator when HIGH
D17-D31	RO	(Inactive)	0	---

R/W = Read/Write, RO = Read-Only.

Table 3.4-4. Rate Generator Frequency Selection

Nrate (RATE[15..0])		FREQUENCY Fgen *
(Dec)	(Hex)	(Hz)
166	00A6	200,801
167	00A7	199,599
---	---	Fgen (Hz) = 33,333,000 / Nrate

Table 3.5-1. Input Data Buffer

Offset: 0008h **Default: N/A**

DATA BIT	MODE*	DESIGNATION	DESCRIPTION
D00	RO	DATA00	Least significant data bit
D01-D14	RO	DATA01 - DATA14	Intermediate data bits
D15	RO	DATA15	Most significant data bit
D16	RO	CHANNEL 00 TAG	Indicates a Channel-00 data value
D17-D31	RO	(Inactive)	---

* RO indicates read-only access. Write-data is ignored.

Table 3.5-2. Input Data Coding; 16-Bit Data

ANALOG INPUT LEVEL	DIGITAL VALUE (Hex)	
	OFFSET BINARY	TWO'S COMPLEMENT
Positive Full Scale minus 1 LSB	0000 FFFF	0000 7FFF
Zero plus 1 LSB	0000 8001	0000 0001
Zero	0000 8000	0000 0000
Zero minus 1 LSB	0000 7FFF	0000 FFFF
Negative Full Scale plus 1 LSB	0000 0001	0000 8001
Negative Full Scale	0000 0000	0000 8000

Table 3.5-3. Input Data Buffer Control Register

Offset: 000Ch **Default: 0000 FFFEh**

D00-D15	R/W	THRESHOLD VALUE	FFFEh	Input buffer threshold value.
D16	R/W	CLEAR BUFFER *	0	Clears (empties) the input buffer and processing pipeline when asserted HIGH.
D17	RO	THRESHOLD FLAG	0	Asserted HIGH when the number of values in the input buffer exceeds the THRESHOLD VALUE.
D18	RW	DISABLE BUFFER	0	Prevents data from loading into the buffer when HIGH.
D19-D31	RO	(Inactive)	0	---

*Clears automatically when operation is completed

Table 3.5-4. Buffer Size Register

Offset: 0018h **Default: 0000 0000h**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-D15	RO	BUFFER SIZE	0000h	Number of values in the input buffer
D16-D31	RO	(Inactive)	0	---

Table 3.5-5. Analog Input Function Selection (BCR field)

AIM[2:0]	FUNCTION OR MODE
0	System analog input mode (Default mode).
1	(Reserved)
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.
4-7	(Reserved)

Table 3.5-6. Differential Processing Modes

BCR D08,09	Designation	Processing Function
0	SINGLE ENDED	Default operating mode. Processing of input data is limited to gain and offset error correction.
1	PSEUDO-DIFFERENTIAL	Channel-00 is the input LO reference for all other channels.
2	FULL DIFFERENTIAL	Each odd-numbered channel is the LO reference for each even-numbered HI channel. I.e.: Channels 00 and 01 become Channel-00 HI and Channel-00 LO, respectively.
3	(Reserved)	

Table 3.7-1. Interrupt Control Register

Offset: 0000 0004h **Default: 0000 0008h**

DATA BIT	MODE	DESIGNATION	DEF	VALUE	INTERRUPT CONDITION
D00-02	R/W	IRQ0 A0,1,2	0	0	Idle. Interrupt disabled unless initializing. Default state after reset.
				1	Autocalibration operation completed
				2	Input sample initiated (Sync)
				3	Input sample completed (data ready)
				4-7	(Reserved)
D03	R/W	IRQ0 REQUEST	1*	---	Group 0 interrupt request flag. Set HIGH when the selected interrupt condition occurs. Clears the request when cleared LOW by the bus.
D04-06	R/W	IRQ1 A0,1	0	0	Idle; no interrupt condition selected.
				1	Input buffer threshold LOW-HIGH transition
				2	Input buffer threshold HIGH-LOW transition
				3-7	(Reserved)
D07	R/W	IRQ1 REQUEST	0	---	Group 1 interrupt request flag. See D03.
D08-31	RO	(Inactive)	0	---	

R/W = Read/Write, RO = Read-Only. * HIGH after reset.

Table 3.7-2. PCI Interrupt Control

Interrupt Control/Status Register Bit	Interrupt Enabled	Interrupt Disabled (Default)
Bit 08	1	0
Bit 11	1	0
Bit 16	1	0

Table 3.8-1. Typical DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial Analog Input Buffer local address (Analog input buffer)	0000 0008h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

APPENDIX B

MIGRATION FROM PMC-16AI64

FUNCTIONAL AND CONTROL CHANGES

Migration from PMC-16AI64 to PMC-16AI64SS

****

FUNCTIONAL CHANGES:

1. **Input Sampling:**
   Inputs are sampled simultaneously instead of being scanned.

2. **Maximum Sample Rate per-channel:**
   The maximum sample rate per channel is 200 KSPS, and is independent of the number of active channels.

3. **Input Configuration; Differential/Single-Ended:**
   Differential input operation is no longer available. All inputs are now single-ended.

****

APPLICATION CONTROL SOFTWARE ISSUES:

1. Board Control Register (BCR; Section 3.5.3.1 and Table 3.5-5):

- Mode-0 and Mode-1 in the analog input mode control field (AIM[], Table 3.5-5) are revised:

From: (PMC-16AI64):

AIM[2:0]	FUNCTION OR MODE
0	Differential analog input mode (Default mode).
1	Single-Ended analog input mode.

To: (PMC-16AI64SS):

AIM[2:0]	FUNCTION OR MODE
0	System analog input mode (Default mode).
1	(Reserved)

2. Scan and Sync Control Register (Section 3.4.3 and Table 3.4-2):

- The SCAN SIZE field is renamed as ACTIVE CHANNELS,
- The ANALOG INPUTS SCAN CLOCK field is renamed as SAMPLE CLOCK SOURCE.

3. Rate Generator Frequency Calculation (Section 3.4.4 and Table 3.4-4):

The master clock frequency is increased from 24.000 MHz to 33.333 MHz.

4. Selftest Fullscale Value (Section 3.5.3.3):

The selftest positive fullscale value is revised from 94.78 percent of fullscale to 99.90 percent.

****

EXTENDED CAPABILITIES:

1. Unipolar Input Range:

Reserved bit D03 in the BCR (Table 3.2-1) is now active as the UNIPOLAR INPUTS control bit. When this BIT is HIGH, the ±2.5V and ±5V input ranges become 0/+5V and 0/+10V, respectively.

2. Differential Processing:

Reserved bits D08, D09 in the BCR (Table 3.2-1) are now active as the DIFFERENTIAL PROCESSING control field, with functions assigned as:

BCR D08,09	Designation	Processing Function
0	SINGLE ENDED	Default operating mode. Processing of input data is limited to gain and offset error correction.
1	PSEUDO-DIFFERENTIAL	Channel-00 is the input LO reference for all other channels.
2	FULL DIFFERENTIAL	Each odd-numbered channel is the LO reference for each even-numbered HI channel. I.e.: Channels 00 and 01 become Channel-00 HI and Channel-00 LO, respectively.
3	(Reserved)	

Input scaling doubles in the differential processing modes (1 and 2). For example, the ±10V input range becomes a ±20V range when differentially processed. However, actual input voltages are still restricted to the normal ±2.5V, ±5V and ±10V (and unipolar 0/+5V, 0/+10V) range limits.

All differentially processed data is bipolar.

3. Buffer Control:

Reserved bit D18 in the buffer control register (Table 3.5-3) is now active as the DISABLE BUFFER control bit. When this bit is HIGH, writing to the data buffer is inhibited and channel data is discarded. Data already in the buffer is unaffected, and can be accessed from the PCIbus.

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