Joerger ENTERPRISES, INC.

MODEL VTR1012

FOUR CHANNEL, 10MHZ, 12 BIT VME TRANSIENT RECORDER

FEATURES:

- FOUR INDEPENDENT, 10MHZ, 12 BIT TRANSIENT RECORDERS
- 512K SAMPLES PER CHANNEL OF SRAM, 2M WORDS TOTAL
- PRE/POST TRIGGER AND BURST MODE RECORDING
- PROGRAMMABLE INTERNAL CRYSTAL CLOCK OR EXTERNAL CLOCK
- INDIVIDUAL GROUNDING AND FILTERING FOR EACH INPUT
- FRONT PANEL OFFSET CAPABILITY
- "EPICS " SOFTWARE COMPATIBLE
- INTERRUPT STRUCTURE
- BLOCK TRANSFER MODE D16:BLT

The JOERGER ENTERPRISES, INC. MODEL VTR1012 contains four, 12 bit 10MHZ transient recorders packaged in a double height VME module. It is completely self contained. Each channel accepts an analog input, digitizes it using an internal programmable crystal clock or an external clock and loads the data into each channel's on board static memory. Standard memory is 128K samples per channel, 512K is optional. All channels use the same clock and control signals and operate simultaneously. To insure good noise immunity and low channel crosstalk each analog front end is separate. Every channel has its own ground plane and its power lines and analog ground are filtered from each other and the rest of the module. To further insure isolation the front panel connectors are isolated from ground. To insure a wide input voltage range, front panel offset pots with test points are provided for each channel offering full scale offset of ±2 volts. Each channels gain is adjusted to guarantee 12 bit accuracy. To provide the ability to record high frequency input signals, wide bandwidth amplifiers are provided. This versatile performance front end provides the user the ability to handle a wide variety of input signals. Input filters can be used if an application requires. To simplify system implementation "EPICS " software is available.

Registers and memory are accessed as either bytes or words. Each channel's data is in a contiguous block of memory with the module's base address selected by jumper blocks. The three registers CONTROL, GATE DURATION and LOCATION, are accessed via short addressing to a 256 byte block. The control register selects the operating parameters for the module. The gate duration register contains the number of samples to be taken after a trigger. If the external gate is enabled, the gate duration register is not used. The location register contains the pointer to the next memory address to be filled with data.

Several operating modes are available. The normal mode starts digitizing on receipt of a trigger, takes the number of samples set by the gate duration register, stops and sets an interrupt. If the Auto Reset is on, the next trigger will reset the location counter to zero and overwrite the previous samples. If the Auto Reset is off, each following trigger will not reset the location counter and the samples will be stored sequentially until the memory is full. If the "Wrap" mode is off, and the burst cycle is complete, an interrupt is set and further triggers are ignored. If the Wrap mode is on when the memory fills, it will start overwriting the memory and accept triggers until the module is disarmed. In the circular mode the module starts taking data when the unit is armed and cycles through the memory overwriting old data. Upon receipt of a trigger the module takes the number of samples set by the duration counter, stops and sets an interrupt. The complete memory is used with the post trigger samples preset by the gate duration. The balance of the memory contains pretrigger information. The location register can be read out to organize the data.

SPECIFICATIONS

ANALOG INPUT	±2 Volts, other ranges optional. Front panel or P2.
OFFSET	Front Panel ADJ, Testpoint, Full Scale Control
INPUT IMPEDANCE	1K Ohms, 50 Ohms ±2% jumper selectable
BANDWIDTH	10MHz Minimum
DIFFERENTIAL LINEARITY	±.8LSB, No missing codes
CONVERSION RATE	Selected from 8 scaled frequencies using either the SYS Clock, on board crystal oscillator or an external clock.
RESOLUTION	12 Bits, plus overrange.
MEMORY	128K samples/ch Standard, 512K samples/ch Optional.
TRIGGER INPUT	TTL Level, edge triggered, starts post trigger record.
CLOCK INPUT	TTL Level, 50ns minimum pulse width, DC to 10MHZ.
GATE INPUT	TTL Level, up edge starts cycle, down edge stops cycle.
VME INTERFACE	D8 (EO), D16, D16:BLT, A16, A24, A32 SLAVE
CONTROL/STATUS REGISTER	Read/Write: select clock rate, disarm at cycle completion, bus trigger, ext clk, ext gate, ext trigger, reset on trigger, wrap, circular mode, arm, active
GATE DURATION REGISTER	Read/Write: select the number of conversions to perform after a trigger.
LOCATION REGISTER	Read/Write: a pointer to the next sample location
INTERRUPT ID REGISTER	Read/Write Status/ID word
IRQ LEVEL REGISTER	Read IRQ level jumpers
SYSRESET, INTERNAL RESET	Resets module and control register, aborts recording cycle
POWER REQUIREMENTS:	+5V, 2.2A: +12V, 125ma: -12V, 350ma
SIZE:	Single width “VME” 6U card
OPTIONS:	512K SRAM per channel, VTR1012-512 JEI1297

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